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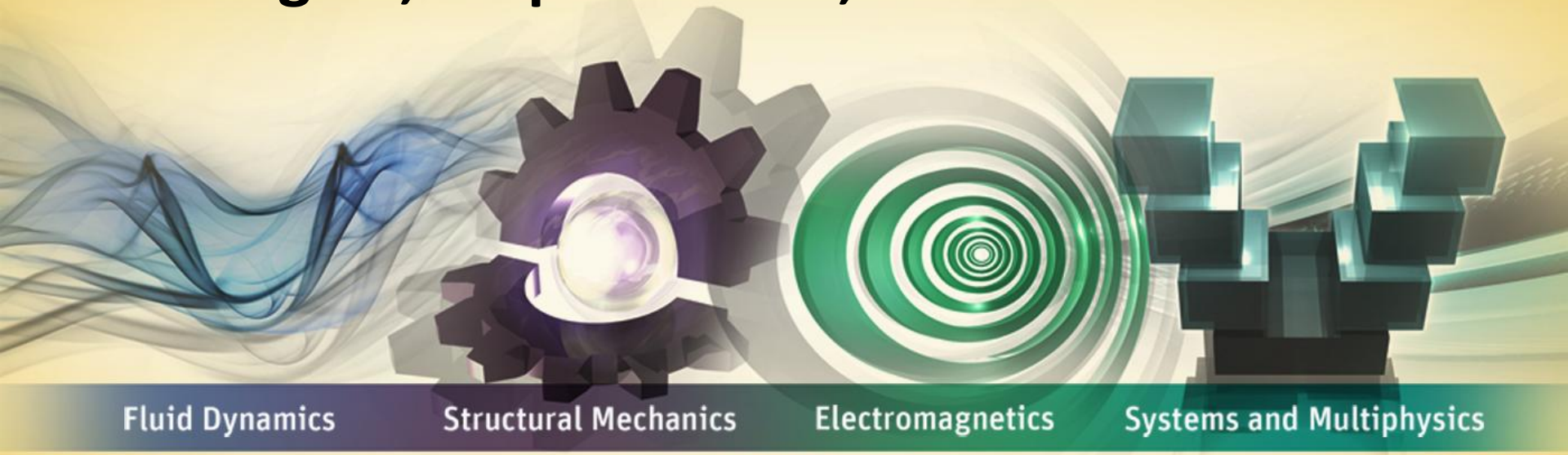
IBIS EMD

Pre-layout versus Post-layout
Thoughts, Requirements, & the Path Forward



Steve Pytel, PhD.

SI Product Manager

Opening Remarks

- The following slides contain my thoughts and opinions on what is needed for and "Interconnect Modeling Protocol" or IMP for short.

- Goal: To enable the industry to perform end to end time and frequency domain circuit simulations with ease.
  - Time Domain Simulation: Implies transient circuit analysis, convolution based circuit analysis, statistical based circuit analysis, IFFT based circuit analysis, and IBIS-AMI analysis (similar to convolution, IFFT, and statistical analysis types)
  - Frequency Domain Simulation: Implies linear network analysis

- Si2 Open3D is in the process of completing an interconnect specification for Chip to System level modeling. I recommend this IBIS working group postpone any decisions on furthering the EMD specification until it can review the upcoming CPIP specification.
  - Once Si2 Open3D completes the specification it will enter a quiet period before the specification can be reviewed by 3rd parties. My opinion is the quiet period should be completed sometime in Q1/2013.
  - You can search (Google for instance) Si2 and CPIP for any available public information or visit http://si2.org/si2_home.php

Pre-layout vs. Post-layout Requirements

Time & Frequency Domain CKT Analysis

Pre-layout considerations (my opinion)

- Assumption: The netlist must support N-port networks: Items in **bold** are in my opinion the most common.
  - Buffer models for signaling
    - **IBIS buffers (.ibs)**
    - **Encrypted buffers (i.e. – HSPICE**, Nexxim, others?)
  - **Touchstone 1** and 2 file formats
  - **W-elements (tabular** and lumped)
  - Passive power delivery networks from previous designs
    - RLCG lumped SPICE networks
    - Distributed RLCGK SPICE networks
    - IBIS .pkg and .ebd networks
  - Active power delivery networks
    - IBIS
    - CPM
    - MCP
  - Signals + PDN
    - Touchstone or Distributed SPICE
  - Others

Post-layout considerations (my opinion)

- Assumption: The netlist must support N-port networks: Items in **bold** are in my opinion the most common.
  - Buffer models for signaling
    - **IBIS buffers (.ibs)**
    - **Encrypted buffers (i.e. – HSPICE**, Nexxim, others?)
  - **Touchstone 1** and 2 file formats
  - **W-elements (tabular** and lumped)
  - **Passive power delivery networks from previous designs**
    - **RLCG lumped SPICE networks**
    - **Distributed RLCGK SPICE networks**
    - IBIS .pkg and .ebd networks
  - Active power delivery networks
    - IBIS
    - CPM
    - MCP
  - **Signals + PDN**
    - **Touchstone or Distributed SPICE**
  - Others

Pytel Key Takeaway: Pre-layout and Post-layout use similar netlisting, but post-layout can be automated with alignment of physical locations. Emphasis on model type differs.

Architectures for Consideration

References: 2.5D & 3D IC

- EEtimes
  - http://www.eetimes.com/design/eda-design/4227311/3D-IC-Design--The-Challenges-of-2-5D-versus-3D-
- MicroNews
  - http://www.i-micronews.com/news/IMEC-methodology-co-optimize-3D-IC-system-design,3217.html
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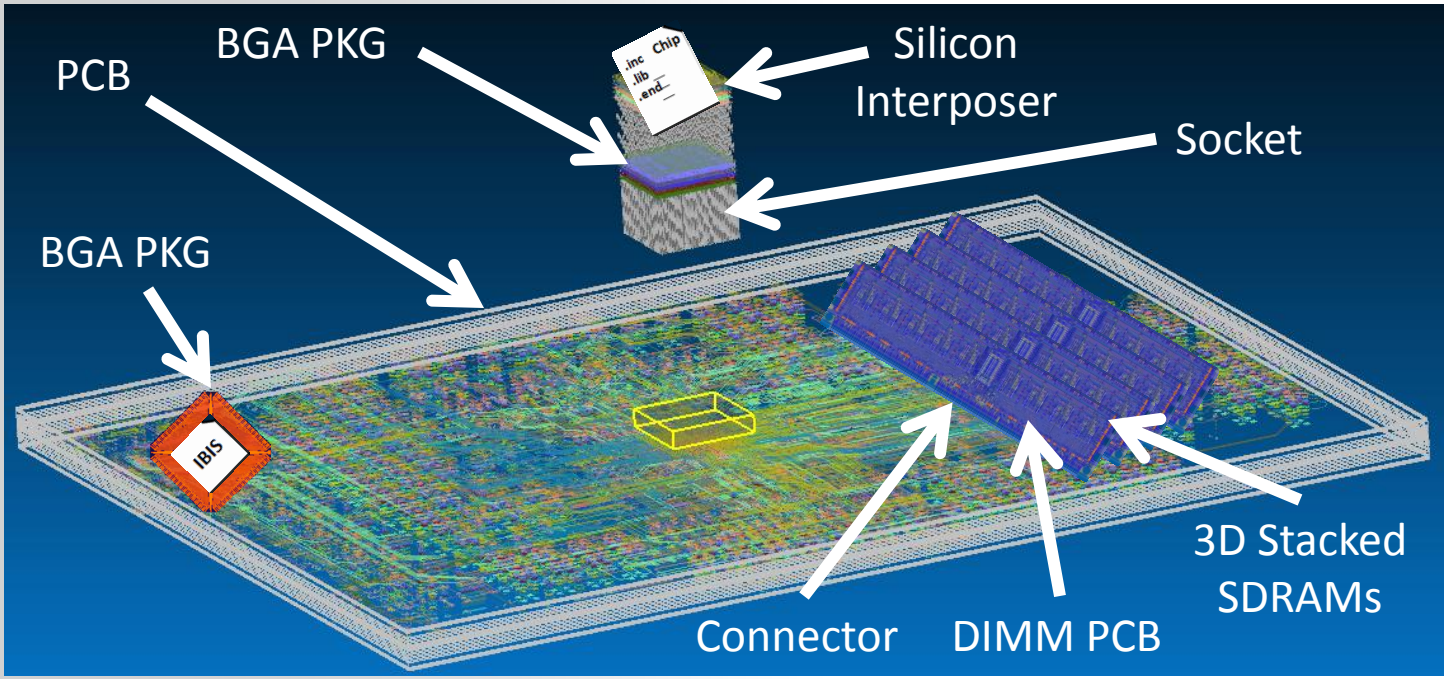
- SemiMD
  - http://semimd.com/blog/tag/tsvs/
- Google Images
  - Search Images 3DIC and 2.5D Interposer

References: Flex Cables

- AreaSX
  - http://www.areasx.com/files/articoli/8143/SX15E_SX16_big.jpg
- Tmart
  - http://www.tmart.com/LCD-Flex-Cable-for-Sony-FP-610-DCR-SR200-SR300_p111909.html
- TSMC Ref. Design Flow 2012
  - http://www.tsmc.com/english/dedicatedFoundry/services/reference_flow.htm
- Other Geometries?
  - Connectors, …

System level Application



- IBIS: Commonly used for DDR simulations
  - DDR4, Wide I/O, Hybrid Memory Cube, …
- IBIS-AMI: Commonly used for SERDES simulations
  - PCIe, SATA, SAS, HDMI, USB, …

Conclusion

- 3DIC and Silicon interposer design is critical for future system integration
- My opinion is IBIS must account for this within any standard it puts forward
  - Another organization is already working on a industry standard to support this.
    - See Si2 Open3D CPIP.
- A key component to creating a successful IBIS specification is distinction of Pre-layout versus Post-layout in my opinion.
  - Current EMD proposal doesn't have support for an automated post-layout solution that would include alignment from Die to System.
    - Critical design requirement in my opinion
      - This could be optional syntax to support both pre- and post-layout requirements
  - Current EMD proposal should be viewed with regards to how IBIS is mainly utilized today: My opinions are listed below:
    - Memory simulations for transient circuit simulation
      - Not including 3DIC and Silicon interposer geometries would significantly reduce the usefulness of any EMD proposal in my opinion.
    - SERDES simulations using IBIS-AMI