**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: *Draft 23 – September 16, 2015***

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS*

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**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS with interconnect modeling features to support broadband and coupled package and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to the new Terminal definitions defined for buffers.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

Definitions:

Enhanced interconnect descriptions in IBIS, called hereinafter “IBIS Interconnect Models”, rely on several assumptions:

1. IBIS Interconnect Models can be described either using IBIS-ISS subcircuit files or Touchstone files. Interconnect Model definitions may be included inside an IBIS file, but neither IBIS-ISS nor Touchstone data may be included inside an IBIS file.
2. If two points in an IBIS Interconnect Model are “Linked”, then there is either a low resistance DC electrical path between the two points, or a small insertion loss at the Nyquist frequency between the two points. For the purposes of IBIS Interconnect Models, “point” and “node” refer to identical locations.
3. IBIS Components, and therefore IBIS Interconnect Models, contain terminals consisting of Pins, Die Pads, Buffer I/O Terminals, and Buffer Supply Terminals. Pins are defined under the [Pin] keyword, and may be I/O, POWER, GND, or NC.
4. For each I/O Pin, there is a single, associated Die Pad and single, associated Buffer I/O Terminal. All of these shall be considered “Linked”.
5. Under [Pin], for each Signal\_name associated with Model\_name POWER or GND, all Pins, Die Pads and Buffer Supply Terminals that use that Signal\_name are “Linked”
6. IBIS assumes that each I/O [Pin] is connected to one Die Pad and one Buffer I/O Terminal. Two differential I/O pins shall be connected to two differential die pads and either two single-ended Buffer I/O Terminals or a single true differential Buffer I/O Terminal.
7. If multiple Buffer Terminals (Supply or I/O) are connected to a single pin, EMD shall be used for the interconnect description.
8. An Interconnect Model may describe the relationship between a single Pin and Buffer Terminal (Supply or I/O), a signle Pin and linked Die Pad, or between a single Die Pad and a Buffer Terminal (Supply or I/O). An Interconnect Model may also describe connections between multiple Pins and multiple Buffer Terminals (Supply and I/O), multiple Pins and multiple Die Pads, or multiple Die Pads and multiple Buffer Terminals (Supply and I/O).

**ANY OTHER BACKGROUND INFORMATION:**

Parameter is shorted to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File\_names are not quoted to be consistent with Corner in the multi-lingual syntax.

For File\_TS, all columns typ, min, and max are entered (or NA for either or both min and max) to follow the corner syntax convention used for most IBIS keywords and subparameters. The typ entry is required, and the typ entry value is used by the EDA tool for any NA entry. The same typ, min, max convention is used for the subparameter Param.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner . Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

The following keywords should be added as their own Chapter. The current Chapter 7 should be modified with the existing text placed in a sub-section called “[PACKAGE MODEL]”.

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**7 PACKAGE MODELING**

Several types of package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector] and the keywords associated with it

The lumped formats are described in the [Package] and [Pin] keyword defintions above. The [Package Model] format is described in this chapter, while Interconnect Model Selectors are described in Chapter 13.

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**13 INTERCONNECT MODEL SELECTORS**

This chapter defines an advanced format for interconnect descriptions that may be used for packages as well as other types of interconnect between buffer models and pins, for signal and power path modeling purposes.

*Keyword:* [Interconnect Model Selector]

*Required:* No

*Description:* Used to list available interconnect models for the component.

*Usage Rules:* Interconnect Models are described by IBIS-ISS or Touchstone files that are between the Pins, Die Pads and Buffer Terminals (Supply and I/O) of a Component.

A component may have none, one or more than one Interconnect Model associated with it. If any Interconnect Models exist for the Component, they shall be listed in this section. An Interconnect Model Selector is required even if only a single Interconnect Model is associated with the Component.

The section under the [Interconnect Model Selector] keyword shall have two fields per line, with each line defining the Interconnect Models associated with the Component. The fields shall be separated by at least one white space. The first field lists the Interconnect Model name (up to 40 characters long). The second field is the name of the file containing the Interconnect Model. If the Interconnect Model is in this IBIS file, then the second field shall be “\*”.

The file containing the Interconnect Model shall be located in the same directory as the .ibs file. The file name shall follow the rules for file names given in Section 3, "GENERAL SYNTAX RULES AND GUIDELINES".

The first entry under the [Interconnect Model Selector] keyword shall be considered the default by the EDA tool. Each Interconnect Model name may only appear once under the [Interconnect Model Selector] keyword for a given Component.

*Example:*

[Interconnect Model Selector]

 QS-SMT-cer-8-pin-pkgs\_iss \*

 QS-SMT-cer-8-pin-pkgs\_sNp QS-SMT-cer-8-pin-pkgs\_sNp.ipkg

[End Interconnect Model Selector]

*Keyword:* [**End Interconnect Model Selector**]

*Required:* Yes, for each instance of the [Begin Interconnect Model Selector] keyword

*Description:* Indicates the end of the Interconnect Model selector data.

*Example:*

[End Interconnect Model Selector]

*Keyword:* [Begin Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an interconnect model description.

*Usage Rules:* [Begin Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed.

*Example:*

[Begin Interconnect Model] QS-SMT-cer-8-pin-pkgs\_iss

The following subparameters are defined:

Manufacturer

Description

Param

File\_TS

File\_IBIS-ISS

Unused\_Terminal\_Termination

Number\_of\_Terminals

Terminal

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Manufacturer rules:

This optional subparameter specifies the name of the interconnect’s manufacturer. The length of the manufacturer’s name shall not exceed 40 characters. Blank characters are permitted.

Description rules:

This optional subparameter provides a concise yet easily human-readable description of what the Interconnect Model represents. The description shall be fewer than 60 characters in length, shall fit on a single line, and may contain spaces.

Unused\_Terminal\_Termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the Terminals of any IBIS-ISS subcircuit or Touchstone networks that are not being used in the [Begin Interconnect Model]/[End Interconnect Model] group. The subparameter name is followed by a single integer argument greater than zero on the same line, separated from the subparameter name by the “=” character and optionally whitespace.

If this subparameter is present, the EDA should connect the unused Terminals to GND through a resistorwith the value of resistance in ohms provided in the argument.

If this parameter is not defined and if Language is IBIS-ISS, then the EDA tool should connect the unused Terminals to GND through a 1 megaohm resistor. If Language is Touchstone, then the EDA tool should connect the unused Terminals to GND through a resistor with the Touchstone File reference resistance of the Terminal.

Only one Unused\_Terminal\_Termination subparameter may appear for a given [Begin Interconnect Model] keyword.

Number\_of\_Terminals rules:

The Number\_of\_Terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name is followed by a single integer argument greater than zero on the same line, separated from the subparameter name by the “=” character and optionally whitespace. Only one Number\_of\_Terminals subparameter may appear for a given [Begin Interconnect Model] keyword. The Number\_of\_Terminals subparameter shall appear before the Terminal subparameter for a given Interconnect Model.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS.

The numerical value rules follow the scaling conventions in Section 3, GENERAL SYNTAX RULES AND GUIDELINES. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to The Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ\_s2p" | file name string passed

 | into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_IBIS-TS (documented next) is required for a [Begin Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_name, and circuit\_name (.subckt name) for an IBIS-ISS file. . The referenced file under file\_name shall be located in the same directory as the .ibs file.

*Example:*

| file\_type file\_name circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Begin Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file name for a Touchstone file. The Touchstone file under file\_name shall be located in the same directory as the .ibs file.

*Example:*

| file\_type file\_name

File\_TS typ.s8p

Terminal rules:

Terminal records shall appear after the Number\_of\_Terminals subparameter and before the [End Interconnect Model] keyword.

Each Terminal line contains information on a terminal of an IBIS-ISS subckt (or Touchstone file).

Terminal records are of the form

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> Aggressor

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_Terminals argument. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any Terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_Terminal\_Termination rules.

There are three classes of pins in a component, Signal Pins, Supply Pins and No Connect Pins. Supply Pins have model\_name POWER or GND. No Connect Pins have model\_name NC. All other pins are classified as Signal Pins. Package models defined in this section assume that there is one Buffer\_I/O Terminal and one Die Pad for each Signal Pin.

The model of an I/O Buffer has supply terminals in addition to the Buffer\_I/O. These supply (or rail) terminals can be PUref, PDref, PCref, GCref and/or EXTref. The association of the PUref, PDref, PCref, GCref and/or EXTref terminal of a buffer are associate with either bus\_label or signal\_name in the [Pin Mapping] section. These terminals can be connected to interconnect models one of two ways:

1. By specifying a unique interconnect terminal for each I/O Buffer PUref, PDref, PCref, GCref and/or EXTref
2. By assuming that all I/O Buffer supply terminals connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all I/O Buffer terminals that are connected to a specific signal\_name or bus\_label on at least one Supply Pin.

Pads are the location of the interface between the die and the package. Interconnect models can either be between the Pins of a component and the I/O Buffers, or they can be split into models between the Pins of a component and the Pads of the die, and model between the Pads of the die and the I/O Buffer models. There is exactly one Pad (Pad\_I/O) for each Signal Pin. There can be any number of Pads (Pad\_Rail) for each signal\_name or buf\_label on Supply Pins. If interconnect models of supply (rail) networks are split between Pin/Pad and Pad/Buffer models, then the interface of supply connections at the die package interface can be handled in one of two ways:

1. By defining a list of Die Supply Pads, and specifying terminals for some or all of the Die Supply Pads that are connected to a bus\_label or signal\_name on at least one Supply Pin.
2. By assuming that all supply Pads connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all Pads that are connected to a specific signal\_name on at least one Supply Pin.

Pins can be terminals of the interconnect model that connect directly to a PCB board or other type of system connection to an IBIS component. Pins can be Signal Pins (Pin\_I/O), or Supply Pins (Pin\_Rail). An interconnect model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the Supply Pins.
2. By assuming that all supply Pins connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all Pins that are connected to a specific signal\_name on at least one Supply Pin.

Terminal\_type must be one of the following: Buffer\_I/O, PUref, PDref, PCref, GCref, EXTref, Buffer\_Rail, Pad\_I/O, Pad\_Rail, Pin\_I/O or Pin\_Rail. Buffer\_I/O, PUref, PDref, PCref, GCref, EXTref and Buffer\_Rail are terminals of an Interconnect Model that connect directly to I/O Buffers. Pin\_I/O and Pin\_Rail are terminals that are at the Die/Package interface. Pin\_I/O and Pin\_Rail are terminals that are at the Component PCB interface. The Terminal\_type\_qualifier for Terminal\_types Buffer\_I/O, PUref, PDref, PCref, GCref and EXTref must be pin\_name. The Terminal\_type\_qualifier for Terminal\_type Buffer\_Rail may be signal\_name or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pad\_I/O must be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pad\_Rail must be either pad\_name, signal\_name or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pin\_I/O must be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pin\_Rail must be either pin\_name, signal\_name or bus\_label.

The optional Aggressor field is only allowed allowed on Buffer\_I/O records. Connections to Buffer\_I/O terminals may be missing coupling to connects that are not included in this interconnect model.

Do we support an additional Terminal\_type Probe which has the format?

<Terminal Number> Probe <probe name>

The EDA tool may leave this terminal unconnected, or connect it to a high impedance simulator probe element.

The following table summarized the rules described above.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Terminal\_Type | pin\_name | signal\_name | bus\_label | pad\_name | Aggressor |
| Buffer\_I/O | X |   |   |   | A |
| Puref | X |   |   |   |   |
| Pdref | X |   |   |   |   |
| Pcref | X |   |   |   |   |
| Gcref | X |   |   |   |   |
| EXTref | X |   |   |   |   |
| Buffer\_rail |   | Y | Y |   |   |
| Pad\_I/O | X |   |   |   |   |
| Pad\_rail |   | Y | Y | Z |   |
| Pin\_I/O | X |   |   |   |   |
| Pin\_rail | Y | Y | Y |   |   |

For an Interconnect Model using File\_TS with N ports, N is determined from the [Number of Ports] field in a Touchstone 2 file. The [Number of Terminals] in the Interconnect Model shall be N+1. Terminal rules are described below:

* The EDA tool shall use the Pin\_name or Signal\_name specified for the associated Terminal “N+1” entry as the reference node for each of the N ports.
* Terminal/Port Mapping
	+ Terminal              Port
	+ 1                              1
	+ 2                              2
	+ …
	+ N                             N
	+ N+1 reference
* If a Port is not connected, then it shall be terminated by the EDA tool with a resistor to the node on Terminal N+1. The resistance shall be the Port Reference Impedance.
* It shall be an error if Terminal N+1 is not specified to be connected to a Pin, a Pad, or a Buffer that is not part of a connection to a Signal\_name that is POWER or GND

The terminals of an interconnect model can be at Pins and Pads, Pins and Buffers or Pads and Buffers. A single interconnect model cannot have terminals at Pins, Pads and Buffers.

*Examples:*

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

D1    DQS+        DQS

D2    DQS-        DQS

P1    VDD         POWER

P2    VDD         POWER

P3    VDD         POWER

P4    VDD         POWER

P5    VDD         POWER

G1    VSS         GND

G2    VSS         GND

G3    VSS         GND

G4    VSS         GND

[Diff Pin] inv\_pin  vdiff  tdelay\_typ tdelay\_min tdelay\_max

D1          D2       NA     NA         NA         NA

[Die Supply Pads]  signal\_name

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

Bus\_label\_signal\_name

A1            VSS          VDD        NC            NC              NC

A2            VSS          VDD        NC            NC              NC

A3            VSS          VDD        NC            NC              NC

D1            VSS          VDD        NC            NC              NC

D2            VSS          VDD        NC            NC              NC

| Full Package/Die Model Complex Power Distribution

Number\_of\_Terminals 29

1  Pin\_I/O     Pin\_name A1  |  DQ1         DQ

2  Pin\_I/O     Pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     Pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     Pin\_name D1  |  DQS+        DQS

5  Pin\_I/O     Pin\_name D2  |  DQS-        DQS

6  Pin\_I/O     Pin\_name P1  |  VDD         POWER

7  Pin\_I/O     Pin\_name P2  |  VDD         POWER

8  Pin\_I/O     Pin\_name P3  |  VDD         POWER

9  Pin\_I/O     Pin\_name P4  |  VDD         POWER

10 Pin\_Rail    Pin\_name P5  |  VDD         POWER

11 Pin\_Rail    Pin\_name G1  |  VSS         GND

12 Pin\_Rail    Pin\_name G2  |  VSS         GND

13 Pin\_Rail    Pin\_name G3  |  VSS         GND

14 Pin\_Rail    Pin\_name G4  |  VSS         GND

15 Buffer\_I/O  Pin\_name A1  |  DQ1         DQ

16 Buffer\_I/O  Pin\_name A2  |  DQ2         DQ

17 Buffer\_I/O  Pin\_name A3  |  DQ3         DQ

18 Buffer\_I/O  Pin\_name D1  |  DQS+        DQS

19 Buffer\_I/O  Pin\_name D2  |  DQS-        DQS

20 PUref   Pin\_name A1  |  DQ1         DQ

21 PUref   Pin\_name A2  |  DQ2         DQ

22 PUref   Pin\_name A3  |  DQ3         DQ

23 PUref   Pin\_name D1  |  DQS+        DQS

24 PUref   Pin\_name D2  |  DQS-        DQS

25 PDref   Pin\_name A1  |  DQ1         DQ

26 PDref   Pin\_name A2  |  DQ2         DQ

27 PDref   Pin\_name A3  |  DQ3         DQ

28 PDref   Pin\_name D1  |  DQS+        DQS

29 PDref   Pin\_name D1  |  DQS+        DQS

| Full Package/Die Model Simple Power Distribution

Number\_of\_Terminals 14

1  Pin\_I/O     Pin\_name A1         |  DQ1         DQ

2  Pin\_I/O     Pin\_name A2         |  DQ2         DQ

3  Pin\_I/O     Pin\_name A3         |  DQ3         DQ

4  Pin\_I/O     Pin\_name D1         |  DQS+        DQS

5  Pin\_I/O     Pin\_name D2         |  DQS-        DQS

6  Pin\_Rail    signal\_name   VDD   |  VDD         POWER

7  Pin\_Rail    signal\_name   VSS   |  VSS         GND

8  Buffer\_I/O  Pin\_name A1         |  DQ1         DQ

9  Buffer\_I/O  Pin\_name A2         |  DQ2         DQ

10 Buffer\_I/O  Pin\_name A3         |  DQ3         DQ

11 Buffer\_I/O  Pin\_name D1         |  DQS+        DQS

12 Buffer\_I/O  Pin\_name D2         |  DQS-        DQS

13 Buffer\_Rail signal\_name   VDD   |  VDD         POWER

14 Buffer\_Rail signal\_name   VSS   |  VSS         GND

| Single DQ (A1)

Number\_of\_Terminals 2

1 Pin\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1

| Single DQ (A1) , Split into package and on-die models

Number\_of\_Terminals 2

1 Pin\_I/O     Pin\_name A1

2 Pad\_I/O     Pin\_name A1

Number\_of\_Terminals 2

1 Pad\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1

Full VDD Power Supply Model

Number\_of\_Terminals 9

1 Pin\_Rail   Pin\_name P1  |  VDD         POWER

2 Pin\_Rail   Pin\_name P2  |  VDD         POWER

3 Pin\_Rail   Pin\_name P3  |  VDD         POWER

4 Pin\_Rail   Pin\_name P4  |  VDD         POWER

5 Pin\_Rail   Pin\_name P5  |  VDD         POWER

6 PDref Pin\_name A1  |  DQ1         DQ

7 PDref Pin\_name A2  |  DQ2         DQ

8 PDref Pin\_name A3  |  DQ3         DQ

9 PDref Pin\_name D1  |  DQS+        DQS

Full VDD Power Supply Model split into package and on-die

Number\_of\_Terminals 8

1 Pin\_Rail Pin\_name P1   |  VDD         POWER

2 Pin\_Rail Pin\_name P2   |  VDD         POWER

3 Pin\_Rail Pin\_name P3   |  VDD         POWER

4 Pin\_Rail Pin\_name P4   |  VDD         POWER

5 Pin\_Rail Pin\_name P5   |  VDD         POWER

6 Pad\_Rail Pad\_name VDD1 |  VDD         POWER

7 Pad\_Rail Pad\_name VDD2 |  VDD         POWER

8 Pad\_Rail Pad\_name VDD3 |  VDD         POWER

Number\_of\_Terminals 7

1 Pad\_Rail Pad\_name VDD1 |  VDD         POWER

2 Pad\_Rail Pad\_name VDD2 |  VDD         POWER

3 Pad\_Rail Pad\_name VDD3 |  VDD         POWER

4 PDref  Pin\_name A1   |  DQ1         DQ

5 PDref  Pin\_name A2   |  DQ2         DQ

6 PDref  Pin\_name A3   |  DQ3         DQ

7 PDref  Pin\_name D1   |  DQS+        DQS

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted

Number\_of\_Terminals 2

1 Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail  signal\_name VDD  |  VDD         POWER

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted, split between package and die

Number\_of\_Terminals 2

1 Pin\_Rail      signal\_name VDD  |  VDD         POWER

2 Pad\_Rail      signal\_name VDD  |  VDD         POWER

Number\_of\_Terminals 2

1 Pad\_Rail      signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail   signal\_name VDD  |  VDD         POWER

| Single DQ Crosstalk Model

Number\_of\_Terminals 6

1 Pin\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1 Aggressor

3 Pin\_I/O     Pin\_name A2

4 Buffer\_I/O  Pin\_name A2

5 Pin\_I/O     Pin\_name A3

6 Buffer\_I/O  Pin\_name A3 Aggressor

Example with signal\_name split into bus\_labels

*Examples:*

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

A4    DQ4         DQ

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

Bus\_label\_signal\_name

A1            VSS           VDD1        NC            NC              NC

A2            VSS           VDD1        NC            NC              NC

A3            VSS           VDD2        NC            NC              NC

A4            VSS           VDD2        NC            NC              NC

P1            NC           VDD1        NC            NC              NC

P2            NC           VDD2        NC            NC              NC

G1            VSS           NC         NC            NC              NC

G2            VSS           NC         NC            NC              NC

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted

Number\_of\_Terminals 2

1 Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Pin\_Rail     signal\_name VSS  |  VSS         GND

3 Buffer\_Rail  bus\_label VDD1 |  VDD         POWER

4 Buffer\_Rail  bus\_label VDD2 |  VDD         POWER

5 Buffer\_Rail  signal\_name VSS  |  VDD         POWER

EDA tool hooks up the following terminals to …

1 Pins P1 and P2

2 Pins G1 and G2

3 PUref of buffers A1 and A2

4 PUref of buffers A3 and A4

5 PDref of buffers A1, A2, A3 and A4

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, for each instance of the [Begin Interconnect Model] keyword

*Description:* Indicates the end of the Interconnect Model data.

*Other Notes:* Between the [Begin Interconnect Model] and [End Interconnect Model] keywords is the package model data itself. The data describes any number of interfaces to either IBIS-ISS models or Touchstone files.

*Example:*

[End Interconnect Model]

Keyword: [Bus Label]

*Required:* No

*Description:* Associates a Power or Ground signal\_name will one or more bus\_label names. Bus\_label names can also be associated with specific Pins, Pads or I/O buffer rail terminals. These buss\_labels names can be used to define terminals of interconnect subckts.

*Sub-Params:* signal\_name

*Usage Rules:* The first column must contain a bus\_label. The second column, signal\_name, gives the data book name for the signal on that bus\_label.

The signal\_name must be a signal\_name on a pin that has model\_name POWER or GND.

A bus\_label may not be the same as any signal\_name, or any other bus\_label. A bus\_label may be inferred by its usage in a [Pin Mapping] sub-parameter.

Column length limits are:

[Bus Label] 40 characters max

signal\_name 40 characters max

*Example:*

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* This begins a section in [Component] that contains one line of data assigning die pads as supply nodes. IBIS assumes that for I/O pins (pins that have a Model\_name that is not POWER, GND or NC), there is a one-to-one correspondence between a Pin, a Die Pad and the Buffer I/O connection point. There are no such assumptions for POWER and GND pins. A POWER or GND Signal\_name may have a different number of Pin nodes, die pad nodes and buffer nodes. If the model maker chooses to make separate package and on-die power distribution networks (PDN), then he shall supply a list of nodes (and their associated Signal\_name) that can be used to mate the package and on-die PDN models.

*Sub-Params:* None

*Usage Rules:*  Arguments under the [Die Supply Pads] keyword consist of two strings per line, where the strings define a die pad node name and a corresponding Signal\_name or bus\_label, in that order. Signal\_names and bus\_labels may appear multiple times, but die pad node names may appear only once each under the [Die Supply Pads] keyword.

*Other Notes:* The data in this section consists of a list of die pad node names and their corresponding Signal\_names or bus\_label that can be used to mate package and on-die PDN networks.

*Example:*

[Die Supply Pads]

VDD1 VDD1

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[End Die Supply Pads]**

*Required:* Yes

*Description:* Indicates the end of the [Die Supply Pads] data.

*Other Notes:*

*Example:*

[End Die Supply Pads]

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

The following section should be appended to the end of the IBIS document.

**12 RULES OF PRECEDENCE**

The sections below detail the rules of precedence to be assumed by EDA tools and model makers where multiple keywords may support similar functions.

**12.1 PACKAGES**

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be used by the EDA tool for simulation; any data present in formats numerically lower on the list shall be ignored.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector]