

Ports Is Ports
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May ~~2229~~, 2013

Ports of interconnect subckts in EMD files are relatively straight forward. An EMD file has External Pins and Internal Pins. The External Pins are listed in the External_Pin_List branch. The internal pins are either in the External_Pin_List branch of EMD Reference_Designators or the [Pin] list in ~~.ibs~~[IBIS Components](#) Reference_Designators.

Change all “Port” to “Terminal”

Ports in [IBIS Components](#) ~~.ibs files~~ are more complicated. pin_names (aka pin numbers) listed in the [Pin] section can be Ports. Each pin_name must be unique. There are three kinds of [Pin]s: Signal Pins, Supply Pins and NC Pins. We will ignore NC Pins in the remainder of this document.

Signal Pins have both a signal_name and model_name. There is no requirement that Signal Pin signal_name(s) are unique in IBIS_CHK. Generally, Signal Pin signal_name(s) are unique. It is up to the EDA tool how to deal with this. The only IBIS files I have seen where signal_name(s) are not unique were used on memory data pins which are “swappable”. It is generally accepted that each Signal Pin pin_name is electrically connect to a unique die pad. A die pad is a connection point on the silicon which connects to a substrate via a wire bond or bump pad. (Note, there are other methods of connecting to a die pad.) These die pads can also be Ports. Each Signal Pin pin_name has a buffer located within the silicon. Each buffer has an associated [Model] indicated in the model_name on the Signal Pin [Pin] record. A buffer has a Port (e.g. A_signal) which is electrically connected to the die pad. A buffer subckt has additional ports. Some of these ports are candidate for interconnect Ports (note capitalization is important here). The ports of a buffer that are not candidates for interconnect Ports are stimulus and enable ports (e.g. D_drive, D_enable) of Tx models (Output, I/O, 3-state, ...), and the output ports (e.g. D_receive) of Rx models (Input, I/O, ...). The candidate buffer ports for Ports (besides the Signal Port) are PuRef, PdRef, PcRef, GcRef. If these Ports are not included in the interconnect subckt, then it is the responsibility of the EDA tool to connect supply pins to the buffer directly instead of power delivered to the buffer through the interconnect.

Supply Pins are more complicated. I think we can safely assume (and we know how assume is spelled) that all Supply Pins with the same signal_name are electrically connected (in EMD terms they are in the same Connection). In general, there is no one-to-one mapping of Supply Pins with Supply Die Pads. Since it is important in some power aware simulations to have Ports on both package supply interconnect models and on-die supply interconnect models it will be necessary to define in IBIS a list of Supply Die Pads which are eligible as Ports in package and on-die interconnect models.

There are a number of special cases for Signal Pins that should be noted here. The first case is multiple pin_names connected in the package to a single die pad. This can be easily accomplished by adding a new IBIS [Component] parameter that indicates pin_names with the same signal_names are electrically connected. If this is the case, then there will be one die-pad Port for each unique signal_name associated with Signal Pins. There will continue to be one Port for each Signal Pin pin_name.

A second special case is a single Signal Pin pin_name that is connected to multiple die pads and by inference multiple buffers. This is currently not allowed in IBIS and I suggest that this continue to be forbidden in IBIS. This special case can be handled by describing such a component as a bare die ~~.ibsIBIS component~~ Component in an EMD file. One solution is two pin_names be the same – currently forbidden in parser not in IBIS.

Each Port in an EMD interconnect subckt is associated with a specific External Pin or Internal Pin. Each Port is identified using the syntax:

<External_Designator>.<Pin_Name> <pin_name>

or

<Reference_Designator>.< Pin_Name>

External_Designator should it be required.

The situation for Ports in IBIS Component ~~.ibs~~-package and on-die interconnect is more complex. For package interconnects, the Ports are either pin_name or die_pad name. For on-die interconnects the Ports are either die_pad name or

buffer_name. Since the name space between pin_names, die_pad_names and buffer_names can overlap, it must be necessary to indicate whether a Port is a Pin, Die Pad, or Buffer, and for Buffer Ports it is also necessary to further qualify a Port as being a Signal, PuRef, PdRef, GcRef, or PcRef.

| In addition, IBIS Component .ibs-package models can be either associated with a Connection (i.e. scoped to a specific pin_name, die_pad_name, and buffer_name, or be associated with a [Model] and Supply signal_name. The concept here is that interconnect subckt can be defined for a package and/or on-die interconnect model that can be applied to all of package and/or on-die interconnect for each Connection of a specific [Model]. For example, a [Component] that has 32 DQ pins (DQ<31:0>) that have the same [Model] DQ each uses the same package and/or on-die interconnect model. A variation of this is that for crosstalk simulation, there can be 32 DQ package models (one for each DQ pin as a victim) each with two additional DQ aggressors. The ports for the DQ victim are the specific Pin and die-pad pin for that particular DQ (e.g. DQ<7>) but that the two aggressor DQ channels need not be specified. Knowing the exact electrical length of the DQ victim is often critical, while knowing the exact electrical length of its DQ aggressors is not. This generally the way that IC Vendors characterize the package interconnect.

| The syntax of an EMD and .ibs fileIBIS Component to define and name Ports that are candidate for interconnect. IBIS Component .ibs files have additional Buffer ports which may or may not be used for interconnect Ports. Once one goes into the Interconnect branch of EMD, IBIS package and IBIS On-Die, the syntax is remarkably similar, except that there is additional flexibility in assigning IBIS pin, pad and buffer Ports to interconnect Ports. This concept must be agreed to before specifying the detailed leaves of interconnect Ports.

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There are three fundamental issues we will need to make regarding enhancements to .ibs files that we should at least identify:

1. Do we support a different number of supply die pads than supply pins?
 - a. Add a [Die Pad] section to .ibs
2. Do we support stacked die?
 - a. Add to the [Component] section:
 - i. [Stacked Die] <N>
 - b. Add to a pin instance
 - i. <pin name> <signal name> <model> r l c Stacked=N
 - c. How is chip enable handled?
 - d. Are all stacked chips identical?
3. Do we support multiple pins connected to one die pad?
 - a. Currently we allow multiple pins to have the same signal_name. I have seen this on memory data lines.
 - b. Add to the [Component] section:
 - i. Same Signal Name Is One Die Pad True|False
 - ii. Default False
 - iii. If True, then all pins with the same Signal_Name are connected to single Die Pad and Single Buffer.
4. Do we support multiple die pads on one die connected to one pin?
 - a. No?
5. Do we support multiple buffers connected to one die pad?
 - a. No?