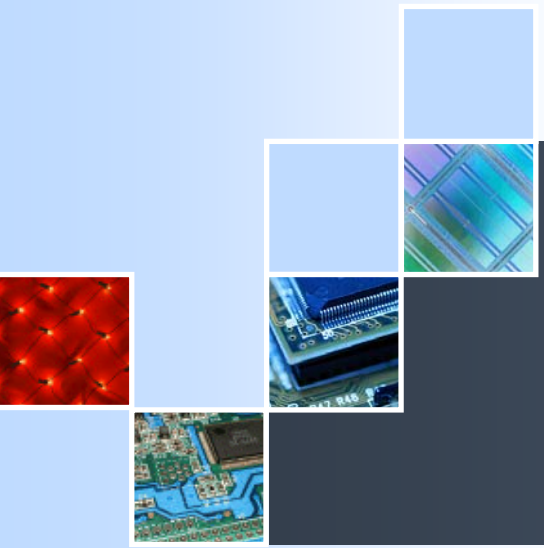


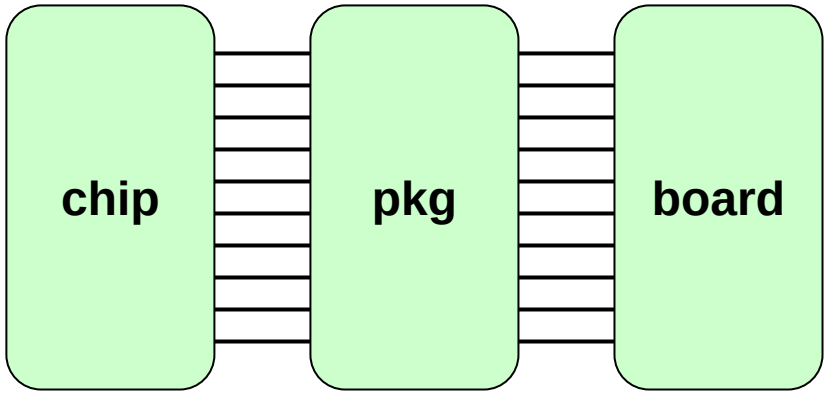
Model Connection Protocols
for Chip/Package/Board System-level Analysis

IBIS Interconnect Task Group Meeting

November 11, 2009

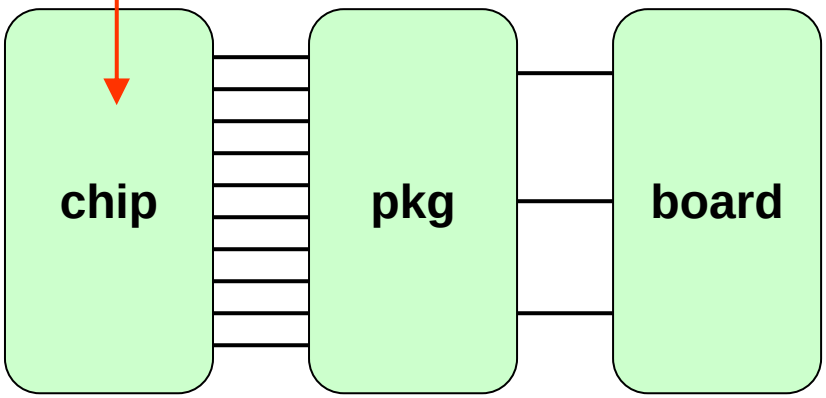
Brad Brim, Sigrity Inc.

System Analysis



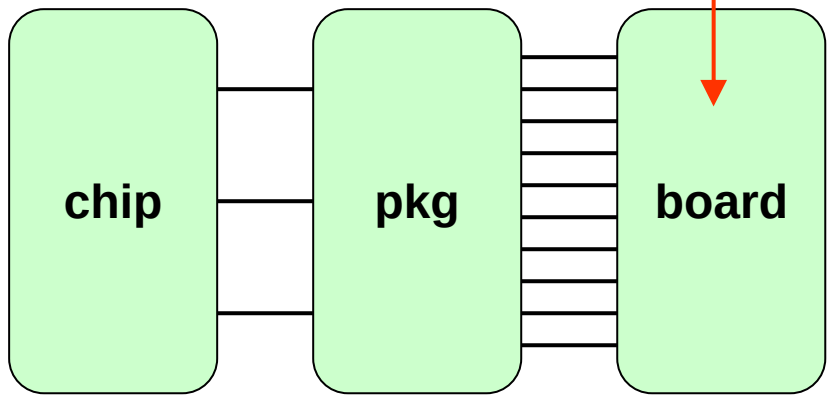
Physical connectivity

Observation



Chip-centric model abstraction

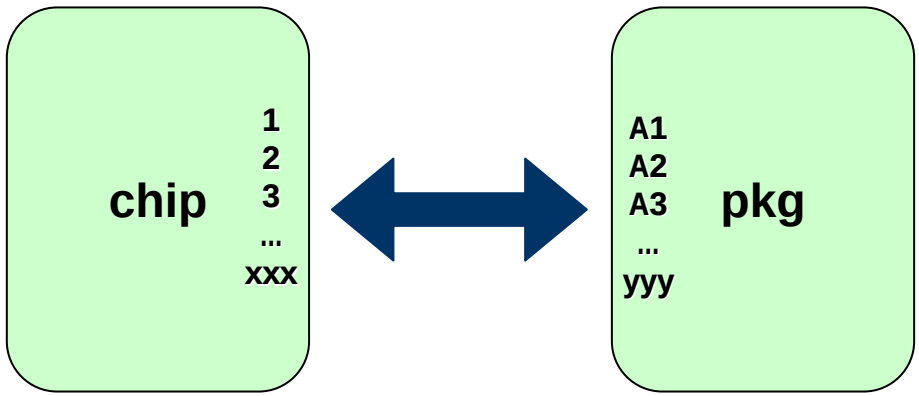
Observation



Board-centric model abstraction

System-level Analysis Challenges

- How do I …
  1. know which pins of one model to connect to the pins of another model?
  2. reliably and quickly connect these models in a netlist or schematic?



Requirements

- Chip/package/board systems have many physical connections (pins)
  - chip-package boundary ≈ 100 – 6000
  - package-board boundary ≈ 100 – 2500
- Not all electrical models can have pin-level resolution
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools
- Adequate modeling may not be possible with net-level resolution
  - especially, if this low resolution is applied throughout the entire system
    - NOTE: “net-level resolution” groups all pins for each net at a domain boundary
- Support is required for
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools

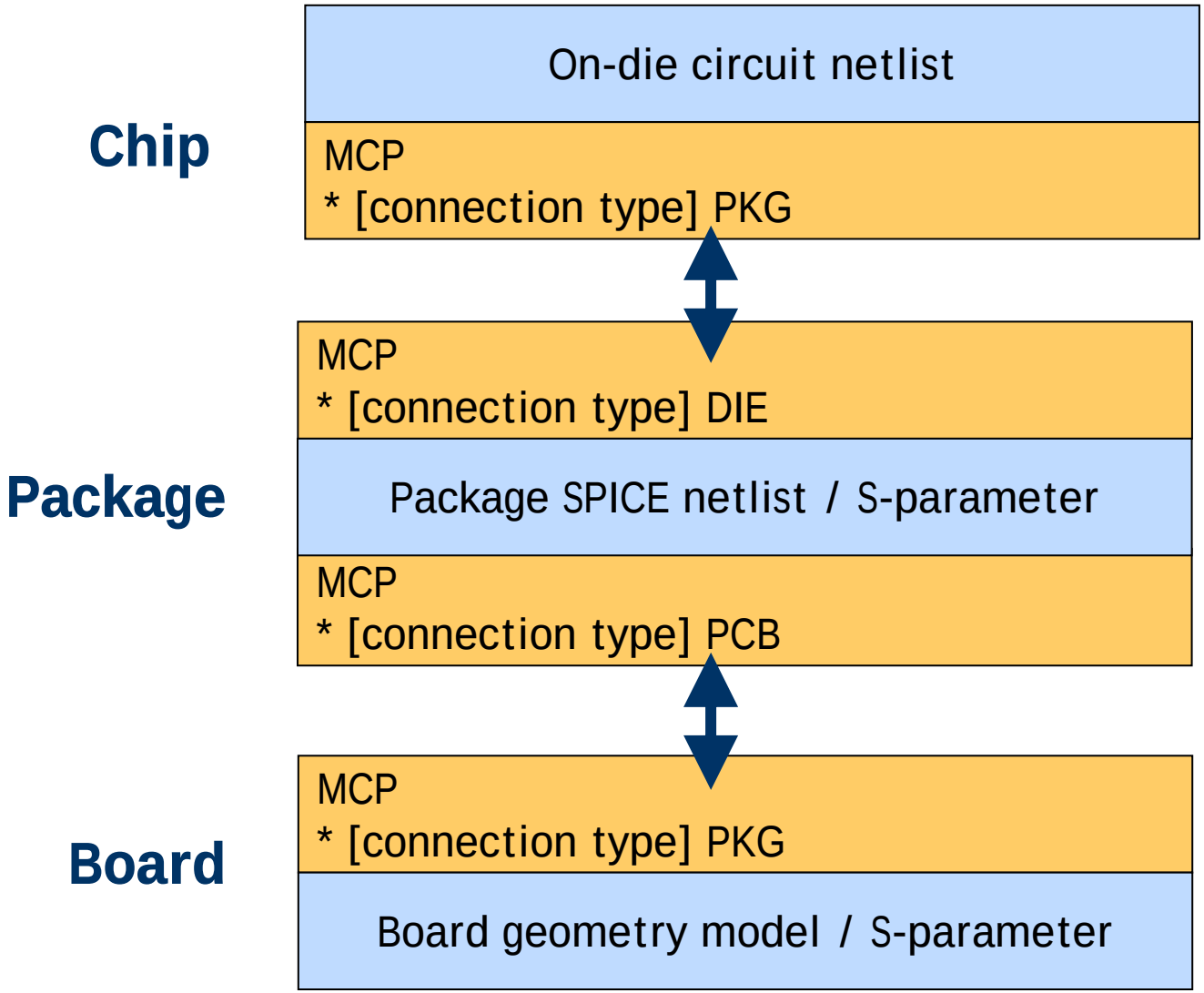
Existing Model Connection Protocols for Chip/Package/Board Analysis

- Sigrity MCP (**M**odel **C**onnection **P**rotocol)
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board system analysis
  - version 1.1 available with user-requested pin locations for support where pin name mismatches exist
- Apache CPP
  - defined by Apache
    - definition covered under NDA
- Implemented as model “headers”
- Contained within model-native comment lines
  - model could be either subcircuit or data file

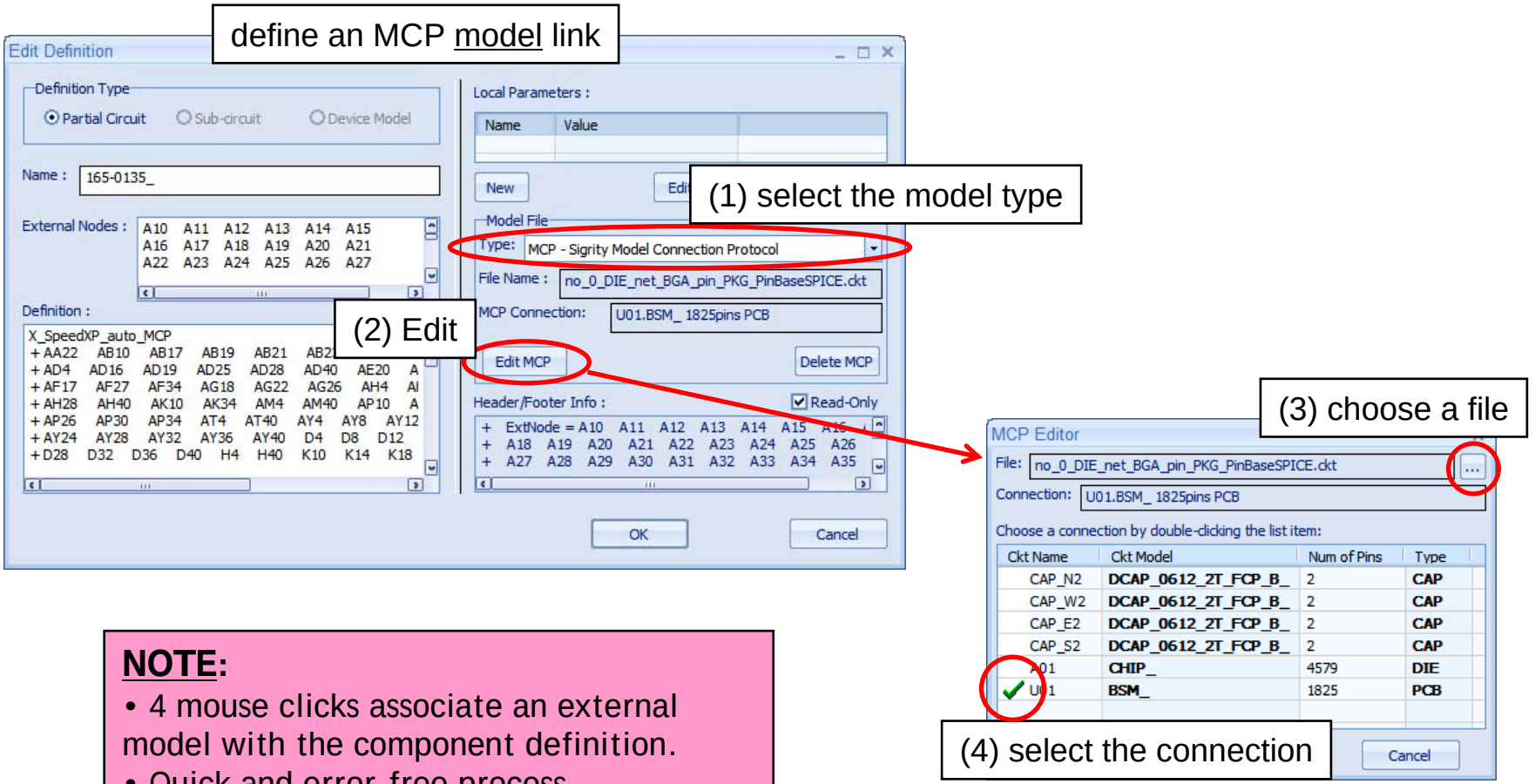
A Typical Model Connection Protocol
(Sigrity MCP)

```
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}
* [MCP Source] source text
* [Coordinate Unit] unit
* [Connection] connectionName  partName  numberPhysicalPins
*   [Connection Type] {DIE|PKG|PCB}
*     [Power Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*    [Ground Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*     [Signal Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
* [MCP End]
```

Concept of the Model-to-Model Link by MCP



EDA Mapping of the MCP package model



NOTE:

- 4 mouse clicks associate an external model with the component definition.
- Quick and error-free process.
- Can also support component creation and automated linking of terminals to physical locations in EDA tool by applying (X,Y) pin positions in the protocol.

Observations

- A connectivity protocol is needed by designers and EDA companies
  - the need is short term
- Semiconductor companies are moving quickly to apply chip/package codesign flows
  - more quickly than previously observed
  - users are implementing multi-vendor flows
  - there are multiple open and closed connectivity protocols
    - with potential for more in the future
    - some vendors are hesitant to implement a protocol defined by another vendor
  - users are asking for an industry “standard” connectivity protocol
- This group may wish to engage in detailed discussion of Connectivity Protocols
  - Sigrity is willing to share its MCP definition as a basis for discussion and possible modification/extension to an industry-consensus connectivity protocol
  - it will be important to discuss the breadth of requirements by users and EDA companies to assure the selected protocol is adequately general

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Thank You!