**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** TBD draft 2 (March 3, 2019)

**ISSUE TITLE:** *Electrical Descriptions of Modules*

**REQUESTOR:**  Walter Katz, Signal Integrity Software (SiSoft)

**DATE SUBMITTED:**

**DATE REVISED:**

**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

There is a need to describe modules that consist of one or more ICs or modules mounted on a PCB, MCM or substrate that connects them to a system thru a set of pins. The following BIRD proposes a new type of file called .emd (Electrical Module Description) that addresses this need. This proposal does not encompass an electrical description of connectors and other interconnect devices.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible description of module interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| * The model maker must be able to provide interconnect models representing modules, using a combination of IBIS-ISS and Touchstone formats. |  |
| * Touchstone models without an IBIS-ISS wrapper circuit must be supported. |  |
|  |  |
| * An interconnect model may connect one signal name or any combination of signal names on one [Begin Module Description]. | Coupled models are supported. |
| * IBIS component pin terminals associated with I/O pins must be assignable to interconnect model terminals directly by pin name. |  |
| * IBIS component pin terminals associated with POWER and GND rail pins must be assignable to interconnect model terminals directly by pin name, or indirectly by [Pin] signal\_name. |  |
| * The model maker must be able to provide alternative interconnect models for any given set of pins. | For example for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
|  |  |
| * The model user must be able to locate all interconnect models that include s specified set of pins it must analyze, | Simulation netlisting begins with a list of pins that must be simulated. |
| * The model user must be able to determine all the pins that a given interconnect model includes. | Once a model is chosen, it may add more pins to the simulation. |
| * The model user must be able to determine how to terminate any terminals of an interconnect model not necessary for an analysis. | May need to handle s-parameter and circuit models differently. |
|  |  |
| * The model user must have useful information needed to make the choice between alternative interconnect models that differ only in characteristics other than the model format and the set of pins included. | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
|  |  |
|  |  |
| * The model user must be informed which pins of an interconnect model have been modeled with coupling to other pins, sufficient for the former to represent the victim pins and the latter all the aggressor pins in a crosstalk simulation. |  |

**BACKGROUND INFORMATION/HISTORY:**

STATEMENT OF THE RESOLVED SPECIFICATIONS: The following text is placed in the specification after the .pkg file description and before the

[End] keyword description.

**<# TBD> ELECTRICAL MODULE DESCRIPTION**

**INTRODUCTION**

A “module” is the generic term to be used to describe a printed circuit board (PCB), Multi Chip Module (MCM), stacked die, interposer or substrate which can contain components or modules, and which can connect to another board or module through a set of user visible pins. The electrical connectivity of such a board or module level component is referred to as an “Electrical Module Description”. For the perposes of the rest of this section, module shall mean PCB, MCM, stacked die, interposer, substrate or similar methods of making connections between electrical modules.

For example, a SIMM module is a module level component that is used to attach several DRAM components on the PCB to another module through edge connector pins. An electrical module description file (a .emd file) is defined to describe the connections of a module level component between the module pins and its components on the module.

What is, and is not, included in an Electrical Module Description is defined by its boundaries. For the definition of the boundaries, see the Description section under the [Interconnect Model] Keyword.

Usage Rules:

A .emd file is intended to be a stand-alone file, not referenced by or included in any .ibs or .pkg file. Electrical Module Descriptions are stored in a file whose name is <filename>.emd, where <filename> must conform to the naming rules given in Section 3 of this specification. The .emd extension is mandatory.

Contents:

A .emd file is structured like a standard .ibs file. It must contain the following keywords, as defined in IBIS: [IBIS Ver], [File Name], [File Rev], and [End]. It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright].

The actual module description is contained between the keywords [Module] and [End Module Description], and includes the keywords listed below:

[Module]

[End Module]

[Manufacturer]

[Description]

[Number Of Pins]

[Pin List]

[Interconnect Model Group]

[End Interconnect Model Group]

[Interconnect Model Set]

[End Interconnect Model Set]

[Interconnect Model]

[End Interconnect Model]

[Reference Designator Map]

[End Module]

Only one [Module]/[End Module] keyword pair is allowed in a .emd file.

**KEYWORD DEFINITIONS**

*Keyword:* [IBIS Ver]

*Required:* Yes

*Description:* Specifies the IBIS template version. This keyword informs electronic parsers of the kinds of data types that are present in the file.

*Usage Rules:* [IBIS Ver] must be the first keyword in any .ibs file. It is normally on the first line of the file, but can be preceded by comment lines that must begin with a “|”.

*Example:*

[IBIS Ver] 8.0 | Used for template variations

*Keyword:* [Comment Char]

*Required:* No

*Description:* Defines a new comment character to replace the default “|” (pipe) character, if desired.

*Usage Rules:* The new comment character to be defined must be followed by the underscore character and the letters “char”. For example: “|\_char” redundantly redefines the comment character to be the pipe character. The new comment character is in effect only following the [Comment Char] keyword. The following characters MAY be used:

! " # $ % & ' ( ) \* , : ; < > ? @ \ ^ ` { | } ~

*Other Notes:* The [Comment Char] keyword can be used anywhere in the file, as desired.

*Example:*

[Comment Char] |\_char

*Keyword:* [File Name]

*Required:* Yes

*Description:* Specifies the name of the .ibs file.

*Usage Rules:* The file name must conform to the rules in paragraph 3 of Section 3, "GENERAL SYNTAX RULES AND GUIDELINES". In addition, the file name must use the extension “.ibs”, “.pkg”, or “.ebd”. The file name must be the actual name of the file.

*Example:*

[File Name] ver8.emd

*Keyword:* [File Rev]

*Required:* Yes

*Description:* Tracks the revision level of a particular .ibs file.

*Usage Rules:* Revision level is set at the discretion of the engineer defining the file. The following guidelines are recommended:

0.x silicon and file in development

1.x pre-silicon file data from silicon model only

2.x file correlated to actual silicon measurements

3.x mature product, no more changes likely

*Example:*

[File Rev] 1.0 | Used for .ibs file variations

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters, and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [Interconnect Model Set] represents.

*Usage Rules:* The description shall fit on a single line, and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keywords:* [Date], [Source], [Notes], [Disclaimer], [Copyright]

*Required:* No

*Description:* Optionally clarifies the file.

*Usage Rules:* The keyword arguments can contain blanks, and be of any format. The [Date] keyword argument is limited to a maximum of 40 characters, and the month should be spelled out for clarity.

Because IBIS model writers may consider the information in these keywords essential to users, and sometimes legally required, design automation tools should make this information available. Derivative models should include this text verbatim. Any text following the [Copyright] keyword must be included, verbatim, in any derivative models.

*Examples:*

[Date] July 4, 2018 | The latest file revision date

|

[Source] Put originator and the source of information here. For

example:

From silicon level SPICE model at NoName.

From lab measurement.

Compiled from manufacturer's data book, etc.

|

[Notes] Use this section for any special notes related to the file.

|

[Disclaimer] This information is for modeling purposes only, and is not

guaranteed. | May vary by component

|

[Copyright] Copyright 2018, XYZ Corp., All Rights Reserved

*Keyword:* [Module]

*Required:* Yes

*Description:* Marks the beginning of an Electrical Module Description.

*Usage Rules:* The keyword is followed by the name of the module level component. The length of the component name must not exceed 40 characters in length, and blank characters are allowed. There must be a matching [Module] keyword.

*Example:*

[Module] 16X8\_SIMM

*Keyword:* [Number Of Pins]

*Required:* Yes

*Description:* Tells the parser the number of pins to expect. Pins are any externally accessible electrical connection to the component.

*Usage Rules:* The field must be a positive decimal integer. The [Number Of Pins] keyword must be positioned before the [Pin List] keyword.

*Example:*

[Number Of Pins] 128

*Keyword:* [Pins]

*Required:* Yes

*Description:* Tells the parser the pin names of the user accessible pins. It also informs the parser which pins are connected to power and ground.

*Sub-Params:* signal\_name, model\_type

*Usage Rules:* Following the [Pins] keyword are three columns. The first column lists the pin name (in data book this can also be called pin number). The second column lists the data book name of the signal connected to that pin. The third column is one of the following model\_types:

I/O This pin is connected to IBIS I/O buffer pads

POWER This pin is connected to a power signal

GROUND This pin is connected to a ground signal

NC This pin is not connected to any signal

There must be as many pin\_name/signal\_name rows as there are pins given by the preceding [Number Of Pins] keyword. Pin names must be the alphanumeric external pin names of the part. The pin names cannot exceed eight characters in length. ~~Any pin associated with a signal name that begins with “GND” or “POWER” will be interpreted as connecting to the modules ground or power plane.~~ In addition, NC is a legal signal name and indicates that the Pin is a “no connect”. As per the IBIS standard “GND,” “POWER,” and “NC” are case insensitive.

*Example:*

| A SIMM Module Example:

|

[Module] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of Pins] 128

[Pin] signal\_name signal\_type

A1 GND GROUND

A2 DQ1 I/O

A3 DQ2 I/O

A4 POWER5 POWER | This pin connects to 5 V

A5 NC NC

A6 POWER3.3 POWER | This pin connects to 3.3 V

*Keyword:* [Interconnect Model Group]

*Required:* Yes

*Description:*  [Interconnect Model Group] has a single argument, which is the name of the associated Interconnect Model Group. The length of the Interconnect Model Group name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Group]/[End Interconnect Model Group] keyword pair is hierarchically scoped by the **[**Module**~~]~~** keyword. The [Interconnect Model Group] keyword is used to define a list of [Interconnect Model Set]s by name that shall be used together to define Interconnect Models to be used in a simulation. A simulation may contain Interconnect Models from the Interconnect Model Sets listed in only one Group.

*Usage Rules:* [Module] must contain one or more [Interconnect Model Group] keywords (identified by a name). Each [Interconnect Model Group] must contain at least one [Interconnect Model Set] name. Interconnect Model Sets contain Interconnect Models used to describe pin, or IBIS component connections to IBIS-ISS subcircuits or Touchstone files.

Interconnect Model Sets that exist for the module shall be listed in one or more Interconnect Model Groups. An Interconnect Model Group is required even if it references only one Interconnect Model Set.

The section under the [Interconnect Model Group] keyword shall have two entries per line, with each line identifying one Interconnect Model Set associated with the module. The entries shall be separated by at least one white space. The first entry lists the Interconnect Model Set name (up to 40 characters long). The second entry is the file reference of the file containing the Interconnect Model Set and shall have the extension “ims”. This file reference shall conform to the rules given in Section 3, ‘GENERAL SYNTAX RULES AND GUIDELINES’. If the Interconnect Model Set is in the same IBIS file as [Begin Module Description], then the second entry shall be “NA”.

The files containing the Interconnect Model Sets with the ims extension shall be located in the same directory as the .ibs file or in a specified directory under the .ibs file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’ (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs file is permitted). An [Interconnect Model Set] with matching name shall be found in the stated location for each Interconnect Model Set named in the [Interconnect Model Group].

Each Interconnect Model Set name and its file\_reference may only appear once under each [Interconnect Model Group] keyword for a given component.

As discussed in Section XXX, two interface locations exist: module pin, component Pin. These interfaces are identified in the terminal lines under the [Interconnect Model] keyword and by their Terminal\_type column entries (shown in Table 41) as follows:

pin: Pin\_I/O, Pin\_Rail, A\_gnd

A\_gnd is the simulator global reference node of the Interconnect Model.

Identifiers associated with these Termimal\_type \*\_I/Os are pin\_name entries. Module pin\_names chall be the pin name in the Module [Pins] section. Component pin\_names shall be the component pin\_name preceded by the references designator of the component with a “.” Inserted between the reference designator and the pin\_name (e.g. U2.DQ1). In addition, some \*\_I/O terminals may have the optional Aggressor\_Only column. If any \*\_I/O pin is marked as Aggressor\_Only. Any \*\_I/O Terminal\_type without the Aggressor\_Only column may be considered as an aggressor or a victim.

The remaining terminals are used for POWER or GND and are referred to as “rails”. The rail identifiers are pin\_name and signal\_name. The component rail identifier signal\_name shall be the signal\_name defined within the IBIS Component.

An Interconnect Model Group contains of a list of Interconnect Model Sets which in turn contains a list of Interconnect Models. There are a number of rules that apply to this combined list of Interconnect Models in an Interconnect Model Group.

* I/O pin\_name rules
  + I/O terminals use pin\_name identifiers
  + All \*\_I/O pin\_names may omit the Aggressor\_Only column (may be aggressors or victims)
  + No I/O pin\_name in a component may appear as a Pin\_I/O terminal without the Aggressor\_Only column in more than one Interconnect Model in the Interconnect Model Group.
  + No I/O pin\_name in a component may appear as a Buffer\_I/O terminal without the Aggressor\_Only column in more than one Interconnect Model in the Interconnect Model Group.
* General description of rail terminals
  + At the pin interface, a terminal whose Terminal\_type is Pin\_Rail can be identified by a pin\_name, signal\_name. A pin\_name maps directly into a Pin\_Rail pin\_name.
    - Note that a terminal whose Terminal\_type is Pin\_Rail may be associated with one pin\_name or a list of pin\_names on a rail that is associated with a signal\_name. If the terminal is associated with more than one pin\_name then these pin\_names are shorted together.
  + At the component pin interface, a terminal whose Terminal\_type is Pin\_Rail can be identified by a pin\_name, signal\_name. A pin\_name maps directly into a Pin\_Rail pin\_name.
    - Note that a terminal whose Terminal\_type is Pin\_Rail may be associated with one pin\_name or a list of pin\_names on a rail that is associated with a signal\_name. If the terminal is associated with more than one pin\_name then these pin\_names are shorted together.
  + A Power Delivery Network (PDN) has one or more connections of rail terminals between Pins and Components Pins.
  + An Interconnect Model with only rail terminals and two interfaces (no I/O terminals) can be used for a PDN.
  + An Interconnect Model with only rail terminals (no I/O terminals) and only one interface is permitted for applications such as for modeling rail decoupling circuits.
  + A PDN structure can also exist in an Interconnect Model with I/O terminals.
  + Also, rail terminals or A\_gnd can be used in Interconnect Models to provide a reference node for the electrical interconnections associated with \*\_I/O terminals.
* Rail terminal rules
  + At the pin interface, a rail pin\_name may appear on a terminal line whose Terminal\_type is Pin\_Rail in multiple Interconnect Models in the Interconnect Model Group.
  + A rail terminal may be in Interconnect Models with any combination of Pins and Component Pins.

Note that these rules apply to the complete list of Interconnect Models that are included in each Interconnect Model Group, regardless of which Interconnect Model Sets contain the Interconnect Models.

All Interconnect Models without I/O terminals, but with only rail terminals are available for simulations.

*Examples:*

| Some [Interconnect Model Set] names used in Examples from Section 12 are

| referenced below:

|

| Example 1

|

[Interconnect Model Group] Full\_ISS\_PDN\_1

| Interconnect Model Set file\_reference

Full\_ISS\_PDN\_1 NA | The [Interconnect Model Set] is

| present in the .ibs file for

| all pins

[End Interconnect Model Group]

|

| Example 2

|

[Interconnect Model Group] Full\_ISS\_PDN\_sn\_2

| Interconnect Model Set file\_reference

Full\_ISS\_PDN\_sn\_2 NA | The [Interconnect Model Set] is

| present in the .ibs file for

| all I/O pins and PDN described

| by signal\_names (sn)

[End Interconnect Model Group]

|

*Keyword:* [**End Interconnect Model Group**]

*Required:* Yes, for each instance of the [Interconnect Model Group] keyword

*Description:* Indicates the end of the data for one [Interconnect Model Group].

*Example:*

[End Interconnect Model Group]

*Keyword:* [Interconnect Model Set]

*Required:* No

*Description:* Used to contain Interconnect Models

*Usage Rules:* [Interconnect Model Set] has a single argument, which is the name of the Interconnect Model Set. The length of the Interconnect Model Set name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Set]/[End Interconnect Model Set] keyword pair is hierarchically equivalent in scope to [Module].

The section under the [Interconnect Model Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more Interconnect Models. See the section [Interconnect Model] for a description of the content of each Interconnect Model.

An [Interconnect Model Set] contains a list of [Interconnect Model]s that have a logical association such as:

* All signals in a bus (e.g.. DDR4, or PCIeG3)
* Full PDN structure from module pin to component pin.
* All I/O models between module and component pins.
* I/O models between component pins.
* Coupled models
* Touchstone electrical models
* Decoupling capacitor models
* IBIS-ISS electrical models

*Example:*

[Interconnect Model Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O buffer

[Interconnect Model] DQ1

…

[End Interconnect Model]

[Interconnect Model] DQ2

…

[End Interconnect Model]

[Interconnect Model] DQS

…

[End Interconnect Model]

[End Interconnect Model Set]

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters, and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [Interconnect Model Set] represents.

*Usage Rules:* The description shall fit on a single line, and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keyword:* [**End Interconnect Model Set**]

*Required:* Yes, for each instance of the [Interconnect Model Set] keyword.

*Description:* Indicates the end of the Interconnect Model Set data.

*Example:*

[End Interconnect Model Set]

**12.2 GENERAL INTERCONNECT SYNTAX REQUIREMENTS**

Terminal lines under the [Interconnect Model] keyword describe connections.

Pin\_name in this context are either the pin\_name in the module [Pins], or reference\_designator.pin for pins that are pins of a component in [Reference Designator Map]

I/O terminals shall be connected using only the pin\_name qualifier:

Rail terminal connections have more options to support direct connections to terminals or to groups of terminals using signal\_name, or pin\_name. The rail terminal can connect to:

* a specific component or module rail pin\_name
* all of the component pins of a rail signal\_name within a component
* all of the module pins of a rail signal\_name

One or more Interconnect Model Sets may be included in a separate Interconnect Model Set file, using a file name with the extension “ims”, or within the .emd file where [Interconnect Model Set Selector] is used. The [Interconnect Model Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [Interconnect Model] keywords and the [Interconnect Model] associated subparameters, as is listed in Table 40.

Table 40 – Interconnect Modeling Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [Interconnect Model Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [Interconnect Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End Interconnect Model] | (note 7) |
| [End Interconnect Model Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [Interconnect Model Set].  Note 2 At least one [Interconnect Model] is required for each [Interconnect Model Set].  Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.  Note 4 This subparameter shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.  Note 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.  Note 6 See text below.  Note 7 Required when the [Interconnect Model] keyword is used  Note 8 Required when the [Interconnect Model Set] keyword is used | |

When Interconnect Model Set definitions occur within a .ibs file, their scope is “local”— they are known only within that .ibs file and no other .ibs file.

Usage Rules for the .ims file:

Interconnect models are stored in a file whose file name uses the format:

<stem>.ims

The <stem> provided shall adhere to the rules given for the [File Name] keyword. Use the “ims” extension to identify files containing Interconnect Models. The .ims file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Begin Module Description] and [Model] keywords are not allowed in the .ims file. The .ims file is for Interconnect Models only.

*Keyword:* [Interconnect Model]

*Required:* Yes

*Description:* Marks the beginning of an Interconnect Model description that is used to define the interfaces to IBIS-ISS subcircuit or Touchstone files.

*Sub-Params:* Unused\_port\_termination, Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically scoped by the [Interconnect Model Set]/[End Interconnect Model Set] keywords.

The [Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Module].

An [Interconnect Model] may contain any combination of component pins and module pins. An Interconnect Modue can have only one of the following combinations:

* Module pins and component pins
* Module pins
* Component pins

An [Interconnect Model] may contain:

* only power rail models
* one or more I/O signal models
* both power rail models and one or more I/O signal models
* module pin rails only
* component pin rails only

Each terminal of an Interconnect Model is connected to a node and has a “voltage”. This, as stated, is imprecise. Voltage, by definition, is a potential difference between two points. It is common to probe and plot the potential difference between simulator nodes at a terminal and a simulator global reference node (e.g., SPICE ideal node “0”), the latter of which is often assumed and/or unstated. This is valid for non-power-aware simulations when the local reference (or return path) node is forced to a global reference by the simulator, or for “ground-referenced” power aware simulations that lump the effects of all rail interconnects together. However, this is not valid when the local reference nodes are “floating”. In this case it is important that the actual reference node for measurements at the I/O buffer is included as a terminal in the Interconnect Model. If this is not done, then the Interconnect Model will not correctly account for all return currents, particularly from capacitive elements. If an Interconnect Model does not contain a reference terminal, then the user of these models should be aware that using these models in power-aware simulations can potentially introduce errors in simulations.

The following subparameters are defined:

Param

File\_IBIS-ISS

File\_TS

Unused\_port\_termination

Number\_of\_terminals = <value>

In addition to these subparameters, the [Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3.2, “SYNTAX RULES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

| into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_reference and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file\_reference for a Touchstone file. The Touchstone file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference

File\_TS typ.s8p

Unused\_port\_termination rules:

The Unused\_port\_termination subparameter is required under this condition:

File\_TS is used and the number of terminal lines (described below) is less than N+1 (where N is the number of ports in the Touchstone file)

Unused\_port\_termination is illegal under these conditions:

File\_IBIS-ISS is used.

File\_TS is used and the number of terminal lines is N+1

If required, only one Unused\_port\_termination subparameter may appear for a given [Interconnect Model] keyword.

The Unused\_port\_termination subparameter is followed by white space and one of these arguments:

Open

Reference

Resistance

“Open” declares that the unused ports remain unterminated (open-circuited).

“Reference” declares that the EDA tool terminates all unused ports with resistors whose resistance values are equal to the reference impedances provided in the Touchstone file for the respective unused ports, and all connected to the model’s reference terminal.

“Resistance” declares that the EDA tool terminates all unused ports with resistors, all having the same value, and all connected to the model’s reference terminal. The “Resistance” entry is followed by a third column entry with the (non-negative) numerical resistance value.

*Examples:*

Unused\_port\_termination Open

Unused\_port\_termination Reference

Unused\_port\_termination Resistance 43.5

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

Only one Number\_of\_terminals subparameter may appear for a given [Interconnect Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given Interconnect Model.

For File\_IBIS-ISS, the Number\_of\_terminals value shall be equal to the number of subcircuit terminals for an IBIS-ISS subcircuit. Because an IBIS-ISS subcircuit requires at least one terminal the Number\_of\_terminals value shall be 1 or greater. The IBIS-ISS subcircuit terminals shall not contain an ideal reference node (SPICE node 0 or its synonyms).

For File\_TS, the Number\_of\_terminals value shall be a value equal to N+1 (where N is the number of ports in the Touchstone file). Because a Touchstone file requires at least one port, the Number\_of\_terminals value shall be 2 or greater.

*Example:*

Number\_of\_terminals = 3

Terminal line rules:

The terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End Interconnect Model] keyword.

Terminal lines are of the following form, with each identifier separated by whitespace:

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

The Terminal\_number is the identifier for a specific terminal. The value shall be 1 or greater and less than or equal to the Number\_of\_terminals. The same Terminal\_number shall not appear more than once for a given Interconnect Model.

For File\_IBIS-ISS, the Terminal\_number entry shall match the IBIS-ISS terminal (node) position. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. Each IBIS-ISS terminal shall have a terminal line entry.

For File\_TS, the Terminal\_number entry shall match the Touchstone file port number or reference terminal line, as shown below. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. The terminal line for Terminal\_number N+1 is required as a reference terminal for each port and shall be connected to a rail terminal or A\_gnd in the Interconnect Model. At least one other terminal line entry is required.

* Terminal\_number Port
* 1                     1
* 2                          2
* …
* N                        N
* N+1 Reference terminal for the Touchstone file

For Touchstone files, each unused port and its corresponding Terminal\_number shall be terminated in simulation with a resistor whose value corresponds to the Unused\_port\_termination subparameter entry. The resistor is connected to the model’s reference terminal.

Terminal\_type  
The Terminal\_type is a string that identifies whether the terminal is a reference, supply or I/O terminal and whether the terminal is connected to a module or component pin. (Note that “I/O” in this context is a synonym for “signal”, as opposed to “supply” or “rail”; it is not intended to imply model type as used in the “Model\_type” subparameter). Furthermore, if the terminal is connected to a buffer supply rail, the Terminal\_type identifies to which specific buffer rail the terminal is connected. The Terminal\_type shall be one of the following:

* Pin\_I/O
* Pin\_Rail

Terminal\_type\_qualifier   
Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, module signal\_name or component signal\_name

Qualifier\_entry   
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

component\_signal\_name <reference\_designator.signal\_name\_entry>

Note that to short all rail pins in [Pin List] with the same signal\_name the reference\_designator shall be bland and the component\_signal\_name will be <.signal\_name\_entry>

A\_gnd

Terminal\_type A\_gnd defines a connection to the simulator global reference node. The A\_gnd node can be used at any interface.

Terminal\_type A\_gnd is not required under File\_TS or File\_IBIS-ISS.

If present under File\_TS, Terminal\_type A\_gnd may be used only once on the N+1th terminal line.

If present under File\_IBIS-ISS, Terminal\_type A\_gnd may be used any number of times on any of the terminal lines.

Terminal\_type\_qualifier   
The Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, module signal\_name or component signal\_name.

Aggressor\_OnlyThe Aggressor\_Only entry is optional and is indicated by the string “Aggressor\_Only” without the quotation marks.

Multi-line Interconnect Models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line Interconnect Model). As a result, while the interconnects at the edges of the Interconnect Model may induce crosstalk onto other interconnects nearby, being on the edge of the Interconnect Model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure.

Connecting Module and Components Pins

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. Terminals may be at module or component pins. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the [Interconnect Model] subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Aggressor\_Only”

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the [Interconnect Model] subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Aggressor\_Only”
* The second column, Terminal\_type is:
  + For I/O connections
    - Terminal\_type must be Pin\_I/O.
    - Terminal\_type\_qualifier shall be pin\_name.
      * Module Pins shall be a pin\_name in the [Pins] list
      * Component Pins shall be in the form:
        + <component reference designator>.< pin\_name in component [Pins] list>.
  + For rail connections
    - Terminal\_type shall be Pin\_Rail
    - Terminal\_type\_qualifier shall be one of the following:
      * Module pin\_name
        + Qualifier\_entry shall be a rail pin\_name in Module [Pins]
      * Module signal\_name
        + Qualifier\_entry shall be a rail signal\_name in Module [Pins]
      * Component pin\_name
        + <component reference designator>.< pin\_name in component [Pins] list>.
      * Component signal\_name
        + <component reference designator>.< signal\_name in component [Pins] list>.

Table 41 summarizes the rules described above.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | | | **Aggressor\_Only** | |
| --- | --- | --- | --- | --- | --- |
| **pin\_name** | **signal\_name** |  |  |
| Pin\_I/O | X |  |  | A |
| Pin\_Rail | Y | Z |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” are POWER and GND names. The letter “A” designates "Aggressor\_Only". The letter Z designates POWER and GND signal names.

Three classes of pins are defined for a component: signal pins, supply pins and no-connect pins. Supply pins have a model\_name of either POWER or GND. No-connect pins have model\_name NC. All other pins are classified as signal pins. Pins are assumed to use the names listed under the first column of the [Pin List] keyword (the pin\_name column).

Pins may be terminals of the Interconnect Model that connect directly to a printed circuit board or other type of system connection to an IBIS component. Pins can be signal pins (Pin\_I/O), or supply pins (Pin\_Rail). An Interconnect Model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the supply pins.
2. By assuming that all supply pins connected to a supply signal\_name are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins that are connected to a specific signal\_name on at least one supply pin.
3. By assuming that all supply pins connected to a supply signal\_name on a specific component are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins on a component that are connected to a specific signal\_name on at least one supply pin.

Any one pin shall not be included in more than one terminal of an Interconnect Model.

*Examples:*

[Module] dimm

[Number of Pins] 9

[Pin] signal\_name signal\_type

A1    DQ1         I/O

A2    DQ2         I/O

A3    DQ3         I/O

D1    DQS+        I/O

D2    DQS-        I/O

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Reference Designator Map]

U1 mem.ibs Memmory

U2 mem.ibs Memmory

[Interconnect Model Group] Just\_One

SomeDQ NA

[End Interconnect Model Group]

[Interconnect Model Set] SomeDQ

[Interconnect Model] DQ1

File\_IBIS-ISS DQ1.iss DQ1

Number\_of\_terminals = 29

1  Pin\_I/O      pin\_name A1

2  Pin\_I/O      pin\_name U1.A1

3  Pin\_I/O      pin\_name U2.A1

4 Pin\_Rail signal\_name VDD

5 Pin\_Rail signal\_name VSS

6 Pin\_Rail signal\_name U1.VDDQ

7 Pin\_Rail signal\_name U1.VSSQ

8 Pin\_Rail signal\_name U2.VDDQ

9 Pin\_Rail signal\_name U2.VSSQ

[End Module]

[End]

*Keyword:* [Reference Designator Map]

*Required:* Yes, if any of the path descriptions use the Node subparameter

*Description:* Maps a reference designator to a component or electrical Module description contained in a .ibs or .emd file.

*Usage Rules:* The [Reference Designator Map] keyword must be followed by a list of all of the reference designators called out by the Node subparameters used in the various path descriptions. Each reference designator is followed by the name of the .ibs or .emd file containing the electrical description of the component or Module, then the name of the component itself as given by the .ibs or .emd file’s [Begin Module Description] or [Begin Module Description] keyword respectively. The reference designator, file name and component name terms are separated by white space. By default the .ibs or .emd files are assumed to exist in the same directory as the calling .emd file. It is legal for a reference designator to point to a component that is contained in the calling .emd file.

The reference designator is limited to ten characters.

*Example:*

[Reference Designator Map]

|

| External Part References:

|

| Ref Des File name Component name

u23 pp100.ibs Processor

u24 simm.emd 16X8\_SIMM

u25 ls244.ibs NoName 74LS244a

u26 r10K.ibs My\_10K\_Pullup

*Keyword:* [End Module]

*Required:* Yes

*Description:* Marks the end of an Electrical Interconnect Description.

*Usage Rules:* This keyword must come at the end of each complete electrical interconnect model description.

Optionally, a comment may be added after the [End Electrical Description] keyword to clarify which Module model has ended.

*Example:*

[End Module Description] | End: 16Meg X 8 SIMM Module

Keyword: [End]

*Required:* Yes

*Description:* Defines the end of the emd file.

*Example:*

[End]