RDIMM Example Figures and Example Syntax for BIRD202

Randy Wolff

Micron Technology

4/17/2020

RDIMM Example Figures

Figure X shows a DDR4 Registered DIMM containing DRAM components labeled by designators U1, U2, U4, U5 (front side) and U7-U11 (back side, not seen) and a Register component labeled by designator U3.

Also shown is pre-register Net A07 connecting from an EMD Pin to a Designator Pin of designator U3 and post-register net BA07 connecting from a Designator Pin of designator U3 to Designator Pins of designators U4, U5, U7, and U8 as well as termination resistor RN13 connecting to the VTT rail.



Figure X

Figure Y, a zoomed in area of Figure X, shows an example of an extended net. The extended net A07 can be modeled two ways:

1. One EMD Model defining only terminals for EMD Pin 211 and Designator Pin U3.W1. The EMD Model contains the complete signal path of net A07, the series resistor R123, and net A07r.
2. One EMD Model or multiple EMD Models contained with an EMD Set that include terminals for EMD Pin 211 and Designator Pin U3.W1 and two terminals for the pins of the series resistor. The resistor would be assigned a designator (R123) referencing an IBIS component.



Figure Y

Figure Z, a zoomed in area of Figure X, shows an example of an internal net. The post-register net BA07 connects from the register’s Designator Pin U3.B11 to the DDR4 DRAMs’ Designator Pins U4.M8, U5.M8, U7.M8, and U8.M8 as well as to one Designator Pin of the termination resistor RN13. RN13 terminates the signal to the VTT rail.



Figure Z

Example Syntax

| EMD Syntax Example 1 (Embedded Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Just\_One

Addr\_07 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07

[EMD Model] A07

File\_IBIS-ISS A07.iss A07

Number\_of\_terminals = 6

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name U3.W1

3 Pin\_Rail bus\_label VDD1

4 Pin\_Rail signal\_name VSS

5 Pin\_Rail bus\_label U3.VDD1

6 Pin\_Rail bus\_label U3.VSS

[End EMD Model]

[EMD Model] BA07

File\_IBIS-ISS A07.iss BA07

Number\_of\_terminals = 16

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail signal\_name VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

| EMD Syntax Example 2 (External Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22OHM

510-501618 resistors.ibs RPACK4\_33OHM

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

|

R123.1 A07

R123.2 A07

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Just\_One

Addr\_07 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07

[EMD Model] A07

File\_IBIS-ISS A07.iss A07

Number\_of\_terminals = 8

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name R123.1

3 Pin\_I/O pin\_name R123.2

4 Pin\_I/O pin\_name U3.W1

5 Pin\_Rail bus\_label VDD1

6 Pin\_Rail signal\_name VSS

7 Pin\_Rail bus\_label U3.VDD1

8 Pin\_Rail signal\_name U3.VSS

[End EMD Model]

[EMD Model] BA07

File\_IBIS-ISS A07.iss BA07

Number\_of\_terminals = 16

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

16 Pin\_I/O pin\_name RN13.7

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail pin\_name RN13.VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

| EMD Syntax Example 3 (External Resistors, Separate A07, A07R, and POWER Models)

| Using DDR4 RDIMM Example

|

[Begin EMD] DDR4\_RDIMM

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22OHM

510-501618 resistors.ibs RPACK4\_33OHM

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07

U3.W3 VSS GND

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

R123.1 A07

R123.2 A07

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Just\_One

Addr\_07 NA

RIGHT\_SIDE\_POWER NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07

[EMD Model] A07

File\_IBIS-ISS A07.iss A07

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name R123.1

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] A07R

File\_IBIS-ISS A07.iss A07R

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name R123.2

2 Pin\_I/O pin\_name U3.W1

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] BA07

File\_IBIS-ISS A07.iss BA07

Number\_of\_terminals = 16

1 Pin\_I/O pin\_name U3.B11

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8

15 Pin\_Rail signal\_name U8.VSS

16 Pin\_I/O pin\_name RN13.7

18 Pin\_Rail pin\_name RN13.VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

[EMD Set] RIGHT\_SIDE\_POWER

[EMD Model] RIGHT\_SIDE\_VDD1\_VTT\_VSS

File\_IBIS-ISS rdimm\_power.iss RIGHT\_SIDE\_VDD1\_VTT\_VSS

Number\_of\_terminals = 8

1 Pin\_Rail bus\_label VDD1

2 Pin\_Rail signal\_name VSS

3 Pin\_Rail signal\_name VTT

4 Pin\_Rail bus\_label U3.VDD1

5 Pin\_Rail signal\_name U3.VSS

6 Pin\_Rail bus\_label U4.VDD1

7 Pin\_Rail signal\_name U4.VSS

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_Rail bus\_label U7.VDD1

11 Pin\_Rail signal\_name U7.VSS

12 Pin\_Rail bus\_label U8.VDD1

13 Pin\_Rail signal\_name U8.VSS

14 Pin\_Rail signal\_name RN13.VTT

[End EMD Model]

[End EMD Set]