Illustrating the need to support pin grouping in the port mapping syntax

Prepared for the IBIS Interconnect Task Group discussions on port mapping

Arpad Muranyi
Siemens EDA

August 30, 2023

- **To simplify the discussion, let's consider first only the VDD ports of a Touchstone file that will be used in an EMD model (.emd file) of a multi-chip device**
- **The [EMD Pin List] keyword has to contain all of the VDD pins on the footprint side of the device**
- **The [Designator Pin List] keyword has to contain all of the VDD pins (pads) found in each IBIS die (designator) model (.ibs file)**
  - **these pin names must match the pin names in the [Pin] keyword of the .ibs file(s)**
  - **the** `signal_name` **in the [Pin] keyword is meaningless in the EMD file**
- **Once the list of EMD and Designator pins are available, they can be associated with the ports of the Touchstone file(s) using** `Pin_Rail, Buffer_Rail, signal_name, bus_label,` **etc.**
- **But, regardless of whether we generate the EMD file manually or with a script, the EMD and Designator pin name lists have to come from somewhere**
  - **the port map is a good place for this information**
  - **however, associating ports with multiple pins requires a pin grouping syntax**

Excerpts from the EMD file

```
[Number Of EMD Pins]  200
[EMD Pin List]  signal_name  signal_type  bus_label
…
A3              VDD              POWER
A4              VDD              POWER
A7              VDD              POWER
AB5             VDD              POWER
AB9             VDD              POWER
AB11            VDD              POWER
AB13            VDD              POWER
AC7             VDD              POWER
B1              VDD              POWER
B5              VDD              POWER
B9              VDD              POWER
B11             VDD              POWER
B13             VDD              POWER
C3              VDD              POWER
…
```

```
[Designator Pin List]  signal_name  signal_type  bus_label
…
U1.4            VDD              POWER
U1.8            VDD              POWER
U1.17           VDD              POWER
U1.20           VDD              POWER
U1.33           VDD              POWER
U1.36           VDD              POWER
U1.40           VDD              POWER
U1.45           VDD              POWER
U1.49           VDD              POWER
U1.52           VDD              POWER
U1.57           VDD              POWER
U1.62           VDD              POWER
U1.65           VDD              POWER
U1.67           VDD              POWER
…
```

```
[EMD Model]                EMDmodel1
File_TS                    ModelFiles/TSfileName.s169p
Number_of_terminals = 170
...
163     Pin_Rail    signal_name    U1.VDD
164     Pin_Rail    signal_name    U2.VDD
165     Pin_Rail    signal_name    U3.VDD
166     Pin_Rail    signal_name    U4.VDD
167     Pin_Rail    signal_name    U5.VDD
168     Pin_Rail    signal_name    VDD
169     Pin_Rail    signal_name    VTT
170     Pin_Rail    signal_name    Ref
[End EMD Model]
```

A proposed port mapping syntax that supports pin grouping

```
! HL_PORTMAP 1.0
! PORT 1    +(PIN U1.94,  A0, S)      -(GROUP:GND.U1,  GND, P)
! PORT 2    +(PIN U2.94,  A0, S)      -(GROUP:GND.U2,  GND, P)
! PORT 3    +(PIN U3.94,  A0, S)      -(GROUP:GND.U3,  GND, P)
! PORT 6    +(PIN BGA.K2, A0, S)      -(GROUP:GND.BGA, GND, P)
! ...
! PORT 7    +(PIN U1.95,  A1, S)      -(GROUP:GND.U1,  GND, P)
! PORT 8    +(PIN U2.95,  A1, S)      -(GROUP:GND.U2,  GND, P)
! PORT 9    +(PIN U3.95,  A1, S)      -(GROUP:GND.U3,  GND, P)
! PORT 12   +(PIN BGA.J2, A1, S)      -(GROUP:GND.BGA, GND, P)
! ...
! PORT 163  +(GROUP:VDD.U1,  VDD, P)  -(GROUP:GND.U1,  GND, P)
! PORT 164  +(GROUP:VDD.U2,  VDD, P)  -(GROUP:GND.U2,  GND, P)
! PORT 165  +(GROUP:VDD.U3,  VDD, P)  -(GROUP:GND.U3,  GND, P)
! PORT 168  +(GROUP:VDD.BGA, VDD, P)  -(GROUP:GND.BGA, GND, P)
! ...
! GROUP PORT   1 NAME:GND.U1,   U1.2,   U1.11,  U1.15,  U1.23,  U1.38,  U1.42,  U1.43,  U1.47,  U1.50,  U1.54,  U1.55,  U1.59,  U1.60,  U1.64...
! GROUP PORT   2 NAME:GND.U2,   U2.2,   U2.11,  U2.15,  U2.23,  U2.38,  U2.42,  U2.43,  U2.47,  U2.50,  U2.54,  U2.55,  U2.59,  U2.60,  U2.64...
! GROUP PORT   3 NAME:GND.U3,   U3.2,   U3.11,  U3.15,  U3.23,  U3.38,  U3.42,  U3.43,  U3.47,  U3.50,  U3.54,  U3.55,  U3.59,  U3.60,  U3.64...
! GROUP PORT   6 NAME:GND.BGA,  BGA.A5, BGA.A9, BGA.A11, BGA.A14, BGA.AA5, BGA.AA13, BGA.AC5,  BGA.AC9, BGA.AC11, BGA.AC14, BGA.B2, BGA.C1,  BGA.C4,  BGA.C5...
! ...
! GROUP PORT   7 NAME:GND.U1,   U1.2,   U1.11,  U1.15,  U1.23,  U1.38,  U1.42,  U1.43,  U1.47,  U1.50,  U1.54,  U1.55,  U1.59,  U1.60,  U1.64...
! GROUP PORT   8 NAME:GND.U2,   U2.2,   U2.11,  U2.15,  U2.23,  U2.38,  U2.42,  U2.43,  U2.47,  U2.50,  U2.54,  U2.55,  U2.59,  U2.60,  U2.64...
! GROUP PORT   9 NAME:GND.U3,   U3.2,   U3.11,  U3.15,  U3.23,  U3.38,  U3.42,  U3.43,  U3.47,  U3.50,  U3.54,  U3.55,  U3.59,  U3.60,  U3.64...
! GROUP PORT  12 NAME:GND.BGA,  BGA.A5, BGA.A9, BGA.A11, BGA.A14, BGA.AA5, BGA.AA13, BGA.AC5,  BGA.AC9, BGA.AC11, BGA.AC14, BGA.B2, BGA.C1,  BGA.C4,  BGA.C5...
! ...
! GROUP PORT 163 NAME:VDD.U1,  U1.4,   U1.8,   U1.17,  U1.20,  U1.33,  U1.36,  U1.40,  U1.45,  U1.49,  U1.52,  U1.57,  U1.62,  U1.65,  U1.67...
! GROUP PORT 163 NAME:GND.U1,  U1.2,   U1.11,  U1.15,  U1.23,  U1.38,  U1.42,  U1.43,  U1.47,  U1.50,  U1.54,  U1.55,  U1.59,  U1.60,  U1.64...
! GROUP PORT 164 NAME:VDD.U2,  U2.4,   U2.8,   U2.17,  U2.20,  U2.33,  U2.36,  U2.40,  U2.45,  U2.49,  U2.52,  U2.57,  U2.62,  U2.65,  U2.67...
! GROUP PORT 164 NAME:GND.U2,  U2.2,   U2.11,  U2.15,  U2.23,  U2.38,  U2.42,  U2.43,  U2.47,  U2.50,  U2.54,  U2.55,  U2.59,  U2.60,  U2.64...
! GROUP PORT 165 NAME:VDD.U3,  U3.4,   U3.8,   U3.17,  U3.20,  U3.33,  U3.36,  U3.40,  U3.45,  U3.49,  U3.52,  U3.57,  U3.62,  U3.65,  U3.67...
! GROUP PORT 165 NAME:GND.U3,  U3.2,   U3.11,  U3.15,  U3.23,  U3.38,  U3.42,  U3.43,  U3.47,  U3.50,  U3.54,  U3.55,  U3.59,  U3.60,  U3.64...
! GROUP PORT 168 NAME:VDD.BGA, BGA.A3, BGA.A4, BGA.A7,  BGA.AB5, BGA.AB9, BGA.AB11, BGA.AB13, BGA.AC7, BGA.B1,  BGA.B5,  BGA.B9, BGA.B11, BGA.B13, BGA.C3...
! GROUP PORT 168 NAME:GND.BGA, BGA.A5, BGA.A9, BGA.A11, BGA.A14, BGA.AA5, BGA.AA13, BGA.AC5,  BGA.AC9, BGA.AC11, BGA.AC14, BGA.B2, BGA.C1,  BGA.C4,  BGA.C5...
! END_HL_PORTMAP
```

Note that each of these four ports are associated with multiple EMD and Designator pins

Note that the list of pins in the green boxes may be different for each Designator device

How can we achieve this without a pin grouping syntax?

The situation is very similar for the VSS pins as well, but the discussion can get complicated (and easily derailed) by the additional complications involving the “referencing problem”

For that reason, I am not addressing the VSS side of things just yet

Let’s first agree on whether the proposed port mapping needs to support a pin grouping syntax