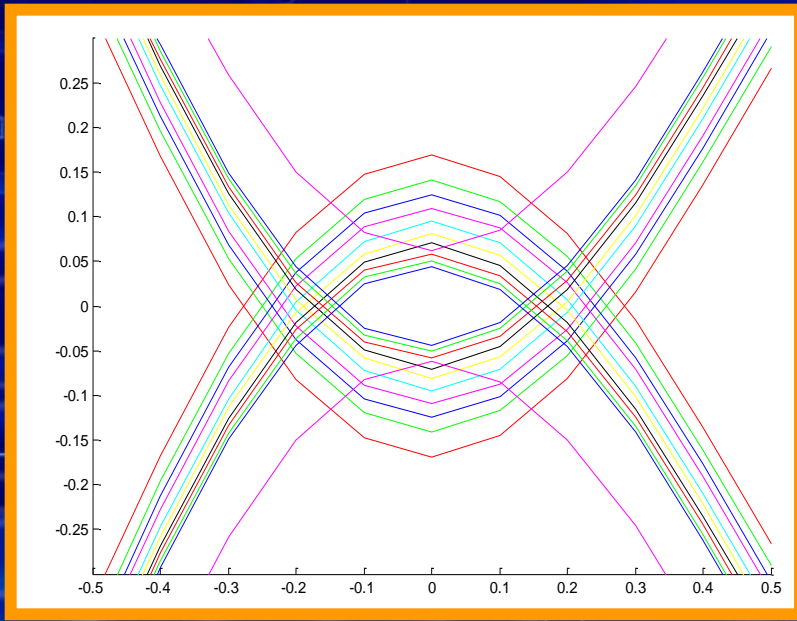


Comparison of the Recent Analog Modeling BIRD Proposals

***IBIS Summit, DAC,
June 7, 2011
San Diego, CA***



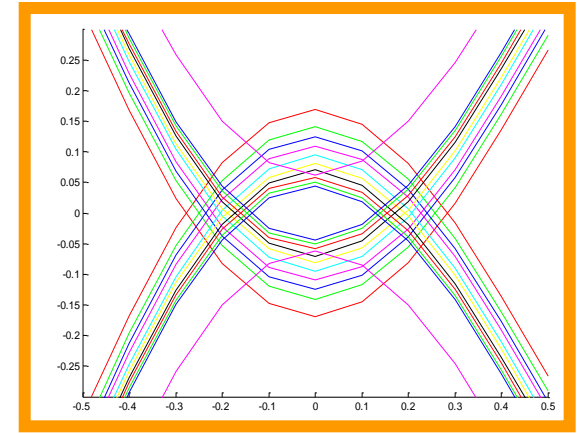
Arpad Muranyi

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Comparison of the Recent Analog Modeling BIRD Proposals

IBIS Summit, DAC,
June 7, 2011
San Diego, CA



1. Addendum to my DesignCon 2011 presentation
2. Overview of Mentor's analog modeling proposals
3. Examples for the Mentor proposals
4. Overview of SiSoft's analog modeling proposals
5. Call to action



Addendum to my DesignCon 2011 presentation

“IBIS-AMI Analog Modeling and Much Needed Improvements for IBIS”

<http://www.eda.org/ibis/summits/feb11/muranyi2.pdf>

- **The above presentation explained the concepts described in my analog modeling BIRDs with examples**
 - **BIRD 116, 117, 118, 125, (129)**
- **The proposals are based on IBIS-ISS and address the shortcomings of legacy IBIS models as well as the needs of the new analog modeling directions emerging with AMI models**
- **The last example showed a complete implementation of Figure 12 (pg. 136) from the IBIS 5.0 specification**
 - **forgot to explain how the supply nodes of [Model] or [External Model] can be connected to specific pins through a package model**



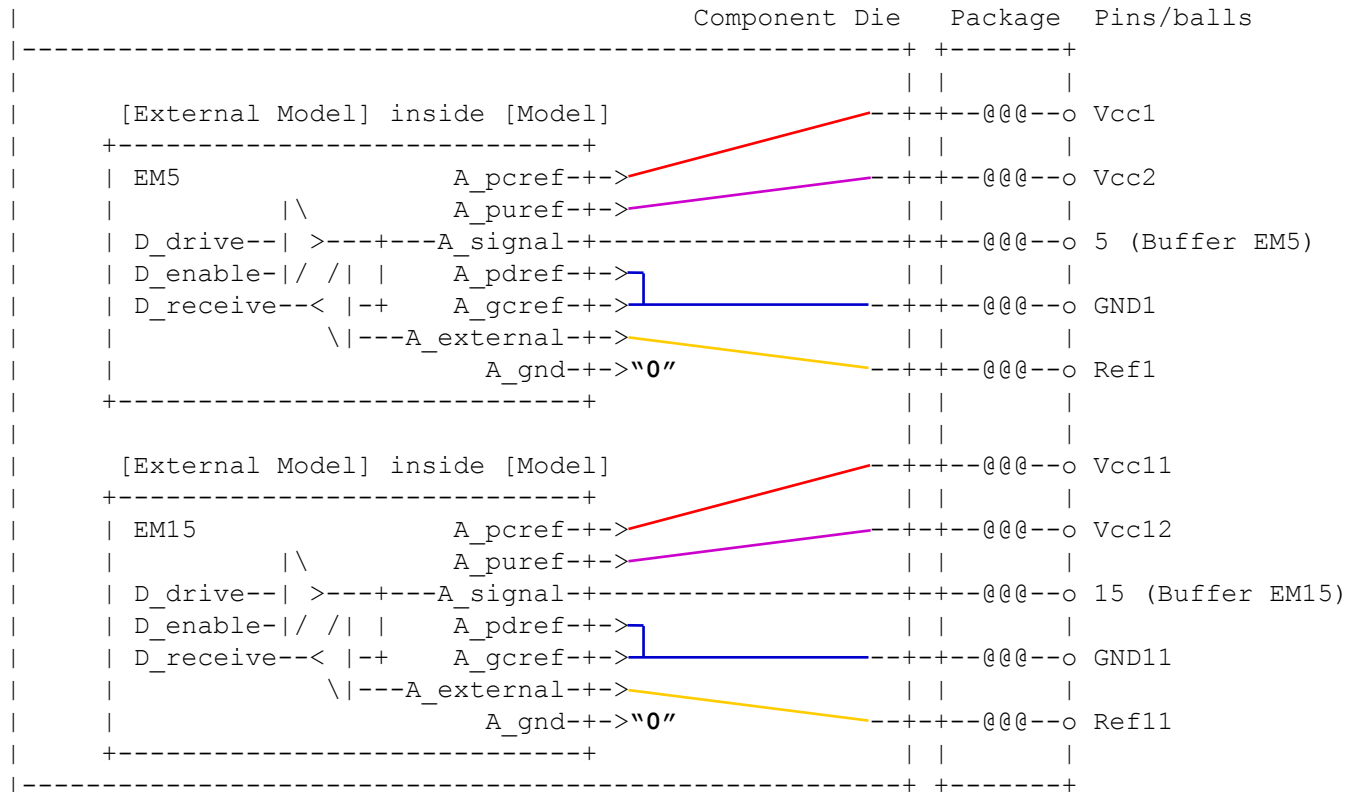
Figure 12 (pg. 136) in IBIS v5.0

	Component	Die	Package	Pins/balls
[External Circuit]	[External Circuit]			
A	A_mypcr	vcc	10	Vcc
	A_mypur	vcc	10	Vcc
D_drive	A_mysig	io1	1	Buffer A
D_enable	A_mypdr	vssa1		
D_receive	A_mygcr	vssa2		
		gnd	11	GND
		Die Interconnect		
[External Circuit]				
B	A_mypur	vccb1		Self Adj
D_drive	A_mysig	o2	2	Justing Buffer
	A_mypdr	vssb1		
	A_mycnt			
	Analog Buffer Control			
		pad_2b		
[External Circuit]				
C	A_mypcr			
	A_mypur			
nd1	A_mysig		3	Buffer C
D_enable	A_mypdr			
D_receive	A_mygcr			
[External Circuit]				
D	A_mypcr			
nd1	A_mysig		4a	Clocka
D_receive	A_mygcr		4b	Clockb
[External Model] inside [Model]				
E	A_pcref			?
	A_puref			?
D_drive	A_pdref			?
D_enable	A_gcref			?
D_receive	A_external			?
	A_gnd			

Figure 12: Reference example for [Node Declarations] keyword



Modified Fig. 12 to illustrate supply connections



How can we tell the simulator how the supply connections of [Model] or [External Model] are made to specific supply die pads so that package parasitics for supply pins can also be included in simulations?

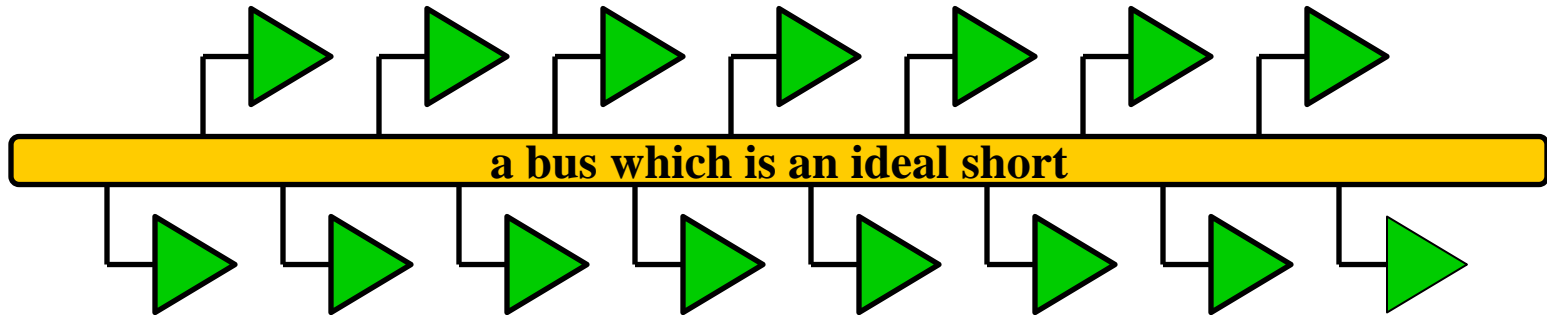


Use [Pin Mapping] to declare supply die pads

```
[Pin]  signal_name  model_name  R_pin  L_pin  C_pin
|
Vcc1   Supply1     POWER
Vcc2   Supply2     POWER
Vcc11  Supply11    POWER
Vcc12  Supply12    POWER
GND1   Ground1     GND
GND11  Ground11   GND
Ref1   Reference1  POWER
Ref11  Reference11 POWER
|
5      Data5      EM5
15     Data15     EM15
|
|
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
Vcc1         NC                PCref_EM5
Vcc2         NC                PUref_EM5
Vcc11        NC                PCref_EM15
Vcc12        NC                PUref_EM15
GND1         Ground_EM5       NC
GND11        Ground_EM15     NC
Ref1         NC                EXref_EM5
Ref11        NC                EXref_EM15
|
5            Ground_EM5       PUref_EM5  Ground_EM5  PCref_EM5  EXref_EM5
15           Ground_EM15     PUref_EM15 Ground_EM15  PCref_EM15 EXref_EM15
```

These are called “bus names” by the specification, and are defined to be ideal shorts. Functionally they are the same thing as “die nodes”.

If a bus is an ideal short, it is a node



Since the “bus” is an ideal short, each receiver sees exactly the same signal

An ideal short “bus” = “node”, correct?

The number of connections we make to the “bus” doesn’t make a difference, if it is ideal, it is still just a “node”...



[Pin Mapping] = [Node Declarations] + Netlisting

- **The [Pin Mapping] keyword serves three functions**
 - declares die nodes (ideal short die buses)
 - associates (i. e. connects) die nodes with the reserved analog supply node names of [Model] or [External Model]
 - A_pdref, A_gdref, A_gcref, A_pceref, A_extref
 - signal nodes are NOT included
 - associates the named die nodes (pads) with pin names
 - eliminates the need for implicit die pad names (derived from pin names)
- **This provides a mechanism to connect the supply nodes of [Model] and [External Model] through an accurate package model (IBIS-ISS) to specific pins**
 - multiple pin to single pad *is* possible (with the 5.0 syntax)
 - multiple pad to single pin *not* possible (with the 5.0 syntax)
- **This works with the existing features of IBIS 5.0!**
 - slight modifications to [Pin Mapping] could provide more capabilities in the future, such as on die interconnect modeling



Using the BIRD 125 concepts for this example

Legacy IBIS file:

```

-----
| Example of an IBIS model using an IBIS-ISS package model.
|-----
Vcc1 Supply1 POWER
Vcc2 Supply2 POWER
Vcc11 Supply11 POWER
Vcc12 Supply12 POWER
GND1 Ground1 GND
GND11 Ground11 GND
Ref1 Reference1 POWER
Ref11 Reference11 POWER
|
5 Data5 EM5
15 Data15 EM15

[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
Vcc1 NC PCref_EM5
Vcc2 NC PUref_EM5
Vcc11 NC PCref_EM15
Vcc12 NC PUIref_EM15
GND1 Ground_EM5 NC
GND11 Ground_EM15 NC
Ref1 NC EXref_EM5
Ref11 NC EXref_EM15
|
5 Ground_EM5 PUref_EM5 Ground_EM5 PCref_EM5 EXref_EM5
15 Ground_EM15 PUIref_EM15 Ground_EM15 PCref_EM15 EXref_EM15
|
[Package Model] QS-SMT-cer-10-pin-pkgs
|...
    
```

IBIS .pkg file:

```

-----
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-----
[Define Package Model] QS-SMT-cer-10-pin-pkgs
[Manufacturer] Quality Semiconductors Ltd.
[OEM] Acme Package Co.
[Description] 10-Pin ceramic SMT package
[Number Of Pins] 10

[Pin Numbers]
Vcc1 DiePort = PCref_EM5
Vcc2 DiePort = PUIref_EM5
Vcc11 DiePort = PCref_EM15
Vcc12 DiePort = PUIref_EM15
GND1 DiePort = Ground_EM5
GND11 DiePort = Ground_EM15
Ref1 DiePort = EXref_EM5
Ref11 DiePort = EXref_EM15
|
5 DiePort = IDP_5
15 DiePort = IDP_15

[Package Circuit]
Language IBIS-ISS

| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ PackageModel.spi S_pkg

| Parameters List of parameters
Parameters TSFile = "My_TstoneFile.s20p"

| Ports are in same order as defined in SPIOB
Ports Vcc1 Vcc2 Vcc11 Vcc12
Ports PCref_EM5 PUIref_EM5 PCref_EM15 PUIref_EM15
Ports GND1 GND11 Ref1 Ref11
Ports Ground_EM5 Ground_M15 EXref_EM5 EXref_EM15
Ports 5 15
Ports IDP_5 IDP_15

|[End Package Circuit]
|[End Package Model]
    
```

IBIS-ISS subcircuit:

```

*****
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8 P9 P10
+ P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ TSFile="TouchstoneFileName.s20p"
Sdriver P1 P2 P3 P4 P5 P6 P7 P8 P9 P10
+ P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
*****
.ends
    
```

Explicit die ports (red) are declared under [Pin Mapping]

Implicit die ports (blue) are declared here

Matched by name

Matched by position

Matched by name



Only a slight modification is needed in BIRD 125

- **This works with the existing [Pin Mapping] keyword of IBIS 5.0**
- **BIRD 125 needs a slight modification to include the “bus names” declared in [Pin Mapping] for this purpose:**

```
|*           DiePort This subparameter declares the name of the connection
|*           point for use within [Define Package Model] at which
|*           the package is connected to the die. The subparameter
|*           must be followed by an equal sign ("=") and the name
|**          of a node or bus that was previously declared by the
|**          [Node Declarations] or the [Pin Mapping] keywords in the
|*           .ibs file, or a reserved word "IDiePort_" immediately
|*           followed by the pin name that precedes this reserved word.
```



Overview of Mentor's analog modeling proposals



Overview of the Mentor analog BIRD drafts

- **BIRD 116: Add IBIS-ISS to [External Model] and [External Circuit] as a Supported Language**
- **BIRD 117: Parameterize A_to_D and D_to_A Converters**
 - allows parameters in .ami files to define their amplitude and edge rate
- **BIRD 118: Analog Parameter Assignments**
 - allows values to be assigned to [External ***] parameters
 - for [External Model] we can use parameters from .ami files
- **BIRD 125: Make IBIS-ISS Available for Package Modeling**
 - no changes in the .ibs file
 - one new keyword [Package Circuit] under [Define Package Modeling], following the style of the existing [External Circuit]
- **BIRD 129: Add “Polarity” Argument to D_to_A Converters**
 - simplifies the content of IBIS-ISS buffer models and the construction of differential buffer stimulus parameters in .ami files



Summary of the Mentor analog BIRD drafts

- **These BIRDs provide solutions for the analog buffer and package modeling problems for legacy and AMI models**
- **Analog modeling remains in the .ibs file**
 - **but parameters can be supplied to them in .ami files**
- **The concepts and syntax are well documented, the BIRDs are in a “finished” condition, ready to be voted on**
 - **this is not to say that we can’t make any changes if we receive useful suggestions and feedback**
- **The concepts do not require substantial changes in the existing IBIS specification**



What the Mentor BIRDs cannot do

- The buffer BIRDs did not define IBISfile(ParName)
 - good idea, can be added easily
- BIRD 125 currently associates the pin names under the .ibs [Pin] and .pkg [Pin Numbers] keywords by name
 - this doesn't allow for shifting around a package model along the pins in the .ibs [Pin] keyword
 - we can consider to modify BIRD 125 to add this capability to it, but is this really useful in practice?

```
[Pin] signal_name  model_name
|
1  Channel_1P  ISS_Diff_Tx
2  Channel_1N  ISS_Diff_Tx
3  ground1     GND
4  Channel_2P  ISS_Diff_Tx
5  Channel_2N  ISS_Diff_Tx
6  ground2     GND
7  supply1     POWER
8  ground3     GND
9  Channel_3P  ISS_Diff_Tx
10 Channel_3N  ISS_Diff_Tx
11 Channel_4P  ISS_Diff_Tx
12 Channel_4N  ISS_Diff_Tx
13 ground4     GND
14 supply2     POWER
15 ground5     GND
16 Channel_5P  ISS_Diff_Tx
17 Channel_5N  ISS_Diff_Tx
18 ground6     GND
19 Channel_6P  ISS_Diff_Tx
20 Channel_6N  ISS_Diff_Tx
```

How would you slide an 8-port S-parameter file with two differential signal pairs along this pin list automatically?

or

How would you slide an 8-port S-parameter file with one differential signal pair with power and GND along this pin list automatically?



Examples for Mentor's analog modeling proposals



S-parameter Tx model with [External Model] & IBIS-ISS

Legacy IBIS file:

```
-----  
| Example of an analog AMI Tx model using [External Model] and  
| an IBIS-ISS S-parameter:  
-----  
[Model] ISS_Diff_Tx  
Model_type Output_diff  
Rref_diff = 100  
|  
[Voltage Range] 1.0 NA NA  
|  
[Ramp]  
dV/dt_r 0.6/40p NA NA  
dV/dt_f 0.6/40p NA NA  
|  
[External Model]  
Language ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ AMIdriver.cir AMI_Sdrv  
|  
| List of parameters  
Parameters TSFile = AMIfile(Tstonefile)  
|  
| List of converter parameters  
Converter_Parameters VloP = AMIfile(Vol)  
Converter_Parameters VhiP = AMIfile(Voh)  
Converter_Parameters VloN = AMIfile(Voh)  
Converter_Parameters VhiN = AMIfile(Vol)  
Converter_Parameters Tfa = AMIfile(Trf)  
Converter_Parameters Tri = AMIfile(Trf)  
|  
| Ports List of port names (in same order as in SPICE)  
Ports A_signal_pos A_signal_neg my_driveP my_driveN A_gnd  
|  
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name  
D_to_A D_drive my_driveP my_ref VloP VhiP Tfa Tri Typ  
D_to_A D_drive my_driveN my_ref VloN VhiN Tfa Tri Typ  
|  
[End External Model]  
|  
[Algorithmic Model]  
Executable Windows_VisualStudio_32 MentorTx.dll MentorTx.ami  
[End Algorithmic Model]
```

EDA tool GUI lets user select "one of many".
Dependency Table may also affect what this GUI does.

Tx.ami file:

```
(Tstonefile (Usage Info) (Type String)  
(Corner "NC.s4p" "WC.s4p" "BC.s4p")  
(Description "Driver on-die S-parameter file")  
)  
(Voh (Usage Info) (Value 0.9) (Type Float)  
(Description "Output open circuit high voltage")  
)  
(Vol (Usage Info) (Value 0.0) (Type Float)  
(Description "Output open circuit low voltage")  
)  
(Trf (Usage Info) (Value 40e-12) (Type Float)  
(Description "20%-80% output rise time")  
)
```

IBIS-ISS subcircuit:

```
*****  
SUBCKT AMI_Sdrv A_signal_pos A_signal_neg my_driveP my_driveN my_ref  
+ TSFile="TouchstoneFileName.s4p"  
  
Sdriver my_driveP A_signal_pos my_driveN A_signal_neg my_ref  
+ MNAME=TSFile  
+ [FBASE = base_frequency] [FMAX=maximum_frequency]  
  
*****  
.ends
```



RC Rx model with [External Model] & IBIS-ISS

Legacy IBIS file:

```
-----  
| Example of an analog AMI Rx model using [External Model] and  
| an IBIS-ISS circuit:  
-----  
[Model] ISS_Diff_Rx  
Model_type Input_diff  
|  
[Voltage Range] 1.0 NA NA  
|  
[External Model]  
Language ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ AMIreceiver.cir AMI_RCrcv  
|  
| List of parameters  
Parameters Rt_H Rt_L = AMIfile(Rt)  
Parameters Rd = AMIfile(Rd)  
Parameters Cc_H Cc_L = AMIfile(Cc)  
Parameters Cd Vt  
|  
| List of converter parameters  
Converter_Parameters Vlo = -0.05  
Converter_Parameters Vhi = 0.05  
|  
| Ports List of port names (in same order as in SPICE)  
Ports A_signal_pos A_signal_neg my_rcv_H my_rcv_L A_gnd  
|  
| D_to_A d_port port1 port2 vlow vhigh corner_name  
A_to_D D_receive my_rcv_H my_rcv_L Vlo Vhi Typ  
|A_to_D D_receive A_signal_pos A_signal_neg Vlo Vhi Typ  
|  
[End External Model]  
|  
[Algorithmic Model]  
Executable Windows_VisualStudio_32 MentorTx.dll MentorRx.ami  
[End Algorithmic Model]  
|
```

Rx.ami file:

```
(Rt (Usage Info) (Value 47.75) (Type Float)  
 (Description "Single-ended termination resistance")  
)  
(Rd (Usage Info) (Value 99.75) (Type Float)  
 (Description "Differential termination resistance")  
)  
(Cc (Usage Info) (Value 0.5e-12) (Type Float) (Default 0.5e-12)  
 (Description "Input Capacitance")  
)
```

IBIS-ISS subcircuit:

```
*****  
.SUBCKT AMI_RCrcv A_signal_pos A_signal_neg my_rcv_H my_rcv_L my_ref  
+ Rt_H = 1e+6  
+ Rt_L = 1e+6  
+ Rd = 1e+6  
+ Cc_H = 0  
+ Cc_L = 0  
+ Cd = 0  
+ Vt = 0  
  
Cc_H A_signal_pos my_ref C=Cc_H  
Cc_L A_signal_neg my_ref C=Cc_L  
Cd A_signal_pos A_signal_neg C=Cd  
Rt_H A_signal_pos my_vtt R=Rt_H  
Rt_L A_signal_neg my_vtt R=Rt_L  
Rd A_signal_pos A_signal_neg R=Rd  
  
Vvtt my_vtt my_ref DC=Vt  
E_H my_rcv_H my_ref VCVS A_signal_pos my_ref 1  
E_L my_rcv_L my_ref VCVS A_signal_neg my_ref 1  
*****  
.ends
```



A simple package model with IBIS-ISS

Legacy IBIS file:

```
-----  
| Example of an IBIS model using an IBIS-ISS package model  
|-----  
|  
[Pin] signal_name model_name  
1 ... ..  
2 ... ..  
3 ... ..  
4 ... ..  
5 Channel_1P ISS_Diff_Tx  
6 Channel_1N ISS_Diff_Tx  
7 Channel_2P ISS_Diff_Tx  
8 Channel_2N ISS_Diff_Tx  
9 ... ..  
10 ... ..  
|  
[Package Model] A_4_pin_pkg_model  
|...  
|...
```

**Matched
by name**

IBIS .pkg file:

```
-----  
| This example implements a package model using an IBIS-ISS  
| subcircuit.  
|-----  
|  
[Define Package Model] A_4_pin_pkg_model  
[Manufacturer] Noname Company, Inc.  
[OEM] Another Noname Package Company, Inc.  
[Description] 4-pin  
[Number Of Pins] 4  
|  
[Pin Numbers]  
5 DiePort = IDP_5  
6 DiePort = IDP_6  
7 DiePort = IDP_7  
8 DiePort = IDP_8  
|  
[Package Circuit]  
Language IBIS-ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ PackageModel.spi S_pkg  
|  
| Parameters List of parameters  
Parameters TSFile = "My_TstoneFile.s8p"  
|  
| Ports are in same order as defined in SPICE  
Ports 5 6 7 8  
Ports IDP_8 IDP_7 IDP_6 IDP_5  
|  
[End Package Circuit]  
[End Package Model]
```

**Declaration of
Implicit die ports**

IBIS-ISS subcircuit:

```
*****  
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8  
+ TSFile="TouchstoneFileName.e8p"  
  
Sdriver P1 P2 P3 P4 P5 P6 P7 P8  
+ MNAME=TSFile  
+ [FBASE = base_frequency] [FMAX=maximum_frequency]  
*****  
.ends
```

**Matched
by position**

**Matched
by name**



Figure 12 implemented with IBIS-ISS

Legacy IBIS file:

```

-----
| Example of an IBIS model using an IBIS-ISS package model.
| This example implements a package call for the drawing in
| Fig. 12 on pg. 136 of the IBIS v5.0 specification.
|-----
|
[Pin] signal_name model_name
10 Vcc POWER
1 A0 CIRCUITCALL
11 GND GND
2 CAS0 CIRCUITCALL
3 A1 CIRCUITCALL
4a Clk_A CIRCUITCALL
4b Clk_B CIRCUITCALL
5 A2 Buffer_E

[Node Declarations]
| Die nodes:
a b c d e f g h nd1 | List of die nodes
|
| Die pads:
pad_2a pad_2b pad_4 pad_11 | List of die pads
[End Node Declarations]
[Package Model] QS-SMT-cer-8-pin-pkgs
|...
  
```

**Matched
by name**

IBIS-ISS subcircuit:

```

*****
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8
+ P9 P10 P11 P12 P13 P14 P15 P16
+ TSfile="TouchstoneFileName.s16p"

Sdriver P1 P2 P3 P4 P5 P6 P7 P8
+ P9 P10 P11 P12 P13 P14 P15 P16
+ MNAME=TSfile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

*****
.ends
  
```

**Matched
by position**

IBIS .pkg file:

```

-----
| This example implements a package model using an IBIS-ISS
| subcircuit for the drawing in Fig. 12 on pg. 136 of the
| IBIS v5.0 specification.
|-----
|
[Define Package Model] QS-SMT-cer-8-pin-pkgs
[Manufacturer] Quality Semiconductors Ltd.
[OEM] Acme Package Co.
[Description] 8-Pin ceramic SMT package
[Number Of Pins] 8
|
[Pin Numbers]
10 DiePort = IDP_10
1 DiePort = IDP_1
11 DiePort = pad_11
2 DiePort = pad_2a
2 DiePort = pad_2b
3 DiePort = IDP_3
4a DiePort = pad_4
4b DiePort = pad_4
5 DiePort = IDP_5

[Package Circuit]
Language IBIS-ISS

| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ PackageModel.spi S_pkg
|
| Parameters List of parameters
Parameters TSfile = "My_TstoneFile.s16p"
|
| Ports are in same order as defined in SPICE
Ports 10 1 11 2 3 4a 4b 5
Ports IDP_5 pad_4 IDP_3 pad_2b
Ports pad_2a pad_11 IDP_1 IDP_10

[End Package Circuit]
[End Package Model]
  
```

**Implicit die ports
(in blue)**

**Explicit die ports (in red)
are declared under
[Node Declarations]**

**Matched
by name**

Modified Fig. 12 Using BIRD 125 syntax

Legacy IBIS file:

```

-----
| Example of an IBIS model using an IBIS-ISS package model.
|-----
Vcc1 Supply1 POWER
Vcc2 Supply2 POWER
Vcc11 Supply11 POWER
Vcc12 Supply12 POWER
GND1 Ground1 GND
GND11 Ground11 GND
Ref1 Reference1 POWER
Ref11 Reference11 POWER
|
5 Data5 EM5
15 Data15 EM15

[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
Vcc1 NC PCref_EM5
Vcc2 NC PUref_EM5
Vcc11 NC PCref_EM15
Vcc12 NC PUref_EM15
GND1 Ground_EM5 NC
GND11 Ground_EM15 NC
Ref1 NC EXref_EM5
Ref11 NC EXref_EM5
|
5 Ground_EM5 PUref_EM5 Ground_EM5 PCref_EM5 EXref_EM5
15 Ground_EM15 PUref_EM15 Ground_EM15 PCref_EM15 EXref_EM15
|
[Package Model] QS-SMT-cer-10-pin-pkgs
|...
  
```

IBIS .pkg file:

```

-----
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-----
[Define Package Model] QS-SMT-cer-10-pin-pkgs
[Manufacturer] Quality Semiconductors Ltd.
[OEM] Acme Package Co.
[Description] 10-Pin ceramic SMT package
[Number Of Pins] 10

[Pin Numbers]
Vcc1 DiePort = PCref_EM5
Vcc2 DiePort = PUref_EM5
Vcc11 DiePort = PCref_EM15
Vcc12 DiePort = PUref_EM15
GND1 DiePort = Ground_EM5
GND11 DiePort = Ground_EM15
Ref1 DiePort = EXref_EM5
Ref11 DiePort = EXref_EM5
|
5 DiePort = IDP_5
15 DiePort = IDP_15

[Package Circuit]
Language IBIS-ISS

| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ PackageModel.spi S_pkg

| Parameters List of parameters
Parameters TSFile = "My_TstoneFile.s20p"

| Ports are in same order as defined in SPIOB
Ports Vcc1 Vcc2 Vcc11 Vcc12
Ports PCref_EM5 PUref_EM5 PCref_EM15 PUref_EM15
Ports GND1 GND11 Ref1 Ref11
Ports Ground_EM5 Ground_M15 EXref_EM5 EXref_EM15
Ports 5 15
Ports IDP_5 IDP_15

|[End Package Circuit]
|[End Package Model]
  
```

IBIS-ISS subcircuit:

```

*****
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8 P9 P10
+ P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ TSFile="TouchstoneFileName.s20p"
Sdriver P1 P2 P3 P4 P5 P6 P7 P8 P9 P10
+ P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
*****
.ends
  
```

Explicit die ports (red) are declared under [Pin Mapping]

Implicit die ports (blue) are declared here

Matched by name

Matched by name

Matched by position



EBD with IBIS-ISS example

IBIS .ebd file:

```
-----  
| This example implements an EBD model using an IBIS-ISS  
| subcircuit.  
-----
```

```
[Begin Board Description] An_EBD_model  
[Manufacturer]           Noname Company, Inc.  
[Number Of Pins]        4  
|  
[Pin List]  signal_name  
1          POWER5  
2          MySignal  
3          GND  
4          NC  
|  
[Path Description]  
|  
Node  U21.15  
|  
[EBD Circuit]  
Language IBIS-ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ  EBDModel.spi  S_EBD  
|  
| Parameters List of parameters  
Parameters TSFile = "My_TstoneFile.s4p"  
|  
| Ports are in same order as defined in SPICE  
Ports 1  U21.15  3  2  
|  
[End Package Circuit]  
|  
[Reference Designator Map]  
.  
.  
.  
|  
[End Board Description]  
[End]
```

**Matched
by position**

IBIS-ISS subcircuit:

```
*****  
.SUBCKT  S_EBD  P1  P2  P3  P4  
+ TSFile="TouchstoneFileName.s4p"  
  
Sdriver P1  P2  P3  P4  
+ MNAME=TSFile  
+ [FBASE = base_frequency] [FMAX=maximum_frequency]  
*****  
.ends
```



A simple "sliding" package model with IBIS-ISS

Legacy IBIS file:

```
-----  
| Example of an IBIS model using an IBIS-ISS package model  
|-----  
|  
P1] signal_name model_name  
1 Ground_1 GND  
2 Channel_1P ISS_Diff_Tx  
3 Channel_1N ISS_Diff_Tx  
4 Supply_1 POWER  
5 Channel_1P ISS_Diff_Tx  
6 Channel_1N ISS_Diff_Tx  
7 Supply_2 POWER  
8 Channel_2P ISS_Diff_Tx  
9 Channel_2N ISS_Diff_Tx  
10 Ground_2 GND  
|  
[Package Model] A_4_pin_pkg_model  
|...  
|...
```

**Matched
by name**

IBIS-ISS subcircuit:

```
*****  
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8 P9 P10  
+ P11 P12 P13 P14 P15 P16 P17 P18 P19 P20  
+ TSFile = "TouchstoneFileName.s4p"  
+ SlideSelector = 1  
|  
.IF (SlideSelector == 2)  
Sdriver P3 P4 P13 P14  
.ELSEIF (SlideSelector == 3)  
Sdriver P5 P6 P15 P16  
.ELSEIF (SlideSelector == 4)  
Sdriver P7 P8 P17 P18  
.ELSEIF (SlideSelector == 5)  
Sdriver P9 P10 P19 P20  
.ELSE  
Sdriver P1 P2 P11 P12  
.ENDIF  
+ MNAME=TSFile  
*****  
.ends
```

**Matched
by position**

**Slide an .s4p model
along the full pin list**

IBIS .pkg file:

```
-----  
| This example implements a package model using an IBIS-ISS  
| subcircuit.  
|-----  
|  
[Define Package Model] A_10_pin_pkg_model  
[Manufacturer] Noname Company, Inc.  
[OEM] Another Noname Package Company, Inc.  
[Description] 10-pin illustration package model  
[Number Of Pins] 10  
|  
[Pin Numbers]  
1 DiePort = IDP_1  
2 DiePort = IDP_2  
3 DiePort = IDP_3  
4 DiePort = IDP_4  
5 DiePort = IDP_5  
6 DiePort = IDP_6  
7 DiePort = IDP_7  
8 DiePort = IDP_8  
9 DiePort = IDP_9  
10 DiePort = IDP_10  
|  
[Package Circuit]  
Language IBIS-ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ PackageModel.spi S_pkg  
|  
| Parameters List of parameters  
Parameters TSFile = "My_TstoneFile.s4p"  
Parameters SlideSelector = 1  
|  
| Ports are in same order as defined in SPICE  
Ports 1 2 3 4 5 6 7 8 9 10  
Ports IDP_1 IDP_2 IDP_3 IDP_4 IDP_5  
Ports IDP_6 IDP_7 IDP_8 IDP_9 IDP_10  
|  
[End Package Circuit]  
[End Package Model]
```

**Declaration of
Implicit die ports**

**Matched
by name**



Syntax options for “sliding” mechanism

```
*****
.SUBCKT S_pkg P1 P2 P3 P4 P5 P6 P7 P8 P9 P10
+           P11 P12 P13 P14 P15 P16 P17 P18 P19 P20
+ TSFile = "TouchstoneFileName.s4p"
+ SlideSelector = 1

.IF (SlideSelector == 2)
Sdriver P3 P4 P13 P14
.ELSEIF (SlideSelector == 3)
Sdriver P5 P6 P15 P16
.ELSEIF (SlideSelector == 4)
Sdriver P7 P8 P17 P18
.ELSEIF (SlideSelector == 5)
Sdriver P9 P10 P19 P20
.ELSE
Sdriver P1 P2 P11 P12
.ENDIF

+ MNAME=TSFile
*****
.ends
```

.IF/.ELSEIF in IBIS-ISS

**Or using duplicate IBIS-ISS subcircuits
with parameterized filenames and/or subcircuit
names in the “Corner” subparameter**

```
| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ FileNameStringParameter SubCktNameStringParameter
```



Examples for SiSoft's package and EBD modeling proposals implemented with BIRD 125 syntax



SiSoft's IBIS-ISS component pkg

Legacy IBIS file:

```
-----  
| SiSoft's IBIS-ISS component package model example  
| implemented using BIRD 125 syntax  
-----  
|  
[Component] my_ibis_component  
|  
[Pin]  signal_name  model_name  R_pin  L_pin  C_pin  
1     rx1_p         rx         NA     NA     NA  
2     rx1_n         rx         NA     NA     NA  
3     tx1_p         tx         NA     NA     NA  
4     tx1_n         tx         NA     NA     NA  
5     VDDQ         POWER  
6     VSSQ         GND  
|  
[Package Model]  A_differential_pkg_model  
|  
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max  
1  2  
3  4  
|  
[Model]  tx  
. . .  
. . .
```

IBIS-ISS subcircuit (Package.iss):

```
*****  
.subckt Diff_Pins_1_2 pinH pinL padH padL  
+ Td=50ps Zo=50  
  
T1 pinH 0 padH 0 Td=Td Zo=Zo  
T2 pinL 0 padL 0 Td=Td Zo=Zo  
  
*****  
.ends Diff_Pins_1_2
```

IBIS .pkg file:

```
-----  
| This example implements a package model using an IBIS-ISS  
| subcircuit.  
-----  
|  
[Define Package Model]  A_differential_pkg_model  
[Manufacturer]          Noname Company, Inc.  
[OEM]                   Another Noname Package Company, Inc.  
[Description]           Illustration package model  
[Number Of Pins]  2  
|  
[Pin Numbers]  
  1  DiePort = IDP_1  
  2  DiePort = IDP_2  
|  
[Package Circuit]  
Language IBIS-ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ Package.iss Diff_Pins_1_2  
|  
| Parameters List of parameters  
Parameters Td = 99ps  
Parameters Zo = 51  
|  
| Ports are in same order as defined in SPICE  
Ports 1 2 IDP_1 IDP_2  
|  
[End Package Circuit]  
[End Package Model]
```



SiSoft's IBIS-ISS coupled component pkg

Legacy IBIS file:

```
|-----|
| SiSoft's IBIS-ISS component package model example with
| crosstalk and power implemented using BIRD 125 syntax
|-----|
|
|[Component] my_ibis_component
|
|[Pin]  signal_name  model_name  R_pin  L_pin  C_pin
1      rx1_p        rx          NA     NA     NA
2      rx1_n        rx          NA     NA     NA
3      tx1_p        tx          NA     NA     NA
4      tx1_n        tx          NA     NA     NA
5      VDDQ         POWER
6      VSSQ         GND
|
|[Package Model]  A_coupled_pkg_model
|
|[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
1  2
3  4
|
|[Model] tx
. . .
. . .
```

IBIS-ISS subcircuit (Package.iss):

```
*****
.subckt Coupled_Power P1 P2 P3 P4 P5 P6
+ P7 P8 P9 P10 P11 P12
+ TSfile="TouchstoneFileName.s12p"

Sdriver P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12
+ MNAME=TSfile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]

*****
.ends Coupled_Power
```

IBIS .pkg file:

```
|-----|
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-----|
|
|[Define Package Model]  A_coupled_pkg_model
|[Manufacturer]          Noname Company, Inc.
|[OEM]                   Another Noname Package Company, Inc.
|[Description]           Illustration package model
|[Number Of Pins]       6
|
|[Pin Numbers]
1  DiePort = IDP_1
2  DiePort = IDP_2
3  DiePort = IDP_3
4  DiePort = IDP_4
5  DiePort = IDP_5
6  DiePort = IDP_6
|
|[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ Package.iss Coupled_Power
|
| Parameters List of parameters
Parameters TSfile = "My_TstoneFile.s12p"
|
| Ports are in same order as defined in SPICE
Ports 1 2 3 4 5 6
Ports IDP_1 IDP_2 IDP_3 IDP_4 IDP_5 IDP_6
|
|[End Package Circuit]
|[End Package Model]
```



SiSoft's IBIS-ISS EBD example

IBIS .ebd file:

```
-----  
| SiSoft's IBIS-ISS EBD example implemented using BIRD 125 syntax  
-----  
[Begin Board Description] Simple  
[Number Of Pins] 2  
|  
[Pin List] signal_name  
1 DQS0  
2 DQS0#  
|  
[Path Description]  
Node U1.8  
Node U1.9  
Node U2.8  
Node U2.9  
Node U3.8  
Node U3.9  
Node U4.8  
Node U4.9  
|  
[EBD Circuit]  
Language IBIS-ISS  
|  
| Corner corner_name file_name circuit_name (.subckt name)  
Corner Typ Simple.iss Pins_1_2  
|  
| Parameters List of parameters  
Parameters TSFile = "My_TstoneFile.s10p"  
|  
| Ports are in same order as defined in SPICE  
Ports 1 2 U1.8 U1.9 U2.8 U2.9 U3.8 U3.9 U4.8 U4.9  
|  
[End Package Circuit]  
|  
[Reference Designator Map]  
| Ref Des File name Component name  
U1 simple.ibs simple  
U2 simple.ibs simple  
U3 simple.ibs simple  
U4 simple.ibs simple  
|  
[End Board Description]  
[End]
```

IBIS-ISS subcircuit:

```
*****  
.SUBCKT Pins_1_2 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10  
+ TSFile="TouchstoneFileName.s10p"  
  
Sdriver P1 P2 P3 P4 P5 P6 P7 P8 P9 P10  
+ MNAME=TSFile  
+ [FBASE = base_frequency] [FMAX=maximum_frequency]  
  
*****  
.ends
```



Overview of SiSoft's analog modeling proposals



Overview of the SiSoft analog BIRD drafts

- **They were originally part of BIRD 119**
 - the goal of BIRD 119 was to bring the Opal™ features to IBIS
 - BIRD 119 was split into four independent BIRDS on the request of the ATM group
- **BIRD 122 became the “Analog Modeling BIRD”**
 - up to this point, there was no mention of IBIS-ISS or package modeling in these BIRDS
- **A draft for BIRD 122.1 was distributed in March 2011**
 - this version included the idea of making use of IBIS-ISS and to address package modeling also
 - this BIRD draft was rather informal, contained mostly examples
- **The draft of BIRD 122.1 was split into two (unnumbered) BIRD drafts in May 2011**
 - the content is still in an “early stage” condition (mostly examples)
 - there are many undefined rules, ambiguities, inconsistencies



Overview of SiSoft's buffer BIRD draft

- **There are three main features in this BIRD draft**
 - **IBIS-ISS analog buffer subcircuit parameters in .ibs file**
 - this is done with a new keyword: [External ISS], [End External ISS]
 - subparameters include: ISS_Buffer_File, ISS_Buffer_Subckt, ISS_Buffer_Arguments, Tx_Voh, Tx_Vol, Tx_Trf
 - The ISS_Buffer parameters may be defined in either the .ami file or in the [Model] section of a .ibs file: IBIS([Voltage Range]), Vref=IBIS(Vref), C_comp=AMI(Cc)
 - **IBIS-ISS analog buffer subcircuit parameters in .ami file**
 - reserved parameters: ISS_Buffer_File, ISS_Buffer_Subckt, ISS_Buffer_Arguments, Tx_Voh, Tx_Vol, Tx_Trf
 - Model_Specific parameters: C_comp, Impedance, etc...
 - **intrinsic analog buffer model (defined in .ami file)**
 - this works the same way as IBIS-ISS analog buffer subcircuit in .ami file, except the value for ISS_Buffer_Subckt is (Value "Intrinsic_Tstonefile_Tx")
 - no IBIS-ISS subcircuit is needed, because the (hard coded, or predefined) circuit is assumed by the simulator
 - Model_Specific parameters are as defined in the Opal™ document



Overview of SiSoft's package BIRD draft

- **There are two main features in this BIRD draft**

- **IBIS-ISS analog package subcircuit parameters in .ibs file**

- this is done with several new keywords: [ISS Packages], [End ISS Packages], [ISS Package], [End ISS Package]
 - subparameters include: ISS_Package_File, ISS_Package_Subckt, ISS_Package_Arguments, Pin, PinP, PinN, Pad, PadP, PadN, Td=AMI (Td), Zo=AMI (Zo), etc...
 - another form of parameter definition appears: Parameter Zo 50 45 55
 - a new, special node syntax: Pin.1, Pin.[Pullup Reference], etc... is shown in the examples
 - the package can be called from a (new) subparameter of Component:

```
[Component] my_ibis_component  
ISS_Package component_package
```

or from the inside of a [Model]:

```
[Model] tx  
Model_type Output  
...  
ISS_Package tx_package Td=AMI (Length) Zo=AMI (Zo)
```
 - there is another “more IBIS like” syntax example in the proposal
- **IBIS-ISS analog package subcircuit parameters in .ami file**
 - this is missing from this BIRD draft, but it was present in a previous version



General summary of the SiSoft BIRD drafts

- **They contain a lot of good ideas, but little attempt is made to implement them with existing keywords**
 - new [External ISS] vs. reusing [External Model],
 - new [ISS Packages] vs. reusing [Define Package Model], etc...
 - this may be good from one perspective but bad from another
- **These BIRD drafts need a lot of work to get to a finished condition**
 - the draft itself contains numerous inconsistencies, the ideas need to be matured
 - there are a lot of completely new ideas to IBIS, like the dot syntax for node names
 - the numerous new syntax ideas need rigorous rules
 - this may take a huge amount of time and effort



Summary of the SiSoft buffer BIRD draft

- **Do we really want to add hard coded “intrinsic” analog models to the specification?**
 - IBIS-ISS can do the same and more, is this necessary then?
- **Do we really want to instantiate analog buffer models (IBIS-ISS subcircuits) from .ami files?**
 - it is somewhat questionable to put analog buffer model parameters into the “digital” .ami files, but we can live with that...
- **If we decided to eliminate these two features, the only thing that is left is the [External ISS] keyword in the .ibs file**
 - this capability, however, is already described in BIRD 116, making use of the existing [External Model] keyword
 - is it really necessary to introduce a new keyword for a very similar functionality?



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