BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)

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ISSUE TITLE: *Interconnect Modeling Using IBIS-ISS*
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STATEMENT OF THE ISSUE:

This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to new Terminal definitions defined for buffers.

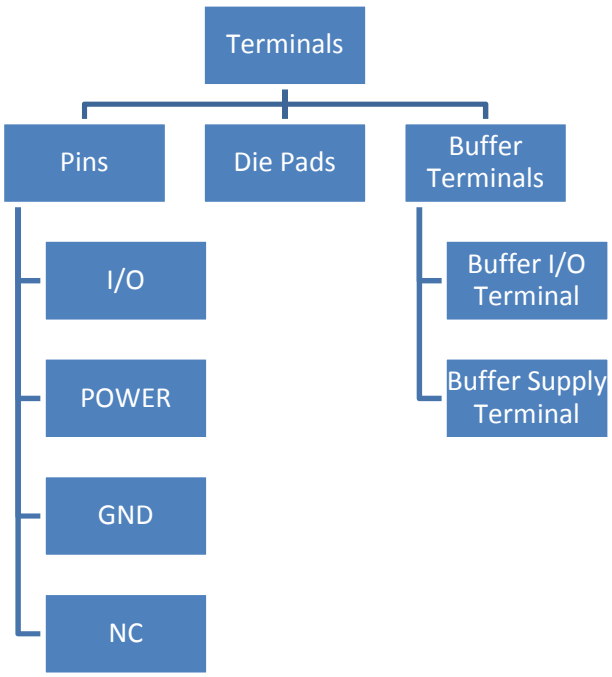
ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:

Definitions:

Enhanced interconnect descriptions in IBIS, called hereinafter “IBIS Interconnect Models”, rely on several assumptions:

1. IBIS Interconnect Models can be described either using IBIS-ISS subcircuit files or Touchstone files. Interconnect Model definitions may be included inside an IBIS file, but neither IBIS-ISS nor Touchstone data may be included inside an IBIS file.
2. If two points in an IBIS Interconnect Model are “Linked”, then there is either a low resistance DC electrical path between the two points, or a small insertion loss at the Nyquist frequency between the two points. For the purposes of IBIS Interconnect Models, “point” and “node” refer to identical locations.
3. IBIS Components, and therefore IBIS Interconnect Models, contain terminals consisting of Pins, Die Pads, Buffer I/O Terminals, and Buffer Supply Terminals. Pins are defined under the [Pin] keyword, and may be I/O, POWER, GND, or NC.
4. Under [Pin], for each signal_name associated with Model_name POWER or GND, all Pins, Die Pads and Buffer Supply Terminals that use that signal_name are “Linked”
5. IBIS assumes that each I/O [Pin] is connected to one Die Pad and one Buffer I/O Terminal. Two differential I/O pins shall be connected to two differential die pads and either two single-ended Buffer I/O Terminals or a single true differential Buffer I/O Terminal.
6. If multiple Buffer Terminals (Supply or I/O) are connected to a single pin, EBD and, when available, EMD shall be used for the interconnect description.
7. An Interconnect Model may describe the relationship between a single Pin and Buffer Terminal (Supply or I/O), a single Pin and Die Pad, or between a single Die Pad and a Buffer Terminal (Supply or I/O). An Interconnect Model may also describe connections

between multiple Pins and multiple Buffer Terminals (Supply and I/O), multiple Pins and multiple Die Pads, or multiple Die Pads and multiple Buffer Terminals (Supply and I/O).



ANY OTHER BACKGROUND INFORMATION:

Parameter is shorted to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File_names are not quoted, to be consistent with Corner in the multi-lingual syntax.

For File_TS, all columns typ, min, and max are entered (or NA for either or both min and max) to follow the corner syntax convention used for most IBIS keywords and subparameters. The typ entry is required, and the typ entry value is used by the EDA tool for any NA entry. The same typ, min, max convention is used for the subparameter Param.

Entries for strings in Param are surrounded by double quotes to be consistent with string_literal Parameters in the multi-lingual syntax (or where the AMI string_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner. Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

The following keywords should be added as their own Chapter. The current Chapter 7 should be modified with the existing text placed in a sub-section called "[PACKAGE MODEL]".

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7 PACKAGE MODELING

Several types of package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector] and the keywords associated with it

The lumped formats are described in the [Package] and [Pin] keyword defintions above. The [Package Model] format is described in this chapter, while Interconnect Model Selectors are described in Chapter 13.

…

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13 INTERCONNECT MODEL SELECTORS

This chapter defines an advanced format for interconnect descriptions that may be used for packages as well as other types of interconnect between buffer models and pins, for signal and power path modeling purposes.

The specification permits .ibs files to contain the following additional list of interconnect model keywords and subparameters. Note that the actual interconnect models may be in a separate < filename>.ict file or may exist in a .ibs file between the [Begin Interconnect Model] ... [End Interconnect Model] keywords for each interconnect model defined. For reference, these keywords and subparameters are listed in **Error! Reference source not found.**.

Table XX – Interconnect Modeling Keywords and Subparameters

Keyword or Subparameter	Notes
[Begin Interconnect Model]	
Manufacturer	
Description	
Param	
File_TS	(note 2)
File_IBIS-ISS	(note 2)
Unused_Terminal_Termination	(note 3)
Number Of Terminals	(note 4)

Keyword or Subparameter	Notes
<terminal line>	(note 5)
[End Interconnect Model]	(note 1)
Note 1 Required when the [Begin Interconnect Model] keyword is used Note 2 One of either the File_TS or File_IBIS-ISS subparameters is required. Note 3 The subparameter token shall be followed by the "=" character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace. Note 4 The subparameter token shall be followed by the "=" character and an integer value, with both optionally surrounded by whitespace. Note 5 No token or other reserved word is defined to identify terminal lines.	

When interconnect model definitions occur within a .ibs file, their scope is "local"— they are known only within that .ibs file and no other. In addition, within that .ibs file, they override any interconnect package models defined using the [Pin], [Package Model] or [Define Package Model] keywords.

Usage Rules for the .ict File:

Package models are stored in a file whose name looks like:

<filename>.ict.

The <filename> provided must adhere to the rules given in Section **Error! Reference source not found.**, "GENERAL SYNTAX RULES AND GUIDELINES". Use the ".ict" extension to identify files containing interconnect models. The .ict file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparametersfollow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .ict file. The .ict file is for interconnect models only.

Keyword: **[Interconnect Model Selector]**

Required: No

Description: Used to list available interconnect models for the Component.

Usage Rules: Interconnect Models are described by IBIS-ISS subcircuits or Touchstone files that connect the Pins, Die Pads, and Buffer Terminals (Supply and I/O) of a Component.

A Component may have none, one, or more than one Interconnect Model associated with it. If any Interconnect Models exist for the Component, they shall be listed in this section. An Interconnect Model Selector is required even if only a single Interconnect Model is associated with the Component. [Interconnect Model Selector] is hierarchically within the scope of the [Component] keyword.

The section under the [Interconnect Model Selector] keyword shall have two fields per line, with each line defining the Interconnect Models associated with the Component. The fields shall be separated by at least one white space. The first field lists the Interconnect Model name (up to 40 characters long). The second field is the name of the file containing the Interconnect Model, with the extension ".ict". If the Interconnect Model is in this IBIS file, then the second field shall be "*".

The file containing the Interconnect Model shall be located in the same directory as the .ibs file. The file name shall follow the rules for .ibs file names given in Section 3, 'GENERAL SYNTAX RULES AND GUIDELINES".

The first entry under the [Interconnect Model Selector] keyword shall be considered the default by the EDA tool. Each Interconnect Model name may only appear once under the [Interconnect Model Selector] keyword for a given Component.

Example:

```
[Interconnect Model Selector]
   QS-SMT-cer-8-pin-pkgs_iss *
   QS-SMT-cer-8-pin-pkgs_sNp qs-smt-cer-8-pin-pkgs_s16p.ict
[End Interconnect Model Selector]
```

Keyword: [**End Interconnect Model Selector**]
Required: Yes, for each instance of the [Begin Interconnect Model Selector] keyword
Description: Indicates the end of the Interconnect Model Selector data.
Example:

```
[End Interconnect Model Selector]
```

Keyword: **[Begin Interconnect Model]**

Required: No

Description: Marks the beginning of an Interconnect Model description.

Sub-Params: Manufacturer, Description, Unused_Terminal_Termination, Number_of_Terminals, Param, File_TS, File_IBIS-ISS

Usage Rules: [Begin Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Begin Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically equivalent in scope to [Component] and [Model].

The [Begin Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Component].

The following subparameters are defined:

Manufacturer
Description

Unused_Terminal_Termination = <value>
Number_of_Terminals = <value>
Param
File_TS
File_IBIS-ISS

In addition to these subparameters, the [Begin Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Manufacturer rules:

This optional subparameter specifies the name of the interconnect's manufacturer. The length of the manufacturer's name shall not exceed 40 characters. Blank characters are permitted.

Description rules:

This optional subparameter provides a concise yet easily human-readable description of what the Interconnect Model represents. The description shall be fewer than 60 characters in length, shall fit on a single line, and may contain spaces.

Unused_Terminal_Termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the Terminals of any IBIS-ISS subcircuit or Touchstone network that is not being used in the [Begin Interconnect Model]/[End Interconnect Model] group. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the "=" character. The subparameter name, "=" character, and argument may optionally be separated by whitespace.

If this subparameter is present, the EDA tool should connect the unused Terminals to GND through a resistor with the value of resistance in ohms provided in the argument.

If this parameter is not defined and File_IBIS-ISS is present, then the EDA tool should connect the unused Terminals to GND through a 1 megaohm or larger resistor (the exact value used shall be reported to the user by the EDA tool). If File_TS is present, then the EDA tool should connect the unused Terminals to GND through a resistor with the Touchstone file's reference resistance for the corresponding Terminal.

Only one Unused_Terminal_Termination subparameter may appear for a given [Begin Interconnect Model] keyword.

Number_of_Terminals rules:

The Number_of_Terminals subparameter is required and defines the number of Terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the

subparameter name by the "=" character. The subparameter name, "=" character, and argument may optionally be separated by whitespace. Only one Number_of_Terminals subparameter may appear for a given [Begin Interconnect Model] keyword. The Number_of_Terminals subparameter shall appear before any Terminal lines and after the Manufacturer subparameter for a given Interconnect Model.

Param rules:

The subparameter Param is optional and only legal with the File_IBIS-ISS subparameter documented below. Param is illegal with the File_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3, "GENERAL SYNTAX RULES AND GUIDELINES". The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to The Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

Examples:

```
| Param   name     format   value
Param     abc      Value    2m         | 2E-3 in IBIS
Param     def      Value    4k         | 4E3 in IBIS
Param     ts_file  Value    "typ_s2p"  | file name string passed
                                       | into IBIS-ISS
```

File_IBIS-ISS rules:

Either File_IBIS-ISS or File_IBIS-TS is required for a [Begin Interconnect Model]/[End Interconnect Model] group. The File_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file_name, and circuit_name (.subckt name) for an IBIS-ISS file. . The referenced file under file_name shall be located in the same directory as the .ibs file.

Example:

```
| file_type    file_name    circuit_name(.subckt name)
File_IBIS-ISS  net.iss      netlist_typ
```

File_TS rules:

Either File_TS or File_IBIS-ISS is required for a [Begin Interconnect Model]/[End Interconnect Model] group. File_TS is followed by one unquoted string argument, which is the file name for a Touchstone file. The Touchstone file under file_name shall be located in the same directory as the referencing.ibs file or .ict file.

Example:

```
| file_type     file_name
File_TS         typ.s8p
```

Terminal Line rules:

Terminal lines shall appear after the Number_of_Terminals subparameter and before the [End Interconnect Model] keyword. No token or reserved word identifies terminal lines.

Each Terminal line contains information on a terminal of an IBIS-ISS subcircuit (or Touchstone file).

Terminal lines are of the form

<Terminal_number> <Terminal_type> <Terminal_type_qualifier> Aggressor

Terminal_number
Terminal_number is an identifier for a specific terminal. Terminal_number shall be a positive non-zero integer less than or equal to the value of the Number_of_Terminals argument. The same Terminal_number shall not appear more than once for a given Interconnect Model. If any Terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused_Terminal_Termination rules.

Terminal_type shall be one of the following: Buffer_I/O, PUref, PDref, PCref, GCref, EXTref, Buffer_Rail, Pad_I/O, Pad_Rail, Pin_I/O, or Pin_Rail. Buffer_I/O, PUref, PDref, PCref, GCref, EXTref and Buffer_Rail are terminals of an Interconnect Model that connect directly to I/O buffers. Pin_I/O and Pin_Rail are terminals that are at the Die/Package interface. Pin_I/O and Pin_Rail are terminals that are at the Component PCB interface.

The Terminal_type_qualifier for Terminal_types Buffer_I/O, PUref, PDref, PCref, GCref and EXTref shall be pin_name. The Terminal_type_qualifier for Terminal_type Buffer_Rail may be signal_name or bus_label.

The Terminal_type_qualifier for Terminal_type Pad_I/O shall be pin_name.

The Terminal_type_qualifier for Terminal_type Pad_Rail shall be either pad_name, signal_name, or bus_label.

The Terminal_type_qualifier for Terminal_type Pin_I/O shall be pin_name.

The Terminal_type_qualifier for Terminal_type Pin_Rail shall be either pin_name, signal_name, or bus_label.

The optional Aggressor field is only allowed allowed on Buffer_I/O records. Connections to Buffer_I/O terminals may be missing coupling to connects that are not included in this interconnect model.

Table XX summarizes the rules described above.

Table XX – Allow Terminal_Type Associations[1]

Terminal_type	pin_name	signal_name	bus_label	pad_name	Aggressor

Terminal_type	pin_name	signal_name	bus_label	pad_name	Aggressor
Buffer_I/O	X				A
PUref	X				
PDref	X				
PCref	X				
GCref	X				
EXTref	X				
Buffer_Rail		Y	Y		
Pad_I/O	X				
Pad_Rail		Y	Y	Z	
Pin_I/O	X				
Pin_Rail	Y	Y	Y		

Notes

1) In the table, “X” refers to I/O pin names. “Y” and “Z” are POWER and GND names. The letter “A” refers to buffer names.

Connecting Pins, Pads and Terminals

Three classes of pins are defined for a Component: Signal Pins, Supply Pins and No Connect Pins. Supply Pins have a model_name of either POWER or GND. No Connect Pins have model_name NC. All other pins are classified as Signal Pins. Package models defined in this section assume that there is one Buffer_I/O Terminal and one Die Pad for each Signal Pin. Pins are assumed to use the names listed under the first column of the [Pin] keyword (the pin_name column).

The model of an I/O buffer has supply terminals in addition to the Buffer_I/O. These supply (or rail) terminals can be PUref, PDref, PCref, GCref and/or EXTref. The PUref, PDref, PCref, GCref and/or EXTref terminal of a buffer are associated either with a bus_label under the [Pin Mapping] keyword or a signal_name under the [Pin] keyword. These terminals can be connected to interconnect models one of two ways:

1. By specifying a unique interconnect terminal for each I/O buffer PUref, PDref, PCref, GCref and/or EXTref
2. By assuming that all I/O buffer supply terminals connected to a supply signal_name or bus_label are shorted together. This is done by specifying a unique terminal for all I/O buffer terminals that are connected to a specific signal_name or bus_label on at least one Supply Pin.

Pads are the location of the interface between the die and the package. Interconnect models can either be between the Pins of a component and the I/O buffers, or they can be split into models between the

Pins of a component and the Pads of the die, and model between the Pads of the die and the I/O buffer models. There is exactly one Pad (Pad_I/O) for each Signal Pin. There can be any number of Pads (Pad_Rail) for each signal_name or buf_label on Supply Pins. If interconnect models of supply (rail) networks are split between Pin/Pad and Pad/Buffer models, then the interface of supply connections at the die package interface can be handled in one of two ways:

1. By defining a list of Die Supply Pads, and specifying terminals for some or all of the Die Supply Pads that are connected to a bus_label or signal_name on at least one Supply Pin.
2. By assuming that all supply Pads connected to a supply signal_name or bus_label are shorted together. This is done by specifying a unique terminal for all Pads that are connected to a specific signal_name on at least one Supply Pin.

Pins may be terminals of the Interconnect model that connect directly to a PCB board or other type of system connection to an IBIS component. Pins can be Signal Pins (Pin_I/O), or Supply Pins (Pin_Rail). An Interconnect model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the Supply Pins.
2. By assuming that all supply Pins connected to a supply signal_name or bus_label are shorted together. This is done by specifying a unique terminal for all Pins that are connected to a specific signal_name on at least one Supply Pin.

For an Interconnect Model using File_TS with N ports, N shall match the number of ports present in the data of the associated Touchstone 1.x file, or the value associated with the [Number of Ports] field in the associated Touchstone 2 file. The [Number of Terminals] entry in the Interconnect Model shall be an integer equal to N+1. Terminal rules are described below:

- The EDA tool shall use the pin_name or signal_name specified for the associated Terminal "N+1" entry as the reference node for each of the N ports. For an Interconnect Model with N ports, the Terminals and Ports are associated as follows:
  - Terminal — Port
  - 1 — 1
  - 2 — 2
  - …
  - N — N
  - N+1 — reference
- If a Port is not connected, then it shall be terminated by the EDA tool with a resistor to the node on Terminal N+1. The value of this resistance shall be the value associated with the Port Reference Impedance subparameter.
- Terminal N+1 shall be connected to a Pin, Pad, or Buffer which is in turn connected to a signal_name of POWER or GND.

The Terminals of an Interconnect Model may be located at Pins and Pads, Pins and Buffers, or Pads and Buffers. A single Interconnect Model shall not have Terminals at Pins, Pads and Buffers simultaneously.

Examples:

```
[Pin] signal_name model_name      R_pin   L_pin   C_pin
A1    DQ1         DQ
A2    DQ2         DQ
A3    DQ3         DQ
D1    DQS+        DQS
D2    DQS-        DQS
P1    VDD         POWER
P2    VDD         POWER
P3    VDD         POWER
P4    VDD         POWER
P5    VDD         POWER
G1    VSS         GND
G2    VSS         GND
G3    VSS         GND
G4    VSS         GND

[Diff Pin] inv_pin  vdiff  tdelay_typ tdelay_min tdelay_max
D1          D2       NA     NA         NA         NA

[Die Supply Pads]  signal_name
VDD1 VDD
VDD2 VDD
VDD3 VDD
VSS1 VSS
VSS2 VSS

[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
A1            VSS          VDD        NC            NC              NC
A2            VSS          VDD        NC            NC              NC
A3            VSS          VDD        NC            NC              NC
D1            VSS          VDD        NC            NC              NC
D2            VSS          VDD        NC            NC              NC

[Begin Interconnect Model]     QS-SMT-cer-8-pin-pkgs_iss
| Full Package/Die Model Complex Power Distribution
Number_of_Terminals 29
1  Pin_I/O     Pin_name A1  |  DQ1         DQ
2  Pin_I/O     Pin_name A2  |  DQ2         DQ
3  Pin_I/O     Pin_name A3  |  DQ3         DQ
4  Pin_I/O     Pin_name D1  |  DQS+        DQS
5  Pin_I/O     Pin_name D2  |  DQS-        DQS
6  Pin_I/O     Pin_name P1  |  VDD         POWER
7  Pin_I/O     Pin_name P2  |  VDD         POWER
8  Pin_I/O     Pin_name P3  |  VDD         POWER
9  Pin_I/O     Pin_name P4  |  VDD         POWER
10 Pin_Rail    Pin_name P5  |  VDD         POWER
11 Pin_Rail    Pin_name G1  |  VSS         GND
12 Pin_Rail    Pin_name G2  |  VSS         GND
13 Pin_Rail    Pin_name G3  |  VSS         GND
14 Pin_Rail    Pin_name G4  |  VSS         GND
15 Buffer_I/O  Pin_name A1  |  DQ1         DQ
16 Buffer_I/O  Pin_name A2  |  DQ2         DQ
17 Buffer_I/O  Pin_name A3  |  DQ3         DQ
18 Buffer_I/O  Pin_name D1  |  DQS+        DQS
19 Buffer_I/O  Pin_name D2  |  DQS-        DQS
```

```
20 PUref        Pin_name A1   |   DQ1          DQ
21 PUref        Pin_name A2   |   DQ2          DQ
22 PUref        Pin_name A3   |   DQ3          DQ
23 PUref        Pin_name D1   |   DQS+         DQS
24 PUref        Pin_name D2   |   DQS-         DQS
25 PDref        Pin_name A1   |   DQ1          DQ
26 PDref        Pin_name A2   |   DQ2          DQ
27 PDref        Pin_name A3   |   DQ3          DQ
28 PDref        Pin_name D1   |   DQS+         DQS
29 PDref        Pin_name D1   |   DQS+         DQS
[End Interconnect Model]
```

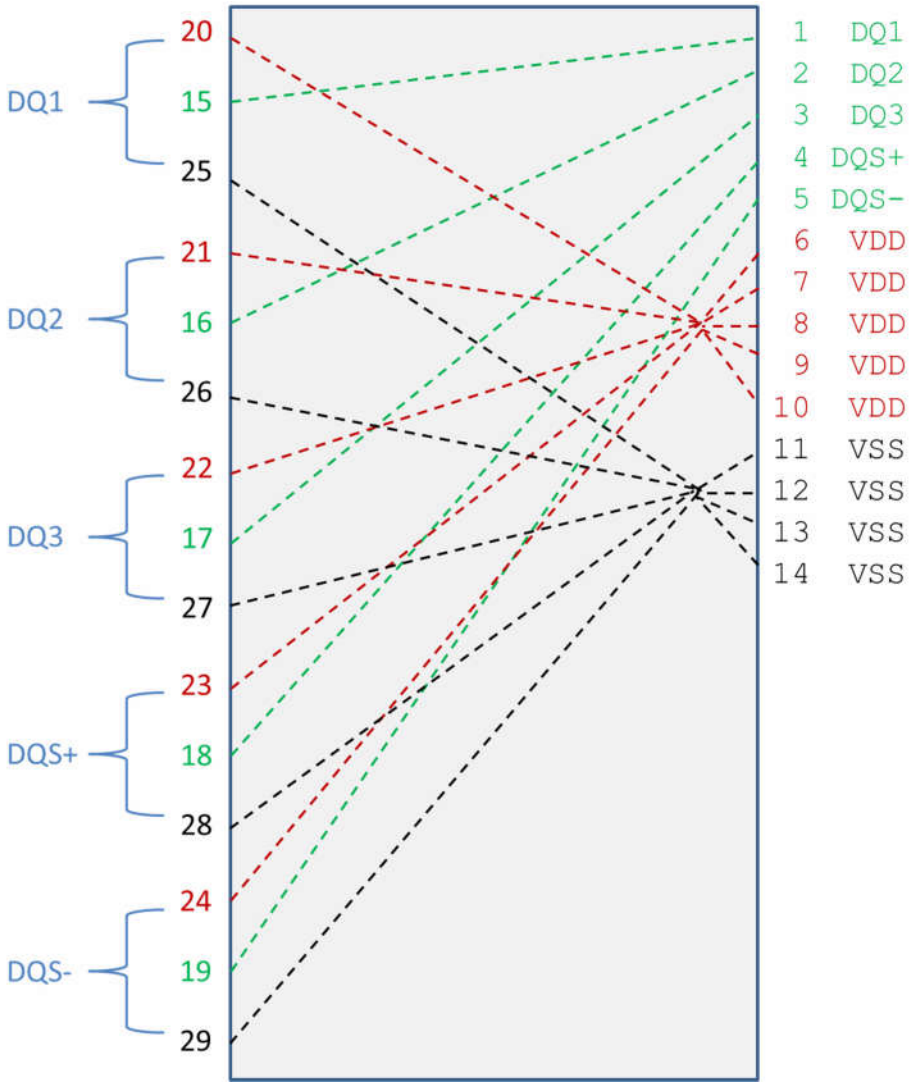

Figure 1 – Electrical Connections for Full Package/Die Model Complex Power Example

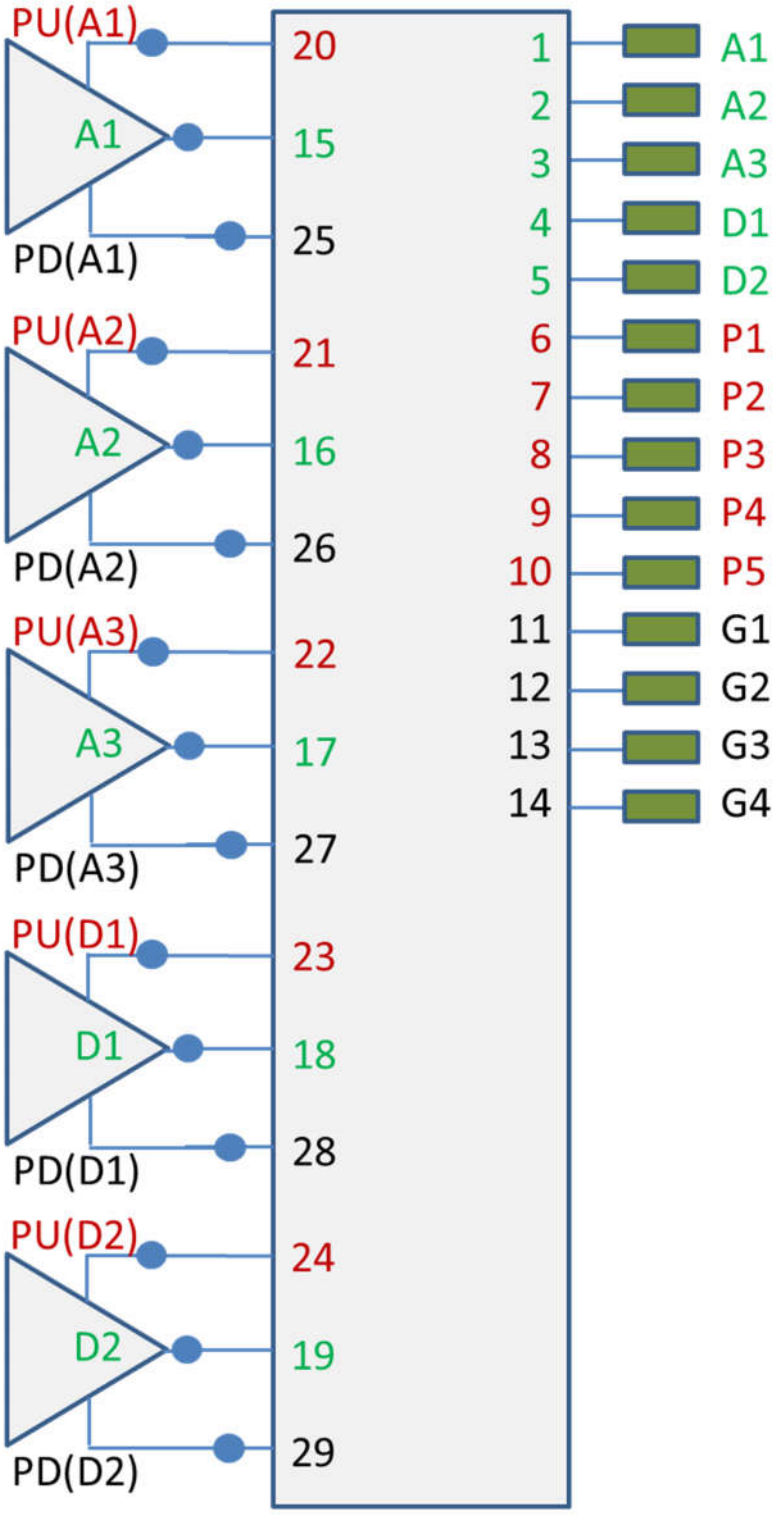

Figure 2 – Buffer and Pin Connections for Full Package/Die Model Complex Power Example

| Full Package/Die Model Simple Power Distribution

```
[Begin Interconnect Model]
Number_of_Terminals 14
1  Pin_I/O     Pin_name A1          |  DQ1          DQ
2  Pin_I/O     Pin_name A2          |  DQ2          DQ
3  Pin_I/O     Pin_name A3          |  DQ3          DQ
4  Pin_I/O     Pin_name D1          |  DQS+         DQS
5  Pin_I/O     Pin_name D2          |  DQS-         DQS
6  Pin_Rail    signal_name   VDD    |  VDD          POWER
7  Pin_Rail    signal_name   VSS    |  VSS          GND
8  Buffer_I/O  Pin_name A1          |  DQ1          DQ
9  Buffer_I/O  Pin_name A2          |  DQ2          DQ
10 Buffer_I/O  Pin_name A3          |  DQ3          DQ
11 Buffer_I/O  Pin_name D1          |  DQS+         DQS
12 Buffer_I/O  Pin_name D2          |  DQS-         DQS
13 Buffer_Rail signal_name   VDD    |  VDD          POWER
14 Buffer_Rail signal_name   VSS    |  VSS          GND
[End Interconnect Model]
```

| Single DQ (A1)

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 2
1 Pin_I/O     Pin_name A1
2 Buffer_I/O  Pin_name A1
[End Interconnect Model]
```

| Single DQ (A1), Split into package and on-die models

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 2
1 Pin_I/O     Pin_name A1
2 Pad_I/O     Pin_name A1
[End Interconnect Model]

[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs2_iss
Number_of_Terminals 2
1 Pad_I/O     Pin_name A1
2 Buffer_I/O  Pin_name A1
[End Interconnect Model]
```

|Full VDD Power Supply Model

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 9
1 Pin_Rail   Pin_name P1  |  VDD         POWER
2 Pin_Rail   Pin_name P2  |  VDD         POWER
3 Pin_Rail   Pin_name P3  |  VDD         POWER
4 Pin_Rail   Pin_name P4  |  VDD         POWER
5 Pin_Rail   Pin_name P5  |  VDD         POWER
6 PDref Pin_name A1  |  DQ1         DQ
7 PDref Pin_name A2  |  DQ2         DQ
8 PDref Pin_name A3  |  DQ3         DQ
9 PDref Pin_name D1  |  DQS+        DQS
[End Interconnect Model]
```

|Full VDD Power Supply Model split into package and on-die

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 8
1 Pin_Rail Pin_name P1   |  VDD         POWER
2 Pin_Rail Pin_name P2   |  VDD         POWER
3 Pin_Rail Pin_name P3   |  VDD         POWER
4 Pin_Rail Pin_name P4   |  VDD         POWER
5 Pin_Rail Pin_name P5   |  VDD         POWER
6 Pad_Rail Pad_name VDD1 |  VDD         POWER
7 Pad_Rail Pad_name VDD2 |  VDD         POWER
8 Pad_Rail Pad_name VDD3 |  VDD         POWER
[End Interconnect Model]

[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs2_iss
Number_of_Terminals 7
1 Pad_Rail Pad_name VDD1 |  VDD         POWER
2 Pad_Rail Pad_name VDD2 |  VDD         POWER
3 Pad_Rail Pad_name VDD3 |  VDD         POWER
4 PDref    Pin_name A1   |  DQ1         DQ
5 PDref    Pin_name A2   |  DQ2         DQ
6 PDref    Pin_name A3   |  DQ3         DQ
7 PDref    Pin_name D1   |  DQS+        DQS
[End Interconnect Model]
```

|Power supply model assuming pins shorted, pads shorted, and buffer rail shorted

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 2
1 Pin_Rail     signal_name VDD  |  VDD         POWER
2 Buffer_Rail  signal_name VDD  |  VDD         POWER
[End Interconnect Model]
```

|Power supply model assuming pins shorted, pads shorted, and buffer rail shorted, split between package and die

```
[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 2
1 Pin_Rail      signal_name VDD  |  VDD         POWER
2 Pad_Rail      signal_name VDD  |  VDD         POWER
[End Interconnect Model]

[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs2_iss
Number_of_Terminals 2
1 Pad_Rail      signal_name VDD  |  VDD         POWER
2 Buffer_Rail   signal_name VDD  |  VDD         POWER
[End Interconnect Model]
```

| Single DQ Crosstalk Model

```
[Begin Interconnect Model]  DIP-6-pin-pkgs_iss
Number_of_Terminals 6
1 Pin_I/O     Pin_name A1
2 Buffer_I/O  Pin_name A1 Aggressor
3 Pin_I/O     Pin_name A2
4 Buffer_I/O  Pin_name A2
5 Pin_I/O     Pin_name A3
6 Buffer_I/O  Pin_name A3 Aggressor
[End Interconnect Model]
```

Example with signal_name split into bus_labels

Examples:

```
[Pin] signal_name model_name      R_pin   L_pin   C_pin
A1    DQ1         DQ
A2    DQ2         DQ
A3    DQ3         DQ
A4    DQ4         DQ
P1    VDD         POWER
P2    VDD         POWER
G1    VSS         GND
G2    VSS         GND

[Bus Label] signal_name
VDD1 VDD
VDD2 VDD

[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
A1            VSS          VDD1       NC            NC              NC
A2            VSS          VDD1       NC            NC              NC
A3            VSS          VDD2       NC            NC              NC
A4            VSS          VDD2       NC            NC              NC
P1            NC           VDD1       NC            NC              NC
P2            NC           VDD2       NC            NC              NC
G1            VSS          NC         NC            NC              NC
G2            VSS          NC         NC            NC              NC


|Power supply model assuming pins shorted, pads shorted, and buffer rail
|shorted

[Begin Interconnect Model]  QS-SMT-cer-8-pin-pkgs_iss
Number_of_Terminals 2
1 Pin_Rail     signal_name VDD  |  VDD         POWER
2 Pin_Rail     signal_name VSS  |  VSS         GND
3 Buffer_Rail  bus_label   VDD1 |  VDD         POWER
4 Buffer_Rail  bus_label   VDD2 |  VDD         POWER
5 Buffer_Rail  signal_name VSS  |  VDD         POWER
[End Interconnect Model]

|The EDA tool connects the terminals and pins as follows:
|
|1 Pins P1 and P2
|2 Pins G1 and G2
|3 PUref of buffers A1 and A2
|4 PUref of buffers A3 and A4
|5 PDref of buffers A1, A2, A3 and A4
```

Keyword: [**End Interconnect Model**]
Required: Yes, for each instance of the [Begin Interconnect Model] keyword
Description: Indicates the end of the Interconnect Model data.
Other Notes: Between the [Begin Interconnect Model] and [End Interconnect Model] keywords is the package model data itself. The data describes any number of interfaces to either IBIS-ISS models or Touchstone files.

Example:

```
[End Interconnect Model]
```

The following keywords should be placed in the specification text near the [Pin Mapping] keyword.

Keyword: **[Bus Label]**

Required: No

Description: Associates a POWER or GROUND signal_name with one or more bus_label names within a Component. Bus_label names can also be associated with specific Pins, Pads or I/O buffer rail terminals. These bus_labels names can be used to define terminals of interconnect subcircuits.

Sub-Params: signal_name

Usage Rules: The first column shall contain a bus_label. The second column, signal_name, gives the data book name for the signal on that bus_label.

The signal_name shall be the signal_name used for a pin under the [Pin] keyword that uses the model_name POWER or GND.

A bus_label may not be the same as any signal_name. Duplicate bus_labels are not permitted. A bus_label may be defined also by the [Pin Mapping] keyword.

Column length limits are:

[Bus Label]	40 characters max
signal_name	40 characters max

Example:

```
[Bus Label] signal_name
VDD1        VDD
VDD2        VDD
VDD3        VDD
VSS1        VSS
VSS2        VSS
```

Keyword: **[Die Supply Pads]**

Required: No

Description: Assigns die pads as supply nodes within a Component. IBIS assumes that for I/O pins (pins that have a Model_name that is not POWER, GND or NC), there is a one-to-one correspondence between a Pin, a Die Pad and the Buffer I/O terminal connection point. There are no such assumptions for POWER and GND pins. A POWER or GND signal_name may have a different number of Pin nodes, die pad nodes and buffer nodes. If the model maker chooses to make separate package and on-die power distribution networks (PDN), then he shall supply a list of nodes (and their associated signal_name) that can be used to mate the package and on-die PDN models.

Sub-Params: None

Usage Rules: Arguments under the [Die Supply Pads] keyword consist of two strings per line, where the strings define a die pad node name and a corresponding signal_name or bus_label, in that order. Signal_names and bus_labels may appear multiple times, but die pad node names may appear only once each under the [Die Supply Pads] keyword.

Other Notes: The data in this section consists of a list of die pad node names and their corresponding signal_names or bus_label that can be used to mate package and on-die PDN networks.

Example:

```
[Die Supply Pads]
VDD1 VDD1
VDD2 VDD
VDD3 VDD
VSS1 VSS
VSS2 VSS
```

Keyword: **[End Die Supply Pads]**
Required: Yes
Description: Indicates the end of the [Die Supply Pads] data.
Other Notes:
Example:

```
[End Die Supply Pads]
```

An IBIS Interconnect Model section may be included in a separate Interconnect file, with the extension ".ict". The Interconnect file shall contain all of the required elements of a normal .ibs file, including [IBIS Ver], [File Name], [File Rev], and the [End] keywords, and at least one [Begin Interconnect Model] and one [End Interconnect Model] keyword. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of the elements follow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .ict file. The .ict file is for IBIS Interconnect Models only. One or multiple Interconnect Models may be included in a .ict file.

The following sections should be appended to the end of the IBIS document.

12 RULES OF PRECEDENCE

The sections below detail the rules of precedence to be assumed by EDA tools and model makers where multiple keywords may support similar functions.

12.1 PACKAGES

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be used by the EDA tool for simulation; any data present in formats numerically lower on the list shall be ignored for that file.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector]