Introduction to Terminals

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* IBIS lumps all of the on-die interconnect for an I/O buffer between the buffer and the die pad into the IBIS [Model] itself.
  + IBIS assume a short between the legacy [Model] I/O terminal and the Die-pad.
  + This is no longer sufficiently accurate at  today’s very high data rates.
* “Interconnect Model” introduces two new keywords [Interconnect Model Selector] and [Interconnect Model Set] that enhances the IBIS package modeling system to be able to accurately simulate broadband, coupled  I/O channels, and Power Delivery.
* We call it “Interconnect Model” because we wanted to satisfy the current way of making package models between buffer and pin, and support models between the buffer and the pin to include separate on-die interconnect and on-package interconnect models.
* We assume the connections at the On-Die/On-Package (Die-Pad) interface is one-to-one for all I/O connections.
* We support having distributed supply rail between different numbers of Pins, Die-Pads, and Buffer Terminals.
* The supply rail connections at the Pins, Die/Package interface can be modeled simply as one SPICE node for all of the Pins and one SPICE node to all of the I/O Buffer rails for that voltage connection, or as a complex power delivery model which has separate terminal for each pin, die-pad and Buffer. This adds complexity to describing supply rail terminals.
* Ultimately, Interconnect Models are either IBIS-ISS subckts, or Touchstone files. Each [Interconnect Model] points to the name of the IBIS-ISS file/subckt or Touchstone file, and how the terminals of the model need to be connected.

The Terminal section of an Interconnect Model describes how the terminals of an Interconnect Model subckt or Touchstone file instance in a SPICE deck need to be connected at a buffer terminal, die-pad interface or pin/board interface. Package models on pin records and [Define Package Model] are between the pins of the component and the I/O buffer in the silicon. The model  between the pins of the component and the I/O buffer in the silicon can either be in a single Interconnect Model, or can be split into Interconnect Models between the pins of the component and the die-pad interface, and Interconnect Models between the die-pad interface and the I/O buffers.

The sub-parameter Number\_of\_terminals tells how many SPICE nodes are required on the instance in the SPICE deck.

The terminal lines that follow this keyword describe what SPICE node each terminal should be connected to.

* The first field <Terminal\_number> is a number between 1 and the <Number\_of\_terminals> that describes the ordinal (positional) number of the SPICE node in the [Interconnect Model] subckt or Touchstone file instance.
* The SPICE nodes are either I/O connections or on supply-rail connections.
  + I/O connections are to pins that have a Model\_name that is not POWER, GND or NC. Each I/O connection is specified using Pin\_name.
    - Each Pin\_name has only one die-pad and one I/O buffer terminal (in this specification).
  + A supply-rail connection is to a signal\_name of a pin that has model\_name POWER or GND.
    - Interconnect models for rail connections can either be made to a specific pin, die-pad or I/O buffers, or can be made to all of the pins, die-pads or I/O buffers that have connects to that supply-rail signal\_name, or can be made to a subset of the pins, die-pads or I/O buffers that have the same bus\_label.

The second and third required fields of the terminal record are the <terminal\_type> and < Terminal\_type\_qualifier >.

* For I/O terminals
  + The <terminal\_type> determines if the terminal is at the Buffer, Die-Pad or Pin
  + The <Terminal\_type\_qualifier > must be a pin\_name.
* For supply-rail terminals
  + At the Pin/Board interface
    - Pin\_name
    - Signal\_name
    - Bus\_label subset of a Signal\_name
  + At the Die-Pad interface
    - Die\_pad\_name
    - Signal\_name
    - Bus\_label subset of a Signal\_name
  + At the buffer
    - Pin\_name
      * A specific rail (e.g. Power\_clamp\_ref)
    - Signal\_name
    - Bus\_label subset of a Signal\_name

Crosstalk simulations require Interconnect Models have connections to multiple I/O Pin\_names.

* It is often impractical to make Interconnect Models that include all of the I/O connections in a component.
* A DQ bus on a memory controller can easily contain 128 pins, and a fully coupled s-parameter would have 256 ports.
* This specification also supports subset of the complete package model
* An example is a model with the interconnect of DQ6, DQ7 and DQ8.
  + DQ7 has crosstalk in the package with the adjoining signals DQ6 and DQ8.
    - This model represents all of the crosstalk on DQ7 (since it includes DQ6 and DQ8).
  + This model does not include all of the crosstalk affecting DQ8 since the model does not include DQ9.
  + Similarly DQ6 does not include all of its aggressors (DQ5).
  + The model maker tells the EDA tool that connections to terminals DQ6 and DQ8 do not include all of their aggressors by adding the optional field “Aggressor” to their terminals. (Not suitable for victim: Aggressor\_Only, Non\_Victim)
  + In this case, simulations will include coupling on DQ6 and DQ8 from DQ7, but it will not include coupling from their aggressors (DQ5 and DQ9).
  + The DQ7 connections do not have the optional “Aggressor” field. The EDA tool may assume that DQ7 has all (or more practically most of) the coupling to its aggressor connections.