On-Die Modeling

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IBIS-Interconnect

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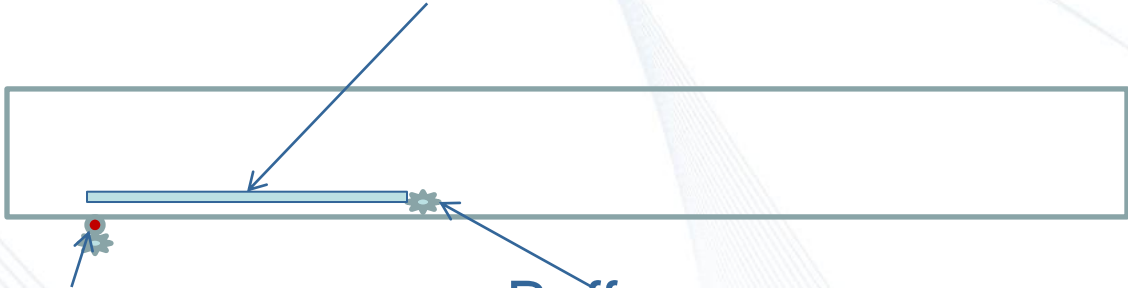*We Are Signal Integrity*

Overview

- History of Presentations
- Assumption is that the EMD concepts can satisfy the needs of the IBIS community from Die to Die
- On-Die Models
- IBIS 5.1 Limitation
- The IC Vendor Needs to Partition the 5.1 Buffer into a IBIS-ISS or Tstonefile On-Die Interconnect and a Different 6.0 Buffer
- Conclusion

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History of Presentations

- Package EBD/EMD
  - http://www.eda.org/ibis/adhoc/interconnect/Package_EBD_EMD.pptx
- Electronic Module Description Specification, Draft 0
  - http://www.eda.org/ibis/adhoc/interconnect/EMD.docx
- Die-to-Die Connections in EMD
  - http://www.eda.org/ibis/adhoc/interconnect/Die2Die.pdf
- MCP and EMD ...
  - E-Mail sent Fri 12/14/2012 12:39 PM

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On-Die Models

On-Die Interconnect (RDL or T-coil)

Buffer
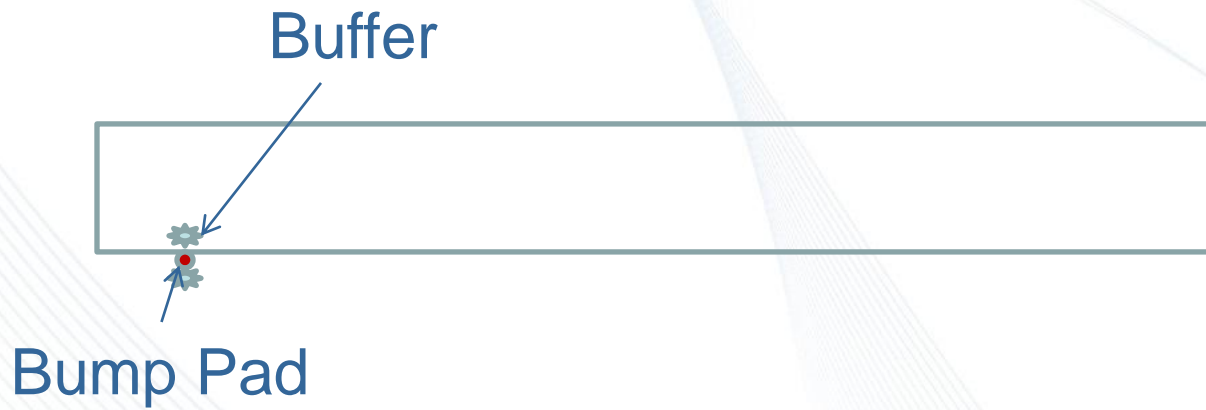
Bump Pad

IBIS 5.1 Limitation

Buffer

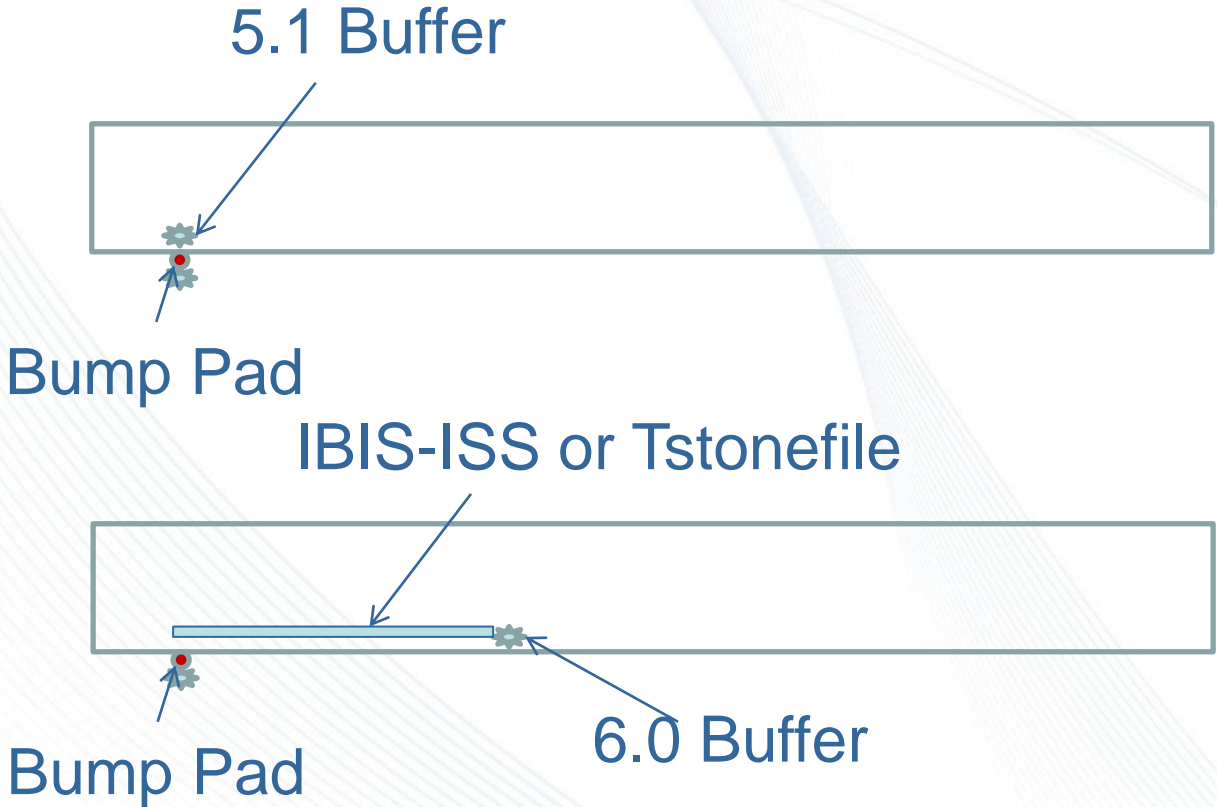Bump Pad

The IC Vendor Needs to Partition the 5.1 Buffer into a IBIS-ISS or Tstonefile On-Die Interconnect and a Different 6.0 Buffer

5.1 Buffer

Bump Pad

IBIS-ISS or Tstonefile

6.0 Buffer

Bump Pad

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For AMI Modeling …

- The IC Vendor most likely partition the On-Die Interconnect and Buffer at a point where he can use a Legacy IBIS [Model] and a Tstonefile for the On-Die Interconnect

- The Legacy IBIS [Model] should be LTI
  - Rx Power Clamp and Ground Clamp are linear
    - Can be represented by an R to ground
  - Tx Pullup and Pulldown Curves are linear and same slope
    - Can be represented by a Voltage Swing, Series Impedance, and a Rise Time

- On-Die Interconnect may be associated with [Model] instead of [Pin]

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For Non AMI Modeling

- The IC Vendor most likely partition the On-Die Interconnect and Buffer at a point where he can use a Legacy IBIS [Model] and a Tstonefile for the On-Die Interconnect

- The Legacy IBIS [Model] has no constraints
  - C_comp will be smaller because it should not include the capacitance in the On-Die Interconnect
  - IV curves will be different because they do on include the resistance in the On-Die Interconnect

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Conclusion

This presentation should at least help us use a common language and understanding of how to partition the On-Die Interconnect and Buffer modeling.

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