Proposed Package Implementations By Pin Number

```
[Define Package Model]  Diff_1_2
Language IBIS-ISS
Corner  Typ  Package.iss  Diff_Pins_typ_1_2
Corner  Min  Package.iss  Diff_Pins_min_1_2
Corner  Max  Package.iss  Diff_Pins_max_1_2
Parameters  Td 99ps
Parameters  Zo 51
Ports  Pin.1  Pin.2  Pad.1  Pad.2
[End Package Model]

[ISS Package Model]  Diff_1_2
Corner  Typ  Package.iss  Diff_Pins_typ_1_2
Corner  Min  Package.iss  Diff_Pins_min_1_2
Corner  Max  Package.iss  Diff_Pins_max_1_2
Parameters  Td 99ps
Parameters  Zo 51
Ports  Pin.1  Pin.2  Pad.1  Pad.2
[End ISS Package Model]
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-------------------------------------------------------------
|
[Define Package Model]  A_differential_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Another Noname Package Company, Inc.
[Description]           Illustration package model
[Number Of Pins]  2
|
[Pin Numbers]
  1   DiePort = IDP_1
  2   DiePort = IDP_2
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  Package.iss  Diff_Pins_1_2
|
| Parameters List of parameters
Parameters  Td = 99ps
Parameters  Zo = 51
|
| Ports are in same order as defined in SPICE
Ports  1  2  IDP_1  IDP_2
|
[End Package Circuit]
[End Package Model]
```

What is being re-used in [Define Package Model]

Blue Not Used Red Used

```
| |-- [Define Package Model]
| |  ----------------------
| |    |-- [Manufacturer]
| |    |-- [OEM]
| |    |-- [Description]
| |    |-- [Number Of Sections]
| |    |-- [Number Of Pins]
| |    |-- [Pin Numbers]              Len, L, R, C, Fork, Endfork
| |    |-- [Model Data]
| |    |  ------------
| |    |    |-- [Resistance Matrix]     Banded_matrix, Sparse_matrix,
| |    |    |  -------------------      Full_matrix
| |    |    |    |-- [Bandwidth]
| |    |    |    |-- [Row]
| |    |    |-- [Inductance Matrix]     Banded_matrix, Sparse_matrix,
| |    |    |  -------------------      Full_matrix
| |    |    |    |-- [Bandwidth]
| |    |    |    |-- [Row]
| |    |    |-- [Capacitance Matrix]    Banded_matrix, Sparse_matrix,
| |    |    |  -------------------      Full_matrix
| |    |    |    |-- [Bandwidth]
| |    |    |    |-- [Row]
| |    |    |-- [End Model Data]
| |    |-- [End Package Model]]
```

IBIS .pkg file:

```
|-------------------------------------------------------------
| This example implements a package model using an IBIS-ISS
| subcircuit.
|-------------------------------------------------------------
|
[Define Package Model]  A_differential_pkg_model
[Manufacturer]          Noname Company, Inc.
[OEM]                   Another Noname Package Company, Inc.
[Description]           Illustration package model
[Number Of Pins]  2
|
[Pin Numbers]
  1   DiePort = IDP_1
  2   DiePort = IDP_2
|
[Package Circuit]
Language IBIS-ISS
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner  Typ  Package.iss  Diff_Pins_1_2
|
| Parameters List of parameters
Parameters  Td = 99ps
Parameters  Zo = 51
|
| Ports are in same order as defined in SPICE
Ports  1  2  IDP_1  IDP_2
|
[End Package Circuit]
[End Package Model]
```

Proposed Package Implementations By Pin Number

```
[ISS Package Model]  Diff_1_2
Corner  Typ  Package.iss  Diff_Pins_typ_1_2
Corner  Min  Package.iss  Diff_Pins_min_1_2
Corner  Max  Package.iss  Diff_Pins_max_1_2
Parameters  Td 99ps
Parameters  Zo 51
Ports  Pin.1  Pin.2  Pad.1  Pad.2
[End Package Model]
|
[ISS Package Model]  SE_13
Corner  Typ  Package.iss  SE_typ
Parameters  Td 99ps
Parameters  Zo 51
Ports  Pin.13 Pad.13
[End Package Model]
|
[ISS Package Model]  SE_14
Corner  Typ  Package.iss  SE_typ
Parameters  Td 80ps
Parameters  Zo 51
Ports  Pin.14 Pad.14
[End Package Model]
```

IBIS .ibs file

```
[Pins]
1 Tx1H My_Tx na na na
2 Tx1L My_Tx na na na
3 Tx2H My_Tx na na na
4 Tx2L My_Tx na na na
5 Tx3H My_Tx na na na
6 Tx3L My_Tx na na na
7 Vdd Power
8 Vdd Power
9 Vdd Power
10 Vqq Ground
11 Vqq Ground
12 Vqq Ground
13 DQ 1 DQ
14 DQ2 DQ
```

Proposed Package Implementations Coupled By Pin Number

```
[ISS Package Model]  Coupled
Corner  Typ  Package.iss  Coupled
Ports  Pin.1 Pin.2 Pin.3 Pin.4 Pin.5 Pin.6
Ports  Pad.1 Pad.2 Pad.3 Pad.4 Pad.5 Pad.6
[End Package Model]

[ISS Package Model]  Coupled_Power
Corner  Typ  Package.iss  Coupled_Power
Ports  Pin.1 Pin.2 Pin.3 Pin.4 Pin.5 Pin.6
Ports  Pad.1 Pad.2 Pad.3 Pad.4 Pad.5 Pad.6
Ports  Pin.7 Pad.7 Pin.10 Pad.10
[End Package Model]
```

IBIS .ibs file

[Pins]

1 Tx1H My_Tx na na na
2 Tx1L My_Tx na na na
3 Tx2H My_Tx na na na
4 Tx2L My_Tx na na na
5 Tx3H My_Tx na na na
6 Tx3L My_Tx na na na
7 Vdd Power
8 Vdd Power
9 Vdd Power
10 Vqq Ground
11 Vqq Ground
12 Vqq Ground
13 DQ 1 DQ
14 DQ2 DQ

Proposed Package Implementations By [Model]

```
[ISS Package Model] My_Tx_Diff
Corner  Typ  Package.iss  Diff_Tx
Parameter Tstonefile  AMI(Tstonefile)
Ports  pin.H Pad.H Pin.L Pad.H
[End Package Model]
|
[ISS Package Model] My_Tx_Coupled_Diff
Corner  Typ  Package.iss  Coupled_Tx
Ports  Pin.H1 Pin.L1 Pin.HV Pin.LV Pin.H2 Pin.L2
Ports  Pad.H1 Pad.L1 Pad.HV Pad.LV Pad.H2 Pad.L2
[End Package Model]
|
[ISS Package Model] My_Rx_Diff
Corner  Typ  Package.iss  Diff_Rx
Parameter Tstonefile  AMI(Tstonefile)
Ports  pin.H Pad.H Pin.L Pad.H
[End Package Model]
|
[ISS Package Model] My_Rx_Coupled_Diff
Corner  Typ  Package.iss  Coupled_Rx
Ports  Pin.H1 Pin.L1 Pin.HV Pin.LV Pin.H2 Pin.L2
Ports  Pad.H1 Pad.L1 Pad.HV Pad.LV Pad.H2 Pad.L2
[End Package Model]
```

IBIS .ibs file

```
[Model] My_Tx
[Algorithmic Model]
Executable Windows_VS9.0_32 My_Tx.dll My_Tx.ami
[End Algorithmic Model]
[Diff ISS Package Model] My_Tx_Diff
[Coupled Diff ISS Package Model] My_Tx_Coupled_Diff
|
[Model] My_Rx
[Algorithmic Model]
Executable Windows_VS9.0_32 My_Rx.dll My_Rx.ami
[End Algorithmic Model]
[Diff ISS Package Model] My_Rx_Diff
[Coupled Diff ISS Package Model] My_Rx_Coupled_Diff
|
…
```

Proposed Package Implementations With Power

```
[ISS Package Model]  Coupled
Corner  Typ  Package.iss  Coupled
Ports  Pin.1 Pin.2 Pin.3 Pin.4 Pin.5 Pin.6
Ports  Pad.1 Pad.2 Pad.3 Pad.4 Pad.5 Pad.6
Ports  Pin.7 pin.8 pin.9 Pad.7
Ports  Pin.10 Pin.11 Pin.12 Pad.10
[End Package Model]
```

IBIS .ibs file

```
[Pins]
1 Tx1H My_Tx na na na
2 Tx1L My_Tx na na na
3 Tx2H My_Tx na na na
4 Tx2L My_Tx na na na
5 Tx3H My_Tx na na na
6 Tx3L My_Tx na na na
7 Vdd Power
8 Vdd Power
9 Vdd Power
10 Vqq Ground
11 Vqq Ground
12 Vqq Ground
```

Proposed Package Implementations
Two Pins, One Buffer

```
[ISS Package Model]  Coupled
Corner  Typ  Package.iss  Coupled
Ports  Pin.1 Pin.2 Pad.1
[End Package Model]
```

IBIS .ibs file

```
[Pins]
1 Tx1 My_Tx na na na
2 Tx1 My_Tx na na na
```

Proposed Package Implementations
EBD, DDR3 Fly By Clock

```
[ISS Package Model]  Clock
Corner  Typ  Package.iss  Clock
Ports  Pin.1 Pin.2
Ports  Pin.U1.8 Pin.U1.9
Ports  Pin.U2.8 Pin.U2.9
Ports  Pin.U3.8 Pin.U3.9
Ports  Pin.U4.8 Pin.U4.9
Ports  Pin.U5.8 Pin.U5.9
Ports  Pin.U6.8 Pin.U6.9
Ports  Pin.U7.8 Pin.U7.9
Ports  Pin.U8.8 Pin.U8.9
[End Package Model]
```

IBIS .ebd file

```
[Pins]
1 Tx1H My_Tx na na na
2 Tx1L My_Tx na na na

[Connection] ClkH
Pins Pin.1
Pins Pin.U1.8 Pin.U2.8 Pin.U3.8 Pin.U4.8
Pins Pin.U5.8 Pin.U6.8 Pin.U7.8 Pin.U8.8
[End Connection]

[Connection] ClkL
Pins Pin.2
Pins Pin.U1.9 Pin.U2.9 Pin.U3.9 Pin.U4.9
Pins Pin.U5.9 Pin.U6.9 Pin.U7.9 Pin.U8.9
[End Connection]

U1 my_ibis.ibs my_ibis
U2 my_ibis.ibs my_ibis
U3 my_ibis.ibs my_ibis
U4 my_ibis.ibs my_ibis
U5 my_ibis.ibs my_ibis
U6 my_ibis.ibs my_ibis
U7 my_ibis.ibs my_ibis
U8 my_ibis.ibs my_ibis
```