**13.7 ADDITIONAL EMD MODEL EXAMPLES**

*Examples:*

The example below for a simplified DIMM includes pins at the EMD interface and at the designator interfaces of two memory components. Three EMD Groups provide EMD Model options including one option with no crosstalk and two options with crosstalk included. The EMD Groups with crosstalk included show use of IBIS-ISS or Touchstone files, and the rail connections are modeled in separate EMD Sets that are included in each EMD Group. The rail terminals are connected by either bus\_label or signal\_name. Bus\_labels are used to split the VDD rail into VDD1 and VDD2 buses. While only one VSS rail is shown, separate VSS rails could exist (for example, VSS1 and VSS2) and would be included by using bus\_label syntax.

[Begin EMD] DIMM

[Number of EMD Pins] 9

[EMD Pin List] signal\_name signal\_type bus\_label

A1 DQ0

A2 DQ1

A3 DQ2

A4 DQ3

P1 VDD POWER VDD1

P2 VDD POWER VDD2

G1 VSS GND

[End EMD Pin List]

[EMD Parts]

ACME\_MEM mem.ibs MEMx4

[End EMD Parts]

[EMD Designator List]

U1 ACME\_MEM

U2 ACME\_MEM

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.1 VDD POWER VDD1

U1.2 VDD POWER VDD2

U1.3 VSS GND

U1.4 VSS GND

U1.5 DQ0

U1.6 DQ1

U1.7 DQ2

U1.8 DQ3

|

U2.1 VDD POWER VDD1

U2.2 VDD POWER VDD2

U2.3 VSS GND

U2.4 VSS GND

U2.5 DQ0

U2.6 DQ1

U2.7 DQ2

U2.8 DQ3

[End Designator Pin List]

| EMD Group has no crosstalk modeled and includes the

| rails in the same IBIS-ISS subcircuit

[EMD Group] All\_DQs\_No\_Coupling\_Rails

All\_DQs\_Uncoupled NA

[End EMD Group]

| EMD Group models crosstalk with IBIS-ISS subcircuits

[EMD Group] All\_DQs\_Aggressor\_Options\_ISS

All\_DQs\_Crosstalk\_ISS NA

Rails\_ISS NA

[End EMD Group]

| EMD Group models crosstalk with Touchstone files

[EMD Group] All\_DQs\_Aggressor\_Options\_TS

All\_DQs\_Crosstalk\_TS NA

Rails\_TS NA

[End EMD Group]

[End EMD] | End of [Begin EMD]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* EMD Sets \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

[EMD Set] All\_DQs\_Uncoupled

[EMD Model] DQ0\_3

File\_IBIS-ISS DQ.iss DQ

Number\_of\_terminals = 20

1 Pin\_I/O pin\_name A1 | DQ0

2 Pin\_I/O pin\_name A2 | DQ1

3 Pin\_I/O pin\_name A3 | DQ2

4 Pin\_I/O pin\_name A4 | DQ3

5 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

6 Pin\_Rail signal\_name VSS | EMD Pin G1

|

7 Pin\_I/O pin\_name U1.5 | DQ0

8 Pin\_I/O pin\_name U1.6 | DQ1

9 Pin\_I/O pin\_name U1.7 | DQ2

10 Pin\_I/O pin\_name U1.8 | DQ3

11 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

12 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

13 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

14 Pin\_I/O pin\_name U2.5 | DQ0

15 Pin\_I/O pin\_name U2.6 | DQ1

16 Pin\_I/O pin\_name U2.7 | DQ2

17 Pin\_I/O pin\_name U2.8 | DQ3

18 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

19 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

20 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] All\_DQs\_Crosstalk\_ISS

| EMD Model includes all crosstalk contributions for DQ1.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ1\_Victim

File\_IBIS-ISS DQ.iss DQ1\_Victim

Number\_of\_terminals = 15

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

2 Pin\_I/O pin\_name A2 | DQ1

3 Pin\_I/O pin\_name A3 Aggressor\_Only | DQ2

4 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

5 Pin\_Rail signal\_name VSS

|

6 Pin\_I/O pin\_name U1.5 | DQ0

7 Pin\_I/O pin\_name U1.6 | DQ1

8 Pin\_I/O pin\_name U1.7 | DQ2

9 Pin\_I/O pin\_name U1.8 | DQ3

10 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

11 Pin\_I/O pin\_name U2.5 | DQ0

12 Pin\_I/O pin\_name U2.6 | DQ1

13 Pin\_I/O pin\_name U2.7 | DQ2

14 Pin\_I/O pin\_name U2.8 | DQ3

15 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

| EMD Model includes all crosstalk contributions for DQ2.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ2\_Victim

File\_IBIS-ISS DQ.iss DQ2\_Victim

Number\_of\_terminals = 15

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

2 Pin\_I/O pin\_name A2 Aggressor\_Only | DQ1

3 Pin\_I/O pin\_name A3 | DQ2

4 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

5 Pin\_Rail signal\_name VSS

|

6 Pin\_I/O pin\_name U1.5 | DQ0

7 Pin\_I/O pin\_name U1.6 | DQ1

8 Pin\_I/O pin\_name U1.7 | DQ2

9 Pin\_I/O pin\_name U1.8 | DQ3

10 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

11 Pin\_I/O pin\_name U2.5 | DQ0

12 Pin\_I/O pin\_name U2.6 | DQ1

13 Pin\_I/O pin\_name U2.7 | DQ2

14 Pin\_I/O pin\_name U2.8 | DQ3

15 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] Rails\_ISS

[EMD Model] Power\_Rails

File\_IBIS-ISS Power\_Rails.iss Rails

Number\_of\_terminals = 8

1 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

2 Pin\_Rail signal\_name VSS | EMD Pin G1

|

3 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

4 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

5 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

6 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

7 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

8 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] All\_DQs\_Crosstalk\_TS

| EMD Model includes all crosstalk contributions for DQ1.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ1\_Victim

File\_TS DQ1\_Victim.ts

Unused\_port\_termination Reference

Number\_of\_terminals = 25

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

3 Pin\_I/O pin\_name A2 | DQ1

5 Pin\_I/O pin\_name A3 Aggressor\_Only | DQ2

7 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

|

9 Pin\_I/O pin\_name U1.5 | DQ0

11 Pin\_I/O pin\_name U1.6 | DQ1

13 Pin\_I/O pin\_name U1.7 | DQ2

15 Pin\_I/O pin\_name U1.8 | DQ3

|

17 Pin\_I/O pin\_name U2.5 | DQ0

19 Pin\_I/O pin\_name U2.6 | DQ1

21 Pin\_I/O pin\_name U2.7 | DQ2

23 Pin\_I/O pin\_name U2.8 | DQ3

|

25 A\_gnd | Reference for all ports

[End EMD Model]

| EMD Model includes all crosstalk contributions for DQ2.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ2\_Victim

File\_TS DQ2\_Victim.ts

Unused\_port\_termination Reference

Number\_of\_terminals = 25

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

3 Pin\_I/O pin\_name A2 Aggressor\_Only | DQ1

5 Pin\_I/O pin\_name A3 | DQ2

7 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

|

9 Pin\_I/O pin\_name U1.5 | DQ0

11 Pin\_I/O pin\_name U1.6 | DQ1

13 Pin\_I/O pin\_name U1.7 | DQ2

15 Pin\_I/O pin\_name U1.8 | DQ3

|

17 Pin\_I/O pin\_name U2.5 | DQ0

19 Pin\_I/O pin\_name U2.6 | DQ1

21 Pin\_I/O pin\_name U2.7 | DQ2

23 Pin\_I/O pin\_name U2.8 | DQ3

|

25 A\_gnd | Reference for all ports

[End EMD Model]

[End EMD Set]

[EMD Set] Rails\_TS

[EMD Model] Power\_Rails

File\_TS Power\_Rails\_TS.s8p

Number\_of\_terminals = 9

1 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

2 Pin\_Rail signal\_name VSS | EMD Pin G1

|

3 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

4 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

5 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

6 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

7 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

8 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

|

9 A\_gnd | Reference for all ports

[End EMD Model]

[End EMD Set]