**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: 198.1**

**ISSUE TITLE:** Keyword additions for On-Die PDN (Power Distribution Network) Modeling

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**DATE ACCEPTED:**

**DEFINITION OF THE ISSUE:**

To resolve the power-supply noise issue, especially high frequency range, On-die decoupling capacitor should be taken account into the simulation. With current IBIS versions, On-die PDN model can be defined by using the keyword [Series Pin Mapping] and “Model\_type Series”.

However, this method seems not to be widely recognized, because the keyword [Series Pin Mapping] and “Model\_type Series” don’t remind one of description of the On-die PDN model. To ease usage of On-die PDN model in the IBIS model, this BIRD proposes to add the new keywords [PDN Domain], [End PDN Domain], [PDN Model], and [End PDN Model] for On-Die PDN model.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Provide On-Die decoupling capacitor model and series resistance model and leakage current model
 |  |
| 1. Describe power node and ground node at die pad
 |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table 2: IBIS Keywords, Sub-parameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
|  [PDN Domain] and [End PDN Domain] under [Component] | New |  |
| “Signal\_name” and “Bus\_label” under [PDN Domain] | New |  |
| [PDN Model] and [End PDN Model] under [PDN Domain] | New |  |
| “C\_pdn”, “R\_pdn” and “R\_leak” under [PDN Model] | New |  |

**PROPOSED CHANGES:**

All page numbers refer to the PDF version of IBIS Version 7.0.

1. In IBIS version 7.0, insert the [PDN Domain], [End PDN Domain], [PDN Model] and [End PDN Model] keywords after [End Interconnect Model Group] keyword on Page.37.

*Keyword:* [PDN Domain], [End PDN Domain]

*Required:* No

*Description:* Marks the beginning and end of an PDN Domain description that is used to specify the two nodes at die pad that joined by On-die PDN model. The two nodes shall be specified by bus\_label and/or signal\_name sub-parameters. A simulation may contain one On-die PDN model listed in one [PDN Domain]. The [PDN Domain]/[End PDN Domain] keyword pair is hierarchically scoped by the [Component] keyword.

*Sub-Params:* Bus\_label, Signal\_name

*Usage Rules:* [PDN Domain] has a single argument, which is the name of the associated PDN Domain. The length of the PDN Domain name shall not exceed 40 characters. Blank characters are not allowed. [Component] may contain zero or more [PDN Domain] keywords (identified by a name).

Each [PDN Domain] shall contain at least one [PDN Model] keyword and two sub-parameters that consists of bus\_label, signal\_name or both of them. If there are no [PDN Model] keyword, the [PDN Domain] keyword is illegal. If there are less than two or more than two bus\_label and/or Signal\_name, the [PDN Domain] keyword is illegal.

Bus\_label rules:

Bus\_label sub-parameter has one entry. A bus\_label that are associated POWER or GND pin can be used as the entry. Each bus\_label shall match the bus\_labels declared in the [Pin], [Pin Mapping], [Bus Label], or [Die Supply Pads] section of the .ibs file. If there are two or more die pads associated with the bus\_label, the die pads shall be considered as shorted.

Signal\_name rules:

Signal\_name sub-parameter has one entry. A signal\_name that are associated POWER or GND pin can be used as the entry. Each signal\_name shall match the signal\_names declared in the [Pin] section of the .ibs file. If there are two or more die pads associated with the signal\_name, the die pads shall be considered as shorted. In addition, if there are two or more die pads associated with the signal\_name and the signal\_name is associated with two or more bus\_labels, the die pads shall be considered as shorted.

A bus\_label and a signal\_name may appear on more than one entry under different [PDN Domain]. This allows for multiple and different On-die PDN models to be placed between any arbitrary Pad\_Rail pair combinations. It is not allowed using nodes that include the same pin in a [PDN Domain].

Note that it is allowed two or more [PDN Domain] to be placed between two nodes. In this case, all [PDN Domain]s are connected in parallel in a simulation. (cf. Only one [PDN model] is used, multiple [PDN model]s are defined in [PDN Domain].

Note that a bus\_label or signal\_name that does not have the path to the buffer rail terminals can be listed under the [PDN Domain] keyword. In this case the On-die PDN models can be used for power integrity (PI) analysis such as core power.

*Examples:*

| PDN 1

[PDN Domain] PDN\_X

Bus\_label VCC1 | VCC1 includes A1 and A2 pins.

Signal\_name VSS

[PDN model] PDN\_model\_A

C\_pdn 15n 20n 5n

R\_pdn 5m 5m 10m

R\_leak 11k 10k 8k

[End PDN model]

[End PDN Domain]

| PDN 2

[PDN Domain] PDN\_Y

Signal\_name VCC2 | VCC2 includes A1, A2 and B1 pins.

Signal\_name VSS

| Note: Bus\_label VCC1 and Signal\_name VCC2 shall not be defined

| under the same PDN Domain, because A1 and A2 pins associated

| with both.

| Note: A1, A2 and B1 pins are considered as shorted at die pads

| in a simulation when the PDN model under PDN\_Y is enable.

| pin(signal\_name) pad(bus\_label)

| A1(VCC2) ----------+(VCC1)

| | be considered as shorted by PDN\_X & PDN\_Y

| A2(VCC2) ----------+(VCC1)

| | be considered as shorted by PDN\_Y

| B1(VCC2) ----------+(VCC2)

|

| C1(VSS) ----------+(VSS)

[PDN model] PDN\_model\_B

C\_pdn 1.1n 1.5n 1.8n

R\_pdn 46m 55m 60m

R\_leak 290k 300k 300k

[End PDN model]

[End PDN Domain]

| PDN 3

[PDN Domain] PDN\_for\_VCC1\_MIM

Bus\_label VCC1 | VCC1 includes A1 and A2 pins.

Signal\_name VSS

| Note: This [PDN Domain] has the same nodes as PDN\_X.

| In this case, a simulation may contain multiple On-die PDN

| models between VCC1 and VSS when the PDN models under PDN\_X and

| PDN\_for\_VCC1\_MIM are both enable.

[PDN model] PDN\_model\_MIM

C\_pdn 23n 23n 23n

R\_pdn 5m 5m 5m

R\_leak 27k 27k 27k

[End PDN model]

[End PDN Domain]

*Keyword:* [PDN Model], [End PDN Model]

*Required:* Yes, for each instance of the [PDN Domain] keyword

*Description:* Marks the beginning and end of a PDN Model description that is used to define the On-die PDN model. An On-die PDN model has two ports that connected the nodes specified by [PDN Domain]. On-die PDN model is consists of three RC values. These values represent MOS capacitor, MIM capacitor, metal resistance, parasitic RC, leakage current, etc. The [PDN Model]/[End PDN Model] keyword pair is hierarchically scoped by the [PDN Domain] keyword.

*Sub-Params:* R\_pdn, C\_pdn, R\_leak

*Usage Rules:* [PDN Model] has a single argument, which is the name of the associated PDN Model. The length of the PDN Model name shall not exceed 40 characters in length. Blank characters are not allowed. [PDN Domain] shall contain one or more [PDN Model] keywords (identified by a name). Each [PDN Model] shall contain R\_pdn, C\_pdn and R\_leak sub-parameters. If any one of these sub-parameters are lacking, the [PDN Model] keyword is illegal.

EDA tool may disable all [PDN Model]s that are contained in a [PDN Domain]. If two or more [PDN Model]s are contained in one [PDN Domain], EDA tool may select one of them. The first [PDN Model] entry under the [PDN Domain] keyword shall be considered the default by the EDA tool.

For each of sub-parameters, the three columns hold the three values whose order does not depend on magnitude. The three entries shall be placed on a single line and shall be separated by at least one whitespace character. All three values are required for these sub-parameters. C\_pdn and R\_pdn shall be non-negative numbers (positive or zero). R\_leak shall be positive numbers (zero is not allowed). If a value of C\_pdn is zero, EDA tool may ignore it. “NA” is allowed for the second and third column only. If the second and/or third column value is NA, then the EDA tool shall use the first column value for simulation.

The electrical circuit model for three sub-parameters is shown in Figure 1. Port1 is connected to a node that is defined by the first Bus\_label or Signal\_name sub-parameter under the [PDN Domain]. Port2 is connected to a node that is defined by the second Bus\_label or Signal\_name sub-parameter under the [PDN Domain].



Figure 1 [PDN Model] circuit

Note that EDA tool may select one column from typical, minimum or maximum data when .ibs file is used. At the same time, the same column of [PDN Model] may be selected. However, it is not necessarily that On-die PDN model characteristics depend on the variations of the buffer such as voltage, temperature and process variations. For example, MIM capacitor hardly depends on them. In such cases, model maker may use the same three values for the entry of [PDN Model] sub-parameters. In addition, On-die PDN model characteristics can depend on many technologies other than the variation of the buffer. For example, On-die capacitance of gated power supply can vary due to the state of gate. In such cases, model maker may descript multiple [PDN Model]s in one [PDN Domain]. Based on the condition assumed by the user, EDA tool may select one of them.

Note that the Interconnect Model and Series Model can also represent On-die PDN characteristic and can be exist with [PDN Model], but model maker should make sure that On-die PDN characteristic is not double counted.

Note that when the [PDN Model] is used together with the Interconnect Model that does not have die pad (pin to buffer, pin only or buffer only interface), there is no connection between them at die pad. (e.g. When an Interconnect model is intended for use in pin to buffer rail path and a [PDN Model] is intended for used for die pad to die pad AC path of the rail, the [PDN Model] does not affect the I/O buffer against model maker’s will.)

*Examples:*

[PDN Domain] PDN\_for\_VDDQ

Bus\_label VDDQ | VDDQ is IO power supply for DDR3/4 combo PHY.

Signal\_name VSS

[PDN Model] DDR3

|VDDQ [Voltage Range] 1.5 1.425 1.575

|[Temperature]   25    125   -40

|MOS TT   SS    FF

C\_pdn 5n 4n 6n

R\_pdn 20m 30m 10m

R\_leak 15k 17k 11k

[End PDN Model]

[PDN Model] DDR4

|VDDQ [Voltage Range] 1.2 1.14 1.26

|[Temperature]     25    125   -40

|MOS TT   SS    FF

C\_pdn 1.5n 1n 1.8n

R\_pdn 20m 30m 10m

R\_leak 15k 17k 11k

[End PDN Model]

[End PDN Domain]

[PDN Domain] MOS\_capacitor\_for\_VCC

Bus\_label VCC

Signal\_name VSS

[PDN Model]

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     200n 150n 250n

R\_pdn      3m 4m 1m

R\_leak     5k 8k 2k

[End PDN Model]

[End PDN Domain]

[PDN Domain] MIM\_capacitor\_for\_VCC

Bus\_label VCC

Signal\_name VSS

| MIM does not depend on MOS PVT variations,

| but intermetal dielectric and metal variations.

[PDN Model] Medium\_MIM

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     70n 70n 70n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1g 1g 1g | R\_leak: Open

[End PDN Model]

[PDN Model] Large\_MIM

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     72n 72n 72n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1g 1g 1g | R\_leak: Open

[End PDN Model]

[PDN Model] Small\_MIM

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     67n 67n 67n

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1g 1g 1g | R\_leak: Open

[End PDN Model]

[End PDN Domain]

[PDN Domain] Gated\_area\_for\_VCC

Bus\_label VCC

Signal\_name VSS

[PDN Model] Gate\_off

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     0n 0n 0n | C\_pdn: zero (ignored)

R\_pdn      0 0 0 | R\_pdn: Short

R\_leak     1g 1g 1g | R\_leak: Open

[End PDN Model]

[PDN Model] Gate\_on

|VCC [Voltage Range] 0.9 0.84 0.96

|[Temperature]    25    125   -40

|MOS TT   SS    FF

C\_pdn     21n 18n 22n

R\_pdn      15m 18m 11m

R\_leak     17k 20k 14k

[End PDN Model]

[End PDN Domain]

**BACKGROUND INFORMATION/HISTORY:**

This proposal has been discussed in JEITA LPB-SC Modeling WG.

Kazuki Murata (Ricoh) proposed in IBIS summit Japan 2017.

Kazuki Murata (Ricoh) presented in LPB Forum 2018.

Megumi Ono (Socionext) proposed in DesignCon 2019 IBIS summit.

Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation) proposed in DesignCon 2020 IBIS summit.