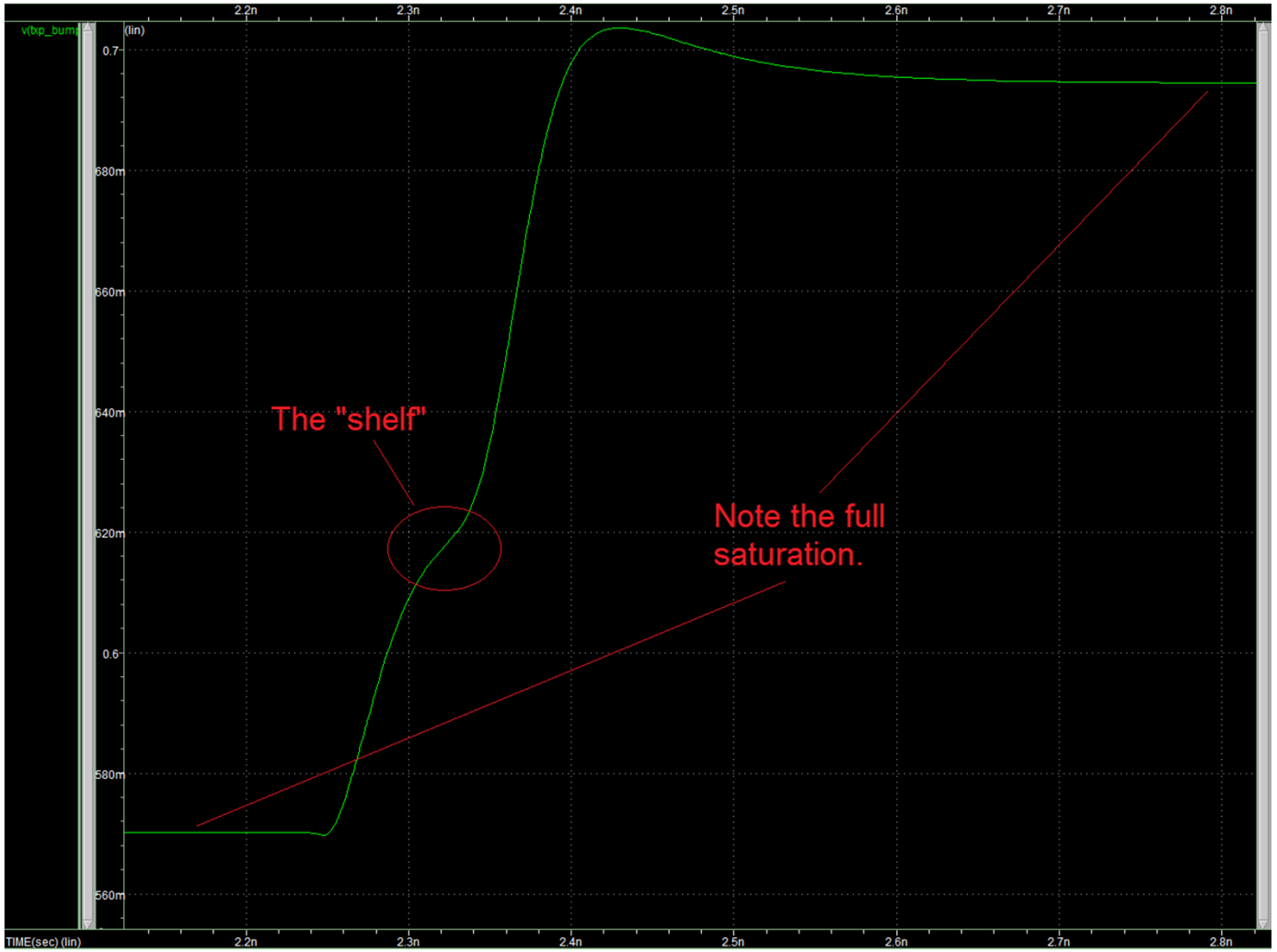
On non-linear edges and over-clocking

A response to AIs taken during the Open IBIS Forum Teleconference by David Banas on April 5, 2013.

Definition/illustration of the “shelf”



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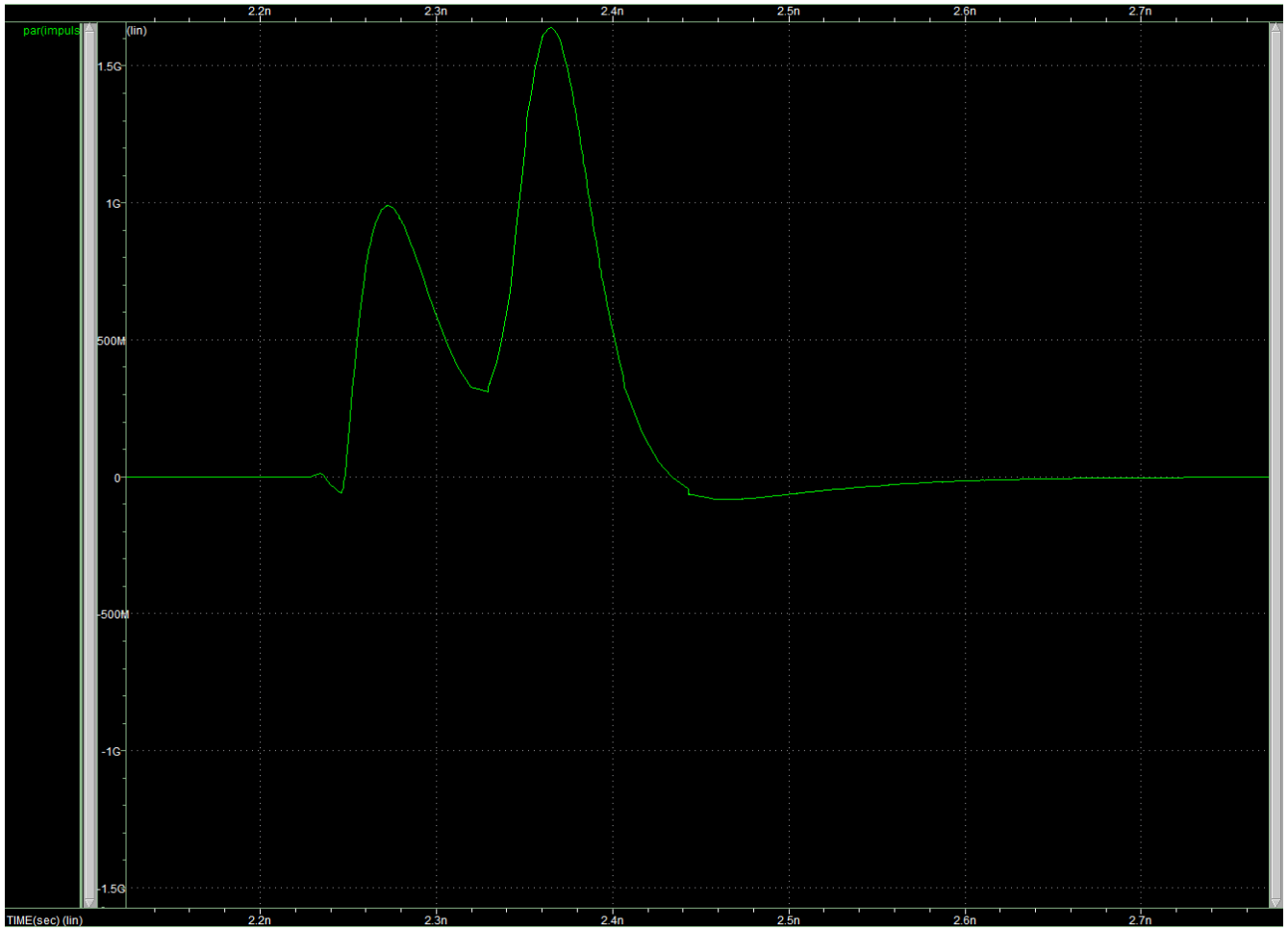
The shelf yields a rather interesting impulse response:



How can we possibly represent this, using a Ramp-only model?

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That was at full output driver saturation.

- **What about a more realistic case? Would the shelf still occur, if I were driving 12.5 Gbps, for instance?**

Yes! Although, it's not as pronounced.

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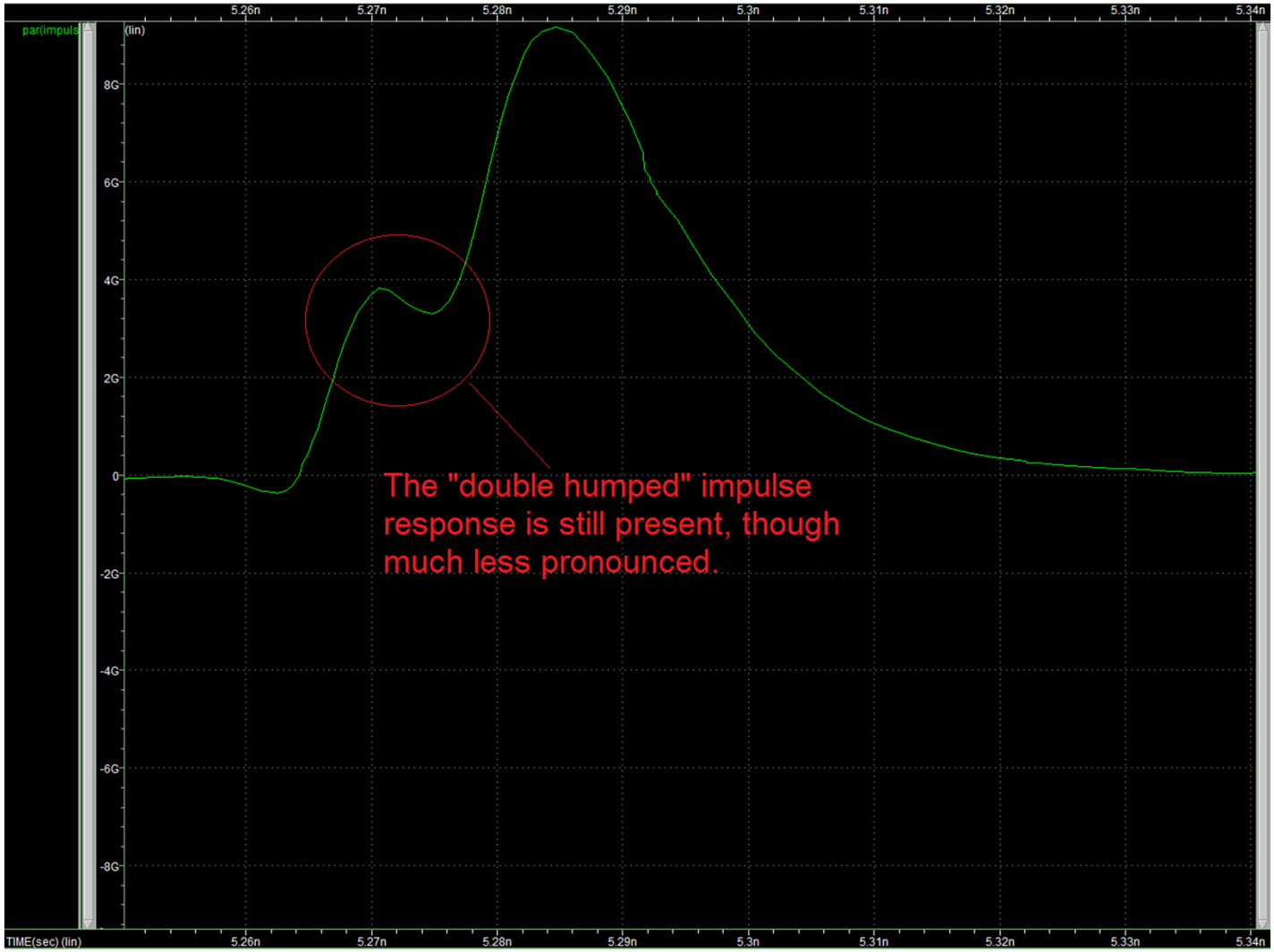
As is evidenced by the new effective impulse response:



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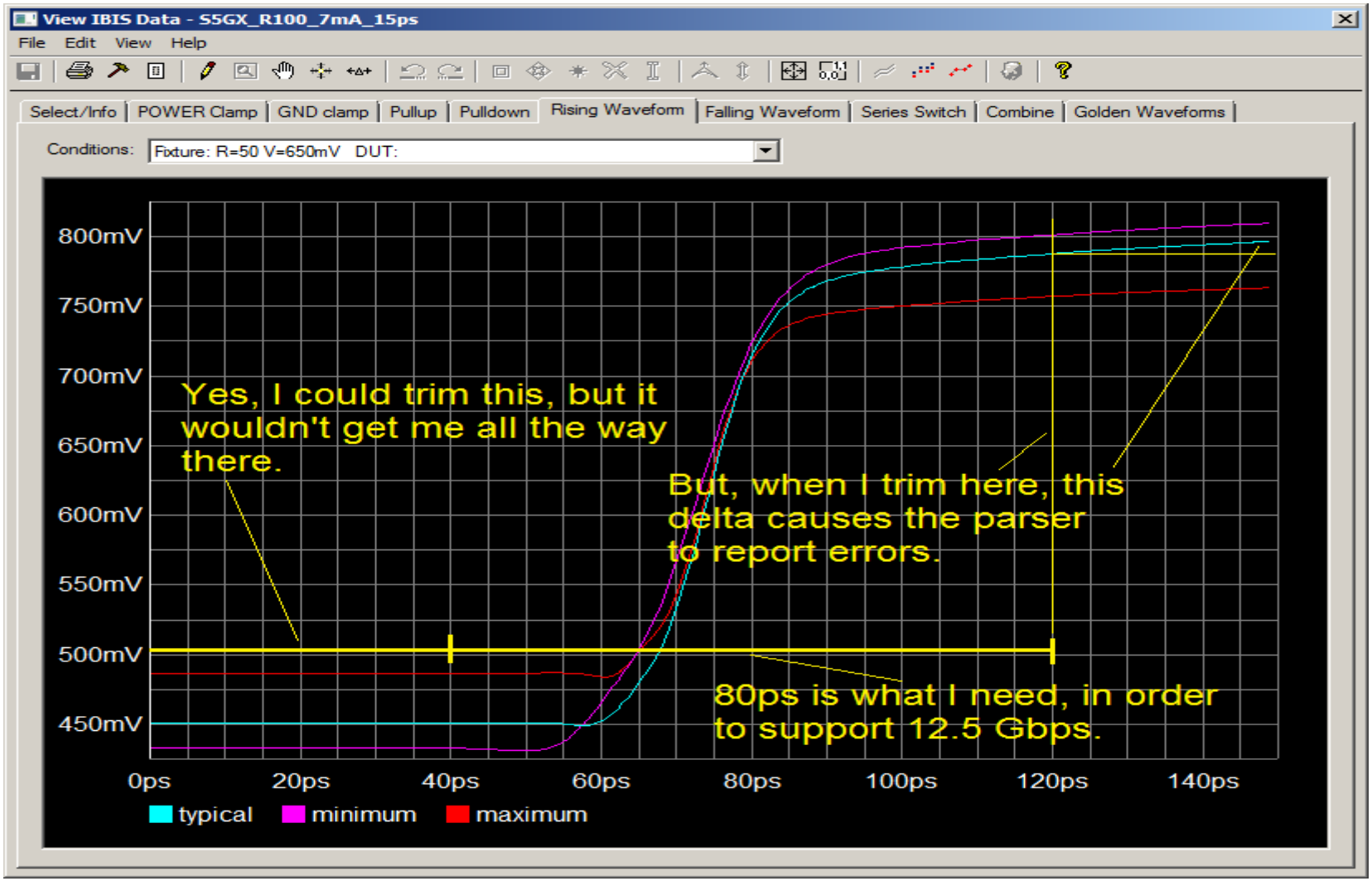
So, we need V/T tables, but…



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Parser errors are one thing; what about EDA tools?

- **Simulator A: PASS**
- **Simulator B: PASS**
- **Simulator C: (Stay tuned.)**
- **Note: “PASS” simply means that the typical, gross errors, regarding over-clocked operation, were not observed.**

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