**IBIS 7.0 Draft Editorial Known Issues**

Last updated December 19, 2018

Text highlighted in green show issues resolved in Draft 1 of IBIS 7.0.

Plain (unhighlighted) text summarizes issues that have not yet been resolved in Draft 1 of IBIS 7.0 and are recommended to be deferred until a later IBIS version.

1. Establish rules for whether “Usage Rules”, “Other Notes”, and similar headers should be removed if without content.
2. Consistently keep or remove periods at end of Definitions and Descriptions.
3. Enforce consistent rule about whether Definitions and Descriptions should be complete sentences.
4. Scrub keywords for clear separation between “Description” and “Usage Rules”. The former should be very brief, with any rules under the latter.
5. Items 9 and 13 in Section 3.2 are not syntax rules and should be moved or removed.
6. Under [Series Pin Mapping] and also [Model], the list of “(POWER, GND, or NC)” should either be expanded to include “CIRCUITCALL” or the entire parenthetical phrase should be removed.
7. Under [Series Pin Mapping], the phrase “straight through On paths” is used before “On” is explained. In addition, the term “paths” can be replaced by “paths for Series\_switch models” to be specific.
8. Under [Series Pin Mapping], the sentence “When using four columns, the header function\_table\_group must be listed.” should be followed by, “In this case, the entries in the function\_table\_group establish membership of the series pins in named groups used by [Series Switch Groups].”
9. Table 1 uses the phrase “the parser” twice, without elaborating that the standard parser is the only one being affected; overall, the phrase is inappropriate for the format specification. The phrase “the parser issues a warning and” should therefore be removed.
10. The Section 8.2 [Number of Pins] description consists solely of “Tells the parser how many pins to expect.” This is at least incomplete. A similar issue occurs under Section 7.3 [Pin Numbers], Section 8.2 [Pin List], and 7.3 [Number Of Pins].
11. The phrase “the parser” is used in [Bandwidth] where “the EDA tool” is clearly meant. The same issue occurs in 10.3.2.
12. [Model Selector] usage rules used the phrase “keyword and/or pin list” without explanation.
13. The [Model] keyword contains the sentence “The Rref\_diff and Cref\_diff are recognized only when the [Diff Pin] keyword connects the models.” This sentence does not clearly state whether these are forbidden if the [Diff Pin] keyword is missing.
14. Under [Model], the sentences “The Vmeas subparameter is the timing reference voltage level that the semiconductor vendor uses for the model.“ should be “The Vmeas subparameter is the timing reference voltage level that the semiconductor vendor uses for measuring the model timing.“
15. Section 5, Interconnect Model Group should change:

If any \*\_I/O pin is marked as Aggressor\_Only, then all \*\_I/O pins with the same pin\_name entry shall be considered as Aggressor\_Only.

… to something like…

If any \*\_I/O pin is marked as Aggressor\_Only, then any \*\_I/O pin with the same pin\_name entry shall be considered as only an aggressor, and not a victim, of coupling.

1. [Driver Schedule] contains the sentences “Even though some of the keywords are ignored in the scheduled model, it may still make sense in some cases to supply correct data with them. One such situation would arise when a [Model] is used both as a regular top-level model as well as a scheduled model.

The [Driver Schedule] table consists of five columns. The first column contains the model names of other models that exist in the .ibs file.” These lines imply that a model can schedule itself, but that only “other models” may be mentioned in the first column.

1. [Voltage Range] does not mention its own connection to derivation of [Ramp] data.
2. [Pulldown], [Pullup],… keyword text uses the following statements, which are no longer strictly true: It is also recognized that the data may be monotonic if currents from both the output stage and the clamp diode are added together as most EDA tools do. To limit the complexity of the IBIS syntax checking programs, such programs will conduct monotonicity testing only on one I-V table at a time.”
3. Section 6.2 is separated from the [Add Submodel] definition.
4. The following sentence under [Submodel Spec] may need to be moved to the same area as the rest rest of the Off\_delay rules: “Therefore the minimum and maximum entries for the Off\_delay subparameter should be ordered simply by their magnitude.”
5. In Section 1, should exact dates be used for all IBIS documents listed?
6. Should headers be used for columns in all examples?
7. [Path Description] contains a number of header-like lines which are not differentiated in terms of style.
8. Under [Pin Numbers], the following text appears:

“If a [Component] references a [Define Package Model] with the [Package Model] or an [Alternate Package Models] keyword, the EDA tool is expected to simulate the package parasitics of the pins in the component's [Pin] keyword that are not listed in the [Pin Numbers] keyword according to the hierarchy rules stated under the [Package] keyword.”

Yet, several paragraphs later, the following text appears:

“If none of the power/ground pins of a bus defined in the [Pin Mapping] keyword appears under the [Pin Numbers] keyword, the EDA tool is expected to use the RLC values from the [Pin] or [Package] keywords according to the hierarchy rules stated under the [Package] keyword.”

Should both paragraphs use the “[Pin] or [Package] keywords” language?