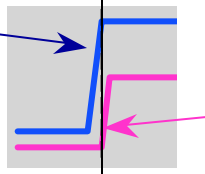
Use Four VT Curves to Model a Normal Digital IO Driver

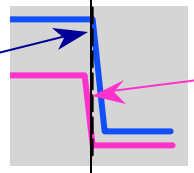
- Rising VT Curve thru 50 Ohms tied to POWER
- Rising VT Curve thru 50 Ohms tied to GROUND
- Falling VT Curve thru 50 Ohms tied to POWER
- Falling VT Curve thru 50 Ohms tied to GROUND

Note that both falling curves and both rising curves must be "time-correlated", meaning they must begin at the same point in time

Why Cadence Uses Four Time-Correlated VT Curves

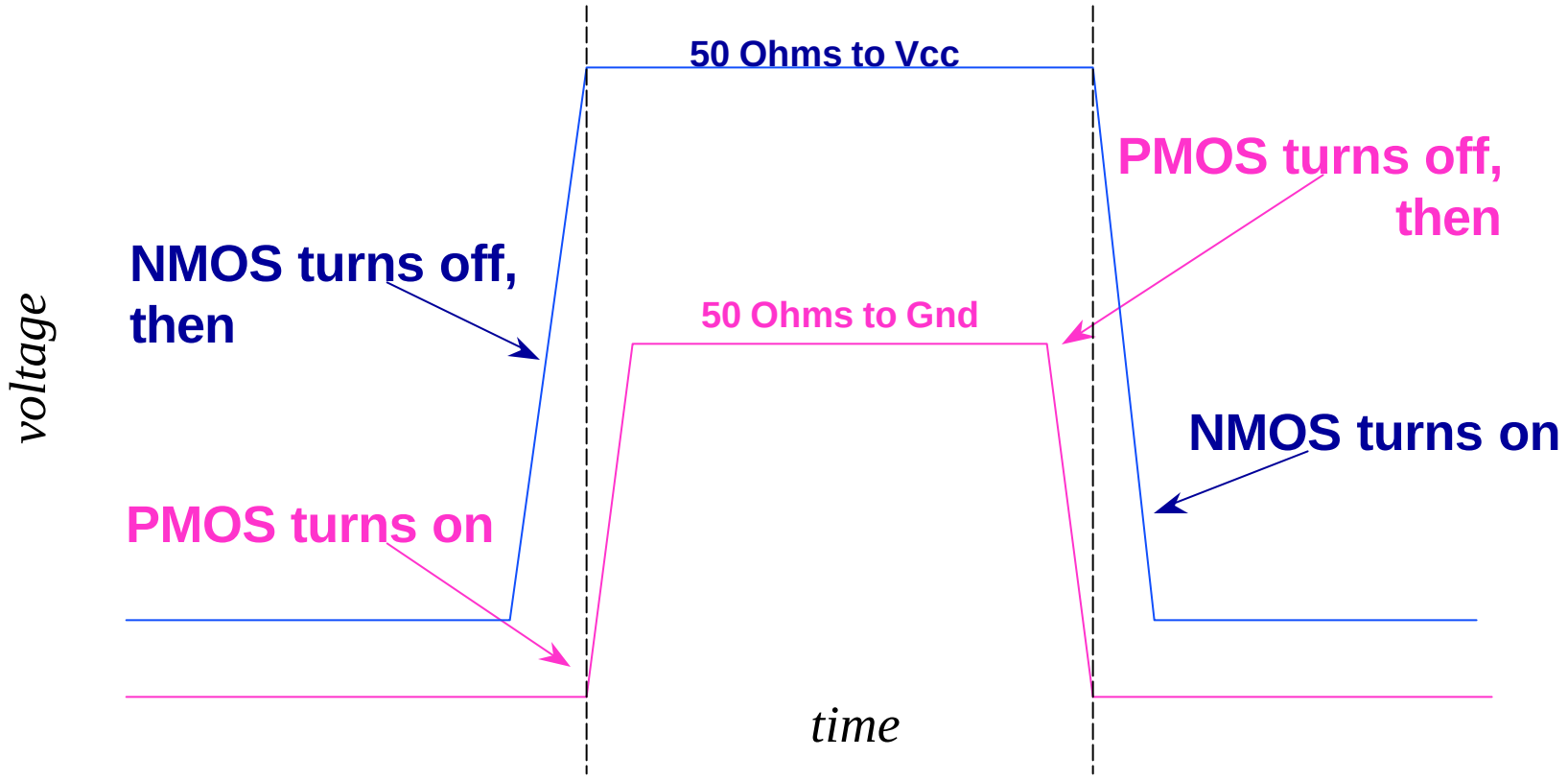
	Tied to POWER	Tied to GROUND
Rising VT	nmos turning off	pmos turning on
Falling VT	nmos turning on	pmos turning off





- each of the 4 curves shows important info, as shown
  - for example, for a rising edge the nmos must turn off as (before) the pmos turns on - to model rising edges accurately you need to capture how these two events happen in time
- when data is collected in this way, you do not need to manually time how pmos/nmos turn on/off relative to each other - it's embedded in the VT data

What the VT Curves should like like, when correct:



- this is just ‘normal’ digital I/O behavior, and prevents “crowbar” current thru the I/O

cadence