**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: TBD**

**ISSUE TITLE:** Clarification when two different I/O pin\_names have the same

signal\_name

**REQUESTOR:**  Walter Katz, Signal Integrity Software, Inc.

**DATE SUBMITTED:**

**DATE REVISED:**

**DATE ACCEPTED:**

**DEFINITION OF THE ISSUE:**

There is no rule that prevents two different pin\_names having the same signal\_name. The following passes IBISCHK7 V7.0.0:

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

CP22 MA7 ADD\_CMD

CP22x MA7 DQ

This is a confusing situation. This BIRD will require that if two or more pins have the same signal\_name they shall have the same model\_name, and that there shall be one instance of that model\_name that is connected to all of the pins with that same signal\_name. This BIRD shall also clarify the package model that shall be used to connect these pins to the model instance.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. New rule that requires that two or more pins with the same signal\_name shall have the same model name.
 |  |
| 1. Define package models shall connect the pins with the same signal name to the I/O buffer model.
 |  |

**PROPOSED CHANGES:**

Replace the following paragraph on page 29

If a pin has a model\_name POWER, then all other pins with the same signal\_name as this pin shall

have model\_name POWER. If a pin has model\_name GND, then all other pins with the same

signal\_name as this pin shall have model\_name GND.

With

With a pin has a model\_name that is not CIRCUITCALL or NC then all other pins with the same

signal\_name as this pin shall have the same model\_name.

After the following bullet item on page 35.

* If an \*\_I/O pin\_name does not appear on a terminal line in any Interconnect Model in an Interconnect Model Group, then the EDA tool should use any other existing package model in this document.

Add

* If two or more I/O pin\_names have the same signal\_name, and one of them is in any Interconnect Model in an Interconnect Model Group, then all of them shall be in the interconnect model.

**BACKGROUND INFORMATION/HISTORY:**