# IBIS Interconnect Commonly Supported Package Sets

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# Overview

Some of us want, and require, the new interconnect modeling BIRD to do everything under the sun, and I think we have accomplished that. What I would suggest, as either part of the BIRD or in a separate “Cookbook” document what EDA tools would expect the minimum requirements of a package model to support:

1. Signal integrity on each I/O buffer on each pin (or pair of differential pins) in the component
2. Signal integrity with crosstalk on each I/O buffer on each pin (or pair of differential pins) in the component
3. Power distribution models.
4. Integrated power and signal coupled models.

# Pin to Pad and Pad to Buffer Models

- The example on the following slides are all Pin to Buffer models.
- Everyone one of the Pin to Buffer interconnect models can be split into separate Pin to Pad and Pad to Buffer models.
  - The Pad terminals of the Pin to Pad model match one to one with the Pad terminals of the Pad to Buffer model

# Signal Integrity Set

- One two terminal model for each single ended I/O buffer and one four terminal model for each differential I/O buffers. The terminals would be the Buf_I/O and Pin_I/O.

# Crosstalk Set

- At least one model for each single ended I/O buffer and for each differential I/O buffers that has terminals Buf_I/O and Pin_I/O that are not marked “Incomplete Coupling”, and some number (which can be 0) terminals of other Buf_I/O and Pin_I/O pairs that may or may not be marked “Incomplete Coupling”.
- A buffer which is not “Incomplete Coupling” can be in multiple models. The model maker cannot make any assumptions on which model an EDA tool will use when analyzing crosstalk on this buffer.

# Power and Signal Integrity Set

- One two terminal model for each single ended I/O buffer and one four terminal model for each differential I/O buffers. The terminals would be the Buf_I/O and Pin_I/O.
- One of the following:
  - One two terminal model for each Power signal_name. The terminals would be Buf_Rail and Pin_Rail. This would assume ground referenced simulations.
  - One multi-terminal model with two terminals for each signal_name that is a Power or GND

# Full Package Model Set

- One or more multi-terminal model(s) for either the whole chip or large sections of the chip. This model can include Power, GND as well as I/O terminals. Terminals would be at the pins and buffers.
- This set would optionally have one of the following:
  - One two terminal model for each Power signal_name. The terminals would be Buf_Rail and Pin_Rail. This would assume ground referenced simulations.
  - One multi-terminal model with two terminals for each signal_name that is a Power or GND

# This does not need to be part of the IBIS specification but a published agreement between EDA companies.

The new interconnect BIRD allows for very flexible ways of creating package models for IBIS components. There is so much flexibility, that it may be challenging for EDA tools to automatically insert the correct package models into a simulation. The EDA companies in IBIS have agreed that package models that follow the rules set out in this document will be supported in their respective EDA tools.