**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: *Draft 9 August 27 , 2014***

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS*

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**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS interconnect models to supterminal Broadband and Coupled package and on-die interconnect using IBIS-ISS and Touchstone models.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

Definitions:

IBIS Interconnect modeling makes several assumptions:

1. Interconnect Models can either be IBIS-ISS subckts or Touchstone Files
2. If two points are “Connected” then there is either a low resistance DC electrical path between the two points, or a small insertion loss at Nyquist frequency between the two points.
3. For each I/O Pin, there is a Die Pad and Buffer I/O that are “Connected”.
4. For each POWER or GND Signal\_name, all pins, die pads and buffer supply terminals that use that Signal\_name are “Connected”
5. The Terminals (or Terminals) of Interconnect Models are Pins, Die Pads, Buffer I/O or Buffer supply terminals.
6. An Interconnect Model may represent a single connection between Pins and Buffers, Pins and Die Pads, or Die Pads and Buffers. An Interconnect Model may also represent multiple connections between Pins and Buffers, Pins and Die Pads, or Die Pads and Buffers.

**ANY OTHER BACKGROUND INFORMATION:**

{*These documents will be archived, so use this section to add any detail that is not part of the section above or the changed text itself , but should not be lost.}*

*Keyword:* [Interconnect Model Selector]

*Required:* No

*Description:* Used to pick an interconnect model for this component.

*Usage Rules:* Interconnet Models are IBIS-ISS subckts or Toucshstone files that are interconnect models between the Pins, Die Pads and Buffers of a Component.

A component may have none, one or more [Interconnect Model]. If there are any [Interconnect Model]s, they must be listed in this section.

The section under the [Interconnect Model Selector] keyword must have two fields. The fields must be separated by at least one white space. The first field lists the [Interconnect Model] name (up to 40 characters long). The second field is the name of the file containing the [Interconnect Model]. If the [Interconnect Model] is in this IBIS file, then the second field must be “\*”.

The first entry under the [Interconnect Model Selector] keyword shall be considered the default by the EDA tool.

*Example:*

[Interconnect Model Selector]

QS-SMT-cer-8-pin-pkgs\_iss \*

QS-SMT-cer-8-pin-pkgs\_sNp QS-SMT-cer-8-pin-pkgs\_sNp.ipkg

[End Interconnect Model Selector]

*Keyword:* [Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an interconnect model description.

*Usage Rules:* The length of the package model name must not exceed 40 characters in length. Blank characters are not allowed.

*Example:*

[Interconnect Model] QS-SMT-cer-8-pin-pkgs\_iss

*Keyword:* [Manufacturer] Allow or Require

*Keyword:* [Description] Allow or Require

Same requirements as in IBIS if separate file.

*Keyword:* **[Begin Interconnect Model] <Interconnect Model Name>**

*Subparameter:* **Source <IBIS-ISS | Touchstone>**

*Subparameter:* **File <file name> {<file name> <file name>}**

*Subparameter:* **Subckt <subckt name> {< subckt name> < subckt name>}**

*Subparameter:* **Parameter <name> <param value> {<param value > <param value >}**

*Subparameter:* **Unused\_Terminal\_Termination <resistance>**

*Subparameter:* **Number\_of\_Terminals <# terminals> | Made into a Subparameter**

*Subparameter:*  **Terminal <Field 1> <Field 2> <Field 3> <Field 4> {<Field 5> <Field 6> <Field 7>}**

*Subparameter:*  **Terminals <Terminal 1> < Terminal 2> < Terminal 3> < Terminal 4> …**

*Keyword:* **[End Interconnect Model]**

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, to end the [**Interconnect Model**] keyword

*Description:* Indicates the end of the interconnect model data.

*Other Notes:* In between the [Interconnect Model] and [End Interconnect Model] keywords is the package model data itself. The data is any number of interfaces to either IBIS-ISS models or Touchstone files.

*Example:*

[End Interconnect Model]

We need a careful discussion on how Pin Mapping is used in conjunction with Terminals that have Signal\_name. (MM)

We need a carefull discussion on when package models are Pre-Layout only. (Walter)

We need a carefull discussion on precedence rules if more than one model can be used to represent interconnect. (Walter)

Interaction with Circuit Call and External Circuit? (Mutually Exclusive)

Interaction with Define Package Model, or are they **mutually exclusive.**

Precedence Rules? Both allowed in a component but only one type can be used.

*Sub-Params:* File\_TS, File\_ISS, Param | Other sub-params not fully documented here

*Usage Rules:* Number\_Of\_Nodes, Terminal and either File\_TS or File\_ISS are required (both File\_TS and File\_ISS together are not permitted).

For referencing Touchstone files:

*Subparameter:* **File\_TS** **Typ\_File Min\_File Max\_File**

*Required:* Either File\_TS or File\_ISS is required for a [Begin Model]/[End Model] group

*Description:* File\_TS is followed by three entries for typ, min, and max file names. The typical entry is required and must point to a Touchstone file located in the same directory as the .ibs file and representing typical conditions. The minimum and maximum entries may point to the same file or other files representing minimum (slow) and maximum (fast) interconnect conditions or contain NA. If the entry is NA, the typical file entry shall be used.

*Example:*

| file\_type typ min max

File\_TS typ.s8p min.s8p max.s8p

or

| file\_type typ min max

File\_TS typ.s4p min.s4p NA

For referencing IBIS-ISS files:

*Subparameter:* **File\_ISS**  **Typ|Min|Max File\_Name Circuit\_Name**

*Required:* Either File\_TS or File\_ISS is required for a [Begin Model]/[End Model] group

*Description:* File\_ISS is followed by three entries consisting of corner\_name, file\_name, and circuit\_name (.subckt name) for that file and located in the same directory as the .ibs file. The corner\_name shall be Typ, Min, or Max. File\_ISS for the Typ corner\_name is required, and File\_ISS for the Min and Max corner\_names are optional. If present, each File\_ISS must have a unique corner\_name. If File\_ISS for either the Min or Max corner\_name is missing, the File\_ISS for the Typ corner\_name shall be used to describe the missing corner\_name file reference. The Min and Max file\_names should represent slow and fast interconnect conditions.*Example:*

| file\_type corner\_name file\_name circuit\_name (.subckt name)

File\_ISS Typ net.iss netlist\_typ

File\_ISS Min net.iss netlist\_min | in same file as net.sp

File\_ISS Max net\_max.iss netlist\_max | in separate file

*Subparameter:* **Param <name> Typ\_Value Min\_Value Max\_Value**

*Required:* No, but legal only if Language is IBIS-ISS.

*Description:*

The subparameter Param is optional and only legal for File\_ISS references. Param shall be followed by a param\_name of the parameter to be passed into the IBIS-ISS and its numerical values or a string values (surrounded by double quotes) located in the typ, min, and max columns. Several Param lines are permitted as long as each of the param\_name entries is distinct. Each Param line shall have a typ entry. Either or both the min and max entries can be NA, in which cases the typ entry is used. The typ, min, and max parameters are, by default, associated with the corner\_name Typ, Min, and Max files and their corresponding circuit\_names. However, the EDA tool is expected to support passing any of the Param typ, min, or max values, as selected by the User or EDA tool, into any File\_ISS corner\_name file. The Param values associated with any param\_name must all be numerical or all string values (or NA). If possible, the Param min and max values should represent slow and fast interconnect conditions. Because of parameter interactions, this may not always be possible.

*Other Notes:* The numerical value rules follow the scaling conventions in Section 3, GENERAL SYNTAX RULES AND GUIDELINES. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megohm, represented as 1M in Param would be converted to 1meg (1x is not recommended) in IBIS-ISS. The value 1Kohm is 1 ohm in IBIS and would therefore be passed into IBIS-ISS as 1 ohm, even though 1K is 1 kilohm in IBIS-ISS. Quoted string parameters are converted to the string parameter syntax in IBIS-ISS. For example, the Param value “typ.s2p” is converted to str(‘typ.s2p’) in IBIS-ISS.

The base unit of frequency is Hertz, and the base unit of length is meter. Values can be passed in terms of other base units of length if scaling conversions are added to the IBIS-ISS .subckt definition. For example, the intended value of 10 mils might be entered as the Param value of 10 if the conversion to 10 mils is done through multiplication within the .subckt.

*Examples:*

| Param param\_name typ min max

Param abc 2m 1m 2m

Param def 4k NA NA

Param ts\_file “typ.s2p” “min.s2p” “max.s2p” | used in IBIS-ISS

NOTES AND QUESTIONS

Source Touchstone | IBIS-ISS is not necessary since the file format is recognized by File\_TS or File\_ISS. File\_ISS captures both the file\_name and circuit\_name for each corner.

For File\_ISS, an alternative syntax could have been File\_ISS\_Typ, File\_ISS\_Min, File\_ISS\_Max to eliminate the corner\_name column, where only File\_ISS\_Typ is required for file references to IBIS-ISS.

Parameter is shorted to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax. (Parameter has several meanings in IBIS/IBIS-AMI.)

File\_names are not quoted to be consistent with Corner in the multi-lingual syntax.

For File\_TS, all columns typ, min, and max are entered (or NA for either or both min and max) to follow the corner syntax convention used for most IBIS keywords and subparameters. The typ entry is required, and the typ entry is used for any NA entry. The same typ, min, max convention is used for the subparameter Param.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

FBASE and FMAX are not defined in IBIS-ISS or Touchstone, so they are not documented here as reserved names for parameters.

Interaction of Param entries was not discussed. For example, for a T-line TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner . Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values.) (TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

*Keyword:* **Unused\_Terminal\_Termination <resistance> (Brad)**

*Required:*  No

*Description:* Defines the termination that is to be applied to the Terminals of a subckt or Touchstone file that are not being used in each [Begin Interconnect Model]/[End Interconnect Model] group.

*Other Notes:* If this subparameter is defined the EDA should connect the unused Terminals to GND through a **<resistance>** ohm resistor.

If this parameter is not defined and if Language is IBIS-ISS, then the EDA tool should connect the unused Terminals to GND through a 1Meg ohm resistor. If Language is Touchstone, then the EDA tool should connect the unused Terminals to GND through a resistor with the Touchstone File reference resistance of the Terminal.

*Example:*

[Unused\_Terminal\_Termination] 50

*Keyword:* **Number\_of\_Terminals <# terminals> | Made into a Subparameter**

*Required:*  Yes, for each [Begin Interconnect Model]/[End Interconnect Model] group

*Description:* The number of terminals (terminals) of the IBIS-ISS subckt or Touchstone file.

*Other Notes:*

*Example:*

Number\_of\_Terminals 2

*Subparameter:*  **Terminal Terminal\_number Location ID {Qualifiers}**

*Required:* An Interconnect Model must have Terminal subparameter records for each [Begin Interconnect Model]/[End Interconnect Model] group.

*Description:* Each Terminal record contains information on a terminal of an IBIS-ISS subckt (or Touchstone file).

Terminal\_number must be a positive integer number greater or equal to one and less than or equal to the number of terminals ([Number of Terminals], of the IBIS-ISS subckt (or Toucshtone file). Two Terminal records may not have the same Terminal\_number. If a Terminal Number does not exist in any of the [Terminal] records then the terminal is unused, and should be terminated according to the Unused\_Terminal\_Termination\_ Rules.

Location shall be Pin, Pad, Buf, Pin\_Sig, Pad\_Sig, Buf\_Sig, Buf\_PURef, Buf\_PDRef, Buf\_PCRef, Buf\_GCRef or Buf\_XRef.

* Pin indicates this terminal is at a specific pin, ID must be a Pin\_name, Model\_name or Default.
* Pad indicates this terminal is at a specific die pad, ID must be a Pin\_name, Model\_name or Default.
* Buf indicates this terminal is at a specific buffer model I/O or signal terminal, ID must be a Pin\_name, Model\_name or Default.
* Pin\_Sig indicates that this terminal is connected to all pins that have Signal\_name ID. ID must be a Signal\_name on a Pin that has Model\_name Power or GND. All pins that have Signal\_name ID are considered shorted together at the pin side of the package model.
* Pad\_Sig indicates that this terminal is connected to all die pads that have Signal\_name ID. ID must be a Signal\_name on a Pin that has Model\_name Power or GND. All die pads that have Signal\_name ID are considered shorted together at the die pad side of the package model.
* Buf\_Sig indicates that this terminal is connected to all buffer model terminals Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference or External Reference that have a Signal\_name ID. ID must be a Signal\_name on a Pin that has Model\_name Power or GND. All Buffer terminal nodes that have Signal\_name ID are considered shorted together at the buffer side of the package model.
* Buf\_PURef indicates this terminal is at a specific buffer model pullup reference, ID must be a Pin\_name, Model\_name or Default.
* Buf\_PDRef indicates this terminal is at a specific buffer model pulldown reference, ID must be a Pin\_name, Model\_name or Default.
* Buf\_PCRef indicates this terminal is at a specific buffer model power clamp reference, ID must be a Pin\_name, Model\_name or Default.
* Buf\_GCRef indicates this terminal is at a specific buffer model ground clamp reference, ID must be a Pin\_name, Model\_name or Default.
* Buf\_XRef indicates this terminal is at a specific buffer model external reference, ID must be a Pin\_name, Model\_name or Default.

ID shall be a Pin\_name, Signal\_name, Model\_name or Default.

Qualifiers may have the values Aggressor, Model\_name, Default, Inverting, Non-Inverting and Connection(n). Qualifiers are optional, there may be zero, one or several qualifiers on each Terminal record. Qualifiers may appear in any order.

* Aggressor, any Terminal may have the qualifier aggressor. It means that terminal does not have coupling from all aggressor sources, so can be treated as an aggressor and should not be treated as a victim.
* Model\_name, means that the ID on this terminal is a Model\_name
* Default, means that the ID on this terminal must be Default.
* A terminal cannot have both Default and Model\_name qualifiers.
* If a terminal either qualifier Default or Model\_name then the terminal is considered a “Pre-Layout” terminal.
* If a “Pre-Layout” terminal is connected to a differential model, then the terminal must have either the Inverting or Non-Inverting qualifier.
* All terminals that have the same Connection(n) (where n is a positive integer) are electrically connected. A single ended connection will have two terminals with Connection(n). A differential connection will have four terminals with Connection(n).` Connection(n) qualifiers are required if there are two or more Pre-Layout connections.
* Special differential rules for Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference.
  + There can be only one terminal for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference on a true differential [External Model]. These can be referenced by either the Non-Inverting or Inverting Pin\_name.
  + There may be only one terminal for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference for each side of a legacy differential model that consists of two independent single ended models. These can be referenced by either the Non-Inverting or Inverting Pin\_name.
  + There may be two terminals for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference for each side of a legacy differential model that consists of two independent single ended models.

*Other Notes:*

More than one [Interconnect Model] may be available for a specific simulation. The EDA tool may choose any of the available models but, in general, should choose a model preferring a model that matches by Pin\_name, then Model\_name and finally Default.

An Interconnect Model will Source Touchstone will reference a Touchstone File with N Ports. N is either determined from the N in the .sNp file name extension for a Touchstone I file or from the [Number of Ports] record in a Touchstone II file. The [Number of Terminals] in the Interconnect Model shall either be N+1. The Terminal Rules is described below:

* [
  + The EDA tool shall use the Pin\_name or Signal\_name specified in the Terminal “N+1” record as the reference node for each of the N ports.
  + Terminal/Port Mapping
    - Terminal              Port
    - 1                              1
    - 2                              2
    - …
    - N                             N
  + If a Port is not connected, then it shall be terminated with a resistor to the node on Terminal N+1. The resistance shall be the Port Reference Impedance.
  + If Terminal N+1 is not connected, then the Port Reference shall be Global Ground.

*Examples:*

IBIS File

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

A1 DQ1 DQ

A2 DQ2 DQ

A3 DQ3 DQ

D1 DQS DQS

D2 DQS DQS

P1 VDD POWER

P2 VDD POWER

P3 VDD POWER

P4 VDD POWER

P5 VDD POWER

G1 VSS GND

G2 VSS GND

G3 VSS GND

G4 VSS GND

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Diff Pin] inv\_pin vdiff tdelay\_typ tdelay\_min tdelay\_max

D1 D2 NA NA NA NA

[Die Supply Pads]

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1 VSS VDD NC NC NC

A2 VSS VDD NC NC NC

A3 VSS VDD NC NC NC

D1 VSS VDD NC NC NC

D2 VSS VDD NC NC NC

* Single DQ (A1)
  + Terminal 1 Pin A1
  + Terminal 2 Buf A1
* Single DQS | There is a [Diff Pin] record “D1 D2 …”
  + Terminal 1 Pin D1
  + Terminal 2 Pin D2
  + Terminal 3 Buf D1
  + Terminal 4 Buf D2
* One DQ (A2) victim, two DQ (A1 and A3) aggressors
  + Terminal 1 Pin A1 Aggressor
  + Terminal 2 Buf A1 Aggressor
  + Terminal 3 Pin A2
  + Terminal 4 Buf A2
  + Terminal 5 Pin A3 Aggressor
  + Terminal 6 Buf A3 Aggressor
* Single DQ (A1) Pin to Die Pad
  + Terminal 1 Pin A1
  + Terminal 2 Pad A1
* Single ended model that can be used for all I/O pins
  + Terminal 1 Pin Default Default
  + Terminal 2 Buf Default Default
* Madel that can connect all Pins with Signal\_name VDD to all Buffer supply terminals that are connected to Signal\_name VDD as described in Pin\_mapping. All Pins with Signal\_name VDD are shorted together. All Buffer supply terminals that are connected to Signal\_name VDD are shorted together
  + Terminal 1 Pin\_Sig VDD
  + Terminal 2 Buf\_Sig VDD
* VDD: Pins connected to board “bed spring” model, all buffers connected to VDD shorted
  + Terminal 1 Pin P1
  + Terminal 2 Pin P2
  + Terminal 3 Pin P3
  + Terminal 4 Pin P4
  + Terminal 5 Pin P5
  + Terminal 6 Buf\_Sig VDD
* VDD: Interconnect between VDD Pins and individual buffer Pullup Reference.
  + Terminal 1 Pin P1
  + Terminal 2 Pin P2
  + Terminal 3 Pin P3
  + Terminal 4 Pin P4
  + Terminal 5 Pin P5
  + Terminal 6 Buf\_PURef A1
  + Terminal 7 Buf\_PURef A2
  + Terminal 8 Buf\_PURef A3
  + Terminal 9 Buf\_PURef D1
* VDD: Interconnect between VDD Pins and die VDD pads.
  + Terminal 1 Pin P1
  + Terminal 2 Pin P2
  + Terminal 3 Pin P3
  + Terminal 4 Pin P4
  + Terminal 5 Pin P5
  + Terminal 6 Pad VDD1
  + Terminal 7 Pad VDD2
  + Terminal 8 Pad VDD3
* VDD: Interconnect between die VDD pads and individual buffer Pullup Reference.
  + Terminal 1 Pad VDD1
  + Terminal 2 Pad VDD2
  + Terminal 3 Pad VDD3
  + Terminal 4 Buf\_PURef A1
  + Terminal 5 Buf\_PURef A2
  + Terminal 6 Buf\_PURef A3
  + Terminal 7 Buf\_PURef D1
* Single DQ
  + Terminal 1 Pin DQ Model\_name
  + Terminal 2 Buf DQ Model\_name
* Single DQS
  + Terminal 1 Pin DQS Model\_name Non-Inverting
  + Terminal 2 Pin DQS Model\_name Inverting
  + Terminal 3 Buf DQS Model\_name Non-Inverting
  + Terminal 4 Buf DQS Model\_name Inverting
* Single DQ victim, two DQ aggressors
  + Terminal 1 Pin DQ Model\_name Aggressor Connection(1)
  + Terminal 2 Buf DQ Model\_name Aggressor Connection(1)
  + Terminal 3 Pin DQ Model\_name Connection(2)
  + Terminal 4 Buf DQ Model\_name Connection(2)
  + Terminal 5 Pin DQ Model\_name Aggressor Connection(3)
  + Terminal 6 Buf DQ Model\_name Aggressor Connection(3)
* One DQ victim, two DQ aggressors, one DQS aggressor
  + Terminal 1 Pin DQ Model\_name Aggressor Connection(1)
  + Terminal 2 Buf DQ Model\_name Aggressor Connection(1)
  + Terminal 3 Pin A2
  + Terminal 4 Buf A2
  + Terminal 5 Pin DQ Model\_name Aggressor Connection(2)
  + Terminal 6 Buf DQ Model\_name Aggressor Connection(2)
  + Terminal 7 Pin DQS Model\_name Aggressor Connection(3) Non-Inverting
  + Terminal 8 Buf DQS Model\_name Aggressor Connection(3) Inverting
  + Terminal 9 Pin DQS Model\_name Aggressor Connection(3) Non-Inverting
  + Terminal 10 Buf DQS Model\_name Aggressor Connection(3) Inverting
* One single ended victim, two single ended aggressors, one differential aggressor
  + Terminal 1 Pin Default Default Aggressor Connection(1)
  + Terminal 2 Buf Default Default Aggressor Connection(1)
  + Terminal 3 Pin Default Default
  + Terminal 4 Buf Default Default
  + Terminal 5 Pin Default Default Aggressor Connection(2)
  + Terminal 6 Buf Default Default Aggressor Connection(2)
  + Terminal 7 Pin Default Default Aggressor Connection(3) Non-Inverting
  + Terminal 8 Buf Default Default Aggressor Connection(3) Inverting
  + Terminal 9 Pin Default Default Aggressor Connection(3) Non-Inverting
  + Terminal 10 Buf Default Model\_name Aggressor Connection(3) Inverting

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* This begins a section in [Component] that contains one line of data for die pads supply nodes. IBIS assumes that for I/O pins (pins that have a Model\_name that is not POWER, GND or NC), there is a one to one correspondence between a Pin, Die Pad and Buffer I/O. There are no such assumptions for POWER and GND pins. A POWER or GND Signal\_name may have a different number of Pin nodes, die pad nodes and buffer nodes. If the model maker chooses to make separate package and on-die power distribution networks (PDN), then he must supply a list of nodes (and their associated Signal\_name) that can be used to mate the package and on-die PDN models.

*Sub-Params:* ?

*Usage Rules:*  TBD

*Other Notes:* The data in this section consists of a list of die pad node names and their corresponding Signal\_names that can be used to mate package and on-die PDN networks.

*Example:*

[Die Supply Pads]

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[End Die Supply Pads]**

*Required:* Yes.

*Description:* Indicates the end of the [Die Supply Pads] data.

*Other Notes:*

*Example:*

[End Die Supply Pads]

**Examples**

[Define Package Model]

[ISS Model Data]

[Begin ISS Model] IOA3

Language Touchstone

File Value ioA3.s2p

Number\_of\_Terminals 2

Terminal 1 Pin Pin\_name A3

Terminal 2 Buffer Pin\_name A3

[End ISS Model]

[Begin ISS Model] IOA7

| This model uses I/O pin A7

Language Touchstone

File Value ioA7.s2p

Number\_of\_Terminals 2

Terminals Pin.A7 Buf.A7

[End ISS Model]

[Begin ISS Model] IOB3C3

Language Touchstone

File Value ioB3C3.s4p

Number\_of\_Terminals 4

Terminal 1 Pin Pin\_name B3

Terminal 2 Buffer Pin\_name B3

Terminal 3 Pin Pin\_name C3

Terminal 4 Buffer Pin\_name C3

[End ISS Model]

[Begin ISS Model] IOA3

Language IBIS\_ISS

File Value io.iss

Subckt io

Parameter Length Value 10. | 10mm

Number\_of\_Terminals 2

Terminal 1 Pin Pin\_name A3

Terminal 2 Buffer Pin\_name A3

[End ISS Model]

[Begin ISS Model] DQS

Language Touchstone

File Value DQS.s4p

Number\_of\_Terminals 4

Terminal 1 Pin Model\_name DQS Diff\_pos

Terminal 2 Buffer Model\_name DQS Diff\_pos

Terminal 3 Pin Model\_name DQS Diff\_neg

Terminal 4 Buffer Model\_name DQS Diff\_neg

[End ISS Model]

[Begin ISS Model] VDDQ

Language IBIS\_ISS

File Value vddq.iss

Subckt vddq

Number\_of\_Terminals 2

Terminal 1 Pin Signal\_name VDDQ

Terminal 2 Buffer Signal\_name VDDQ

[End ISS Model]

[Begin ISS Model] VDDQ\_A3

Language IBIS\_ISS

File Value vddq\_a3.iss

Subckt vddq\_A3

Number\_of\_Terminals 2

Terminal 1 Pin Signal\_name VDDQ

Terminal 2 Buffer Pin\_name A3 Pullup\_Reference

[End ISS Model]

[Begin ISS Model] IOA3

Language Touchstone

File Value ioA3.s10p

Number\_of\_Terminals 10

Terminal 1 Pin Pin\_name A3

Terminal 2 Buffer Pin\_name A3

Terminal 3 Pin Model\_name DQ NA 1 Aggressor

Terminal 4 Buffer Model\_name DQ NA 1 Aggressor

Terminal 5 Pin Model\_name DQ NA 2 Aggressor

Terminal 6 Buffer Model\_name DQ NA 2 Aggressor

Terminal 7 Pin Model\_name DQS Diff\_pos 3 Aggressor

Terminal 8 Buffer Model\_name DQS Diff\_pos 3 Aggressor

Terminal 9 Pin Model\_name DQS Diff\_neg 3 Aggressor

Terminal 10 Buffer Model\_name DQS Diff\_neg 3 Aggressor

[End ISS Model]

[End ISS Model Data]

[End Package Model]