**Rail**: Pins that have model name POWER or GND are rail pins. Terminals on any [Model] or interconnect model connected to rail pins are rail terminals of the model. IBIS is a behavioral language that describes the operation of a Device Under Test conditions with specific DC voltages applied to rail pins, or the rail terminals of a [Model] Simulations may account for operations of [Model]s when the actual voltage applied to a [Model] terminal are not the same as the voltages used for DUT.

**Introduction to Interconnect Modeling**

This interconnect modeling section supports broadband interconnect models between the pins of a component and I/O buffers. These models include the ability to define accurate interconnect coupling and interconnect rail distribution. The detailed effects of on-die interconnect are now important. Interconnect models can be supplied separately for on-die interconnect and package interconnect, or can be supplied as models directly between the package pins and I/O buffers.

An [Interconnect Model] defines the connections to either an IBIS-ISS SPICE subckt or a Touchstone file. An [Interconnect Model] can be between pins of the package and I/O buffers, pins of the package and die-pads or die-pads and I/O buffers.

[Interconnect Model]s are organized into [Interconnect Model Set]s. An [Interconnect Model Set] consist of one or more [Interconnect Model]s. One [Interconnect Model Set] may contain groups of similar models, for example:

* Uncoupled I/O connections.
* Couple I/O connections.
* Rail connections.
* Uncoupled IBIS-ISS models.
* Uncoupled Tocuhstone file connections.

[Interconnect Model]s can have die-pad terminals. A die-pad describes a simulation node at the interface between the die and the package. Each I/O pin has one I/O buffer terminal and one die-pad. Because there is not one-to-one relationship between rail pins and rail die-pads, we have introduced a new section [Die Supply Pads] ([Die Rail Pads]?). The following diagram of a package and die shows graphically the potential [Interconnect Model] terminals for an I/O:

The following diagram of a package and die shows graphically the potential [Interconnect Model] terminals for a rail connection. Note that these terminals can be collapsed to a single terminal at the pin/board interface, the die package interface and the I/O buffer rail terminals. Small red dots are [Die Supply Pads], large black dots are package bump pads.

The Terminal section of an [Interconnect Model] describes how the terminals of an Interconnect Model subckt or Touchstone file instance in a SPICE deck need to be connected at a buffer terminal, die-pad interface or pin/board interface.

The description of I/O terminals is very simple. The terminal needs to describe it it as the I/O Buffer, die-pad interface or pin, qualified by the I/O pin\_name.

The description of rail terminals is more complex to support models that have terminals at each pin, die-pad and and I/O Buffer rail terminals, or groups of pins, die-pads and I/O Buffer rail terminals.

* Pins
* A rail terminal can connect to a specific rail pin\_name
* A rail terminal can connect to all of the pins of a rail signal\_name
* A rail terminal can connect to all of the pins of a bus\_label
* Die-pads
* A rail terminal can connect to a specific [Die Supply Pads]
* A rail terminal can connect to all of the [Die Supply Pads] of a rail signal\_name
* A rail terminal can connect to all of the [Die Supply Pads] of a bus\_label
* I/O Buffer Rail Terminal
* A rail terminal can connect to a specific I/O Buffer rail terminal
* A rail terminal can connect to all of the I/O Buffer rail terminals of a rail signal\_name
* A rail terminal can connect to all of the I/O Buffer rail terminals of a signal\_name

The sub-parameter Number\_of\_terminals tells how many SPICE nodes are required on the instance in a SPICE deck.

The terminal lines that follow this keyword describe the SPICE node each terminal should be connected to. Terminals may be at pins, die-pads or the I/O buffer

* The first column Terminal\_number is a number between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the SPICE node in the [Interconnect Model] subckt or Touchstone file instance. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Agressor”
* The second field Terminal\_type determins if the terminal is at a pin, die-pad or I/O buffer.
	+ For I/O connections
		- Terminal\_type can be Pin\_I/O, Pad\_I/O and Buf\_I/O
		- Terminal\_type\_qualifier shall be pin\_name.
		- Qualifier\_entry shall be the pin\_name of an I/O pin.
	+ For rail connections
		- Allowed Terminal\_type, Terminal\_type\_qualifier and Qualifier\_entry rules are different at pins, die-pads and I/O Buffer.
		- At pins
			* Terminal Type shall be Pin\_Rail
			* Terminal\_type\_qualifier shall be one of the following
				+ pin\_name

Qualifier\_entry shall be the pin\_name of a rail pin.

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * + sgnal\_name

Qualifier\_entry shall be a rail signal\_name

* + - At die-pads
			* Terminal type shall be Pad\_Rail
			* Terminal\_type\_qualifier shall be
				+ pad\_name

Qualifier\_entry shall be the pin\_name of a rail pin.

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * + signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - At I/O Buffers
			* Terminal Type shall be one of the following
				+ Buf\_Rail

Terminal\_type\_qualifier shall be one of the following

signal\_name

Qualifier\_entry shall be a rail signal\_name

bus\_label

Qualifier\_entry shall be a bus\_label

* + - * + Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref or Ext\_ref

Terminal\_type\_qualifier shall be I/O buffer pin\_name

Qualifier\_entry shall be the I/O buffer pin\_name

Crosstalk simulations require Interconnect Models have connections to multiple I/O Pin\_names.

* This specification also a complete interconnect model that includes all of the I/O connections.
* This specification also supports subset of the complete package model.
* An example is a model containing the coupled interconnect of DQ6, DQ7 and DQ8.
	+ The following picture highlights three DQ connections DQ6, DQ7 and DQ8 in a single [Interconnect Model]. DQ7 is in the middle, DQ6 is on the left side of DQ7, and DQ8 is on the right side of DQ7.

* + DQ7 has crosstalk in the package with the adjoining signals DQ6 and DQ8.
		- This model represents all of the crosstalk on DQ7 (since it includes DQ6 and DQ8).
	+ This model does not include all of the crosstalk affecting DQ8 since the model does not include DQ9.
	+ Similarly DQ6 does not include all of its aggressors (DQ5).
	+ The model maker tells the EDA tool that connections to terminals DQ6 and DQ8 do not include all of their aggressors by adding the optional field “Aggressor” to their terminals. (Not suitable for victim: Aggressor\_Only, Non\_Victim)
	+ In this case, simulations will include coupling on DQ6 and DQ8 from DQ7, but it will not include coupling from their aggressors (DQ5 and DQ9).
	+ The DQ7 connections do not have the optional “Aggressor” field. The EDA tool may assume that DQ7 has all (or more practically most of) the coupling to its aggressor connections.