**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 202.1\_draft15

**ISSUE TITLE:** Electrical Descriptions of Modules

**REQUESTOR:**  Walter Katz, Signal Integrity Software

**DATE SUBMITTED:** January 22, 2020

**DATE REVISED:**

**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

The industry lacks a method to describe modules that consist of one or more integrated circuits or other modules mounted on a printed circuit board, multi-chip module or substrate that connects them to a system through a set of pins. The following BIRD proposes a new type of file called .emd – Electrical Module Description (EMD) – that addresses this need. This proposal does not encompass an electrical description of connectors and other interconnect devices.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible descriptions of module interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| * The model maker must be able to provide EMD Models representing modules, using a combination of IBIS-ISS and Touchstone formats. |  |
| * Touchstone models without an IBIS-ISS wrapper circuit must be supported. |  |
| * An EMD Model may connect one signal\_name or any combination of signal\_names in one [Begin EMD]. | Coupled electrical paths are supported. |
| * IBIS component pin terminals associated with I/O pins must be assignable to EMD Model terminals directly by pin name. |  |
| * EMD pin terminals associated with POWER and GND rail pins must be assignable to EMD Model terminals directly by pin name, or indirectly by [Pin] signal\_name or bus\_label. |  |
| * The model maker must be able to provide alternative EMD Models for any given set of pins. | For example, for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
| * The EDA tool and model user must be able to locate all EMD Models that include a specified set of pins it must analyze. | Simulation netlisting begins with a list of pins that must be simulated. |
| * The EDA tool and model user must be able to determine all the pins that a given EMD Model includes. | Once a model is chosen, it may add more pins to the simulation. |
| * The EDA tool and model user must be able to determine how to terminate any terminals of an EMD Model not necessary for an analysis. | May need to handle Touchstone and IBIS-ISS models differently. |
| * The model user must have useful information needed to make the choice between alternative EMD Models that differ only in characteristics other than the model format and the set of pins included. | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
| * The model user must be informed which pins of an EMD Model have been modeled with coupling to other pins, sufficient to represent the victim pins and all the aggressor pins in a crosstalk simulation. |  |

**BACKGROUND INFORMATION/HISTORY:**

STATEMENT OF THE RESOLVED SPECIFICATIONS:

**Under Section 3, First Paragraph**

REPLACE

Unless noted otherwise, this section contains general syntax rules and guidelines for IBIS file formats .ibs (Sections 4, 5, 6 and 12), .pkg (Section 7), .ebd (Section 8), .ims (Section 11), and where applicable, .ami (Sections 10.3 through 10.11) and parameter passing files (Section 6.3).

WITH (adding .emd, .ems):

Unless noted otherwise, this section contains general syntax rules and guidelines for IBIS file formats .ibs (Sections 4, 5, 6 and 12), .pkg (Section 7), .ebd (Section 8), .ims (Section 11), .emd (Section 12??), .ems (Section 13??), and where applicable, .ami (Sections 10.3 through 10.11) and parameter passing files (Section 6.3).

**ADD to Section 3.3 Keyword Hierarchy:**

.emd FILE

├── File Header Section

│ ├── **[IBIS Ver]**

│ ├── **[Comment Char]**

│ ├── **[File Name]**

│ ├── **[File Rev]**

│ ├── **[Date]**

│ ├── **[Source]**

│ ├── **[Notes]**

│ ├── **[Disclaimer]**

│ └── **[Copyright]**

│

├── **[Begin EMD]**

│ ├── **[Manufacturer]**

│ ├── **[Description]**

│ ├── **[Number of EMD Pins]**

│ ├── **[EMD Pin List]** signal\_name, signal\_type

│ │ │bus\_label

│ │ └── **[End EMD Pin List]**

│ │

│ ├── **[EMD Parts]**

│ │ └── **[End EMD Parts]**

│ │

│ ├── **[EMD Designator List]**

│ │ └── **[End EMD Designator List]**

│ │

│ ├── **[Designator Pin List]** signal\_name, signal\_type

│ │ │ bus\_label

│ │ └── **[End Designator Pin List]**

│ │

│ ├── **[Voltage List]**

│ │ └── **[End Voltage List]**

│ │

│ ├── **[EMD Group]**

│ │ └── **[End EMD Group]**

│ │

│ └── **[End EMD]**

│

├── **[EMD Set]**

│ ├── **[Manufacturer]**

│ ├── **[Description]**

│ ├── **[EMD Model]** Param, File\_TS, File\_IBIS-ISS,

│ │ │ Unused\_port\_termination,

│ │ │ Number\_of\_terminals

│ │ └── **[End EMD Model]**

│ │

│ └── **[End EMD Set]**

│

└── **[End]**

.ems FILE

├── File Header Section

│ ├── **[IBIS Ver]**

│ ├── **[Comment Char]**

│ ├── **[File Name]**

│ ├── **[File Rev]**

│ ├── **[Date]**

│ ├── **[Source]**

│ ├── **[Notes]**

│ ├── **[Disclaimer]**

│ └── **[Copyright]**

│

├── **[EMD Set]**

│ ├── **[Manufacturer]**

│ ├── **[Description]**

│ ├── **[EMD Model]** Param, File\_TS, File\_IBIS-ISS,

│ │ │ Unused\_port\_termination,

│ │ │ Number\_of\_terminals

│ │ └── **[End EMD Model]**

│ │

│ └── **[End EMD Set]**

│

└── **[End]**

**In Section 4:**

REPLACE

*Keyword:* [File Name]

*Required:* Yes

*Description:* Specifies the file name of the file containing this keyword.

*Usage Rules:* The file name shall conform to the rules in item 3 of Section **Error! Reference source not found.**.2, "SYNTAX RULES". In addition, the file name shall use the extension “ibs”, “pkg”, “ebd”, or “ims”. The file name shall be the actual name of the file.

*Example:*

[File Name] ver6\_1.ibs

*Keyword:* [File Rev]

*Required:* Yes

*Description:* Tracks the revision level of a particular .ibs, .pkg, .ebd, or .ims file.

*Usage Rules:* Revision level is set at the discretion of the engineer defining the file. The following guidelines are recommended:

0.x silicon and file in development

1.x pre-silicon file data from silicon model only

2.x file correlated to actual silicon measurements

3.x mature product, no more changes likely

*Example:*

[File Rev] 1.0 | Used for .ibs file variations

WITH (adding .emd, .ems)

*Keyword:* [File Name]

*Required:* Yes

*Description:* Specifies the file name of the file containing this keyword.

*Usage Rules:* The file name shall conform to the rules in item 3 of Section **Error! Reference source not found.**.2, "SYNTAX RULES". In addition, the file name shall use the extension “ibs”, “pkg”, “ebd”, “ims”, “emd”, or “ems”. The file name shall be the actual name of the file.

*Example:*

[File Name] ver7\_1.ibs

*Keyword:* [File Rev]

*Required:* Yes

*Description:* Tracks the revision level of a particular .ibs, .pkg, .ebd, .ims, .emd, or .ems file.

*Usage Rules:* Revision level is set at the discretion of the engineer defining the file. The following guidelines are recommended:

0.x silicon and file in development

1.x pre-silicon file data from silicon model only

2.x file correlated to actual silicon measurements

3.x mature product, no more changes likely

*Example:*

[File Rev] 1.0 | Used for IBIS file variations

**In Section 6.3.6 :**

REPLACE

file formats except .ami (e.g., .ibs, .pkg, .ebd and .ims)

WITH (pages 118, 119, 139, 140)

file formats except .ami (e.g., .ibs, .pkg, .ebd, .ims, .emd, and .ems)

**Move Section 12 to Section 14 and Add a New Section 12?:**

**12 ELECTRICAL MODULE DESCRIPTION (EMD)**

**INTRODUCTION**

“Module” is a generic term describing a printed circuit board (PCB), multi-chip module (MCM), stacked die component, interposer, or substrate which can contain components or other modules, and which can connect to another board or module through a set of user-visible pins. The electrical connectivity of such a board or module-level component is described through an “Electrical Module Description”. An [EMD Model] defines an interconnect model between the external pin(s) of the module and the pins of the designators in the module. A designator is either an IBIS .ibs or an EMD .emd file.

For the purposes of the rest of this section, “module” shall mean PCB, MCM, stacked die, interposer, substrate or similar structure connecting EMD Models.

For example, a DIMM module is a module-level component that is used to attach several DRAM components on the PCB to another module through edge connector pins. An Electrical Module Description file (a .emd file) is defined to describe the connections of a module-level component between the module pins and its components on the module.

I/O pins in the EMD Pin List and the Designator Pin List that have the same signal\_name (or as applicable bus\_label) are considered connected. This assumption is due to the expectation that some EMD files will be generated automatically from computer aided design (CAD) layout databases. Each pin in a CAD database is associated with a CAD “net” (short for “network”), and when two pins are associated with the same CAD net, they are connected. Normally the signal\_name of EMD pins and designator pins will be the same as their associated CAD net in the layout database. An exception to this is when there are series terminations and/or parallel terminations. In this case the model maker can choose to either:

1. Combine two CAD nets into an extended net. All the pins in the two CAD nets will use the extended net name as their signal\_name in the EMD file. The termination resistor or capacitor would be included in the electrical model for this extended net. An extended net is defined as the list of EMD and designator pins associated with a common path through an electrical model.
2. Create separate interconnect models for each CAD net. The termination component must be assigned a designator in this case.

One of the features of an EMD file is to enable the EDA tool to generate all the extended nets.

What is and is not included in an EMD Model is defined by its boundaries, referred to here as interfaces. For the definition of interfaces, see the [EMD Model] keyword.

Usage Rules:

A .emd file is intended to be a stand-alone file, not referenced by or included in any .ibs, .ebd, or .pkg file. Electrical Module Descriptions are stored in a file whose name is <stem>.emd, where <stem> must conform to the naming rules given in Section **Error! Reference source not found.** of this specification. The emd extension is mandatory.

Contents:

A .emd file is structured like a standard .ibs file. It must contain the following keywords, as defined in IBIS: [IBIS Ver], [File Name], [File Rev], and [End]. It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright].

The actual module description is contained between the keywords [Begin EMD] and [End EMD], and includes the keywords listed below:

.emd file keywords

[Begin EMD]

[Manufacturer]

[Description]

[Number Of EMD Pins]

[EMD Pin List]

[End EMD Pin List]

      [EMD Parts]

[End EMD Parts]

      [EMD Designator List]

[End EMD Designator List]

[Designator Pin List]

[End Designator Pin List]

[Voltage List]

[End Voltage List]

[EMD Group]

[End EMD Group]

[End EMD]

[EMD Set] [EMD Set] keywords permitted within a .emd file and covered later

[Manufacturer]

[Description]

      [EMD Model]

      [End EMD Model]

[End EMD Set]

.ems file Keywords

[EMD Set]

[Manufacturer]

[Description]

      [EMD Model]

      [End EMD Model]

[End EMD Set]

**KEYWORD DEFINITIONS**

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [EMD Set] represents.

*Usage Rules:* The description shall fit on a single line and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keyword:* [Begin EMD]

*Required:* Yes

*Description:* Marks the beginning of an Electrical Module Description

*Usage Rules:* The keyword is followed by the name of the module-level component. The length of the component name must not exceed 40 characters in length, and blank characters are allowed. There must be a matching [End EMD] keyword.

*Other Notes:* Only one [Begin EMD] keyword is permitted in a .emd file. This is different than the similar rules for .ibs, .pkg, and .ebd file.

*Example:*

[Begin EMD] 16X8\_SIMM

*Keyword:* [Number Of EMD Pins]

*Required:* Yes

*Description:* Defines the number of EMD pins to expect. EMD pins are any externally accessible electrical connection to the module.

*Usage Rules:* The field must be a positive integer. The [Number Of EMD Pins] keyword must be positioned before the [EMD Pin List] keyword. This does not include the number of designator pins.

*Example:*

[Number Of EMD Pins] 128

*Keyword:* [EMD Pin List]

*Required:* Yes

*Description:* Defines the pin names of the user accessible pins. It also defines which pins are connected to power and ground.

*Sub-Params:* signal\_name, signal\_type, bus\_label

*Usage Rules:* Following the [EMD Pin List] keyword are four columns. The first column lists the pin name (in the data book this can also be called pin number). The second column lists the data book name of the signal connected to that pin. The third column is required if the pin is a rail pin or a no connect pin. The allowed values for this third column (as defined in Section 3.2 are:

POWER - reserved model name, used with power supply pins

GND - reserved model name, used with ground pins

NC - reserved model name, used with no-connect pins

Note, ‘NC’ is sometimes used for non-digital pins that cannot be described by IBIS functions.

The fourth column (bus\_label) is optional for rail pins (signal\_type POWER or GND). The bus\_label is a name given to a subset of the pins on a rails signal\_name. All pins that have the same bus\_label must have the same signal\_name. If the bus\_label column is not specified for signal\_type POWER or GND, then the bus\_label shall be assumed to be the signal\_name.

The [EMD Pin List] keyword shall be followed by the strings “signal\_name”, “signal\_type”, and “bus\_label” as column headings.

There must be as many pin\_name/signal\_name/bus\_label rows as there are pins given by the preceding [Number Of EMD Pins] keyword. Pin names must be the alphanumeric external pin names of the module. The pin names cannot exceed eight characters in length. As described in Section 3.2 the reserved words “GND”, “POWER”, and “NC” are case-insensitive.

All non-rail pins (generically referred to as I/O pins) are required to be listed and have only a signal\_name entry. No signal\_type or bus\_label entry is permitted. The signal\_name entry may be used to signify the primary connection to other I/O pins (necessary for Aggressor\_Only described later).

It is often convenient to merge multiple rail pins into a single interconnect model terminal. This may include all of the rail pins with the same signal\_name on the same interface, or all of the rail pins with the same bus label on the same interface. In this case, all of the pins that are merged together into a single terminal are “shorted”.

*Example:*

| A SIMM Module Example:

|

[Begin EMD] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of Pins] 6

[EMD Pin List] signal\_name signal\_type bus\_label

A1 GND GND

A2 DQ1 | I/O pin

A3 DQ2 | I/O pin

A4 POWER5 POWER Power5x

A5 RFU NC

A6 POWER3.3 POWER

[End EMD Pin List]

*Keyword:* **[End EMD Pin List]**

*Required:* Yes

*Description:* Indicates the end of the data after [EMD Pin List].

*Example:*

[End EMD Pin List]

*Keyword:* **[**EMD Parts]

*Required:* Yes, if [Designator Pin List] is defined below

*Description:* Maps an EMD part to an IBIS component or EMD module.

*Usage Rules:* The [EMD Parts] keyword shall be followed by a list of all the EMD parts (also called part numbers or part names in industry).Each EMD part is followed by the file reference of the .ibs or .emd file containing the electrical description of the component or board, then the name of the component itself as given by the .ibs or .emd file’s [Component] or [Begin EMD] keyword respectively.  While official names of parts are recommended, this is not required. The referenced .ibs or .emd files shall exist in the same directory as the calling .emd file or shall exist in a relative path under this directory.

For the context in thisElectrical Module Description section, a “part” declaration shall be one data line under [EMD Parts].

A part that is an .emd file can itself reference an EMD module. This shall be limited to 6 hierarchy levels of nested .emd files.

An EMD file may not reference itself directly or indirectly.

The EMD part, file reference, and component/define module name terms are separated by white space.

The EMD part is limited to forty characters.

Every part referenced in the EMD Designator List shall have one and only one entry in this list of parts.

NAs in the file reference and component/define module columns are permitted if the part has functionality outside of the scope of the IBIS specification, such as certain analog parts. The NA in the File reference column indicates that the part model is not available, although its pinout may be known and included as [Designator Pin List] entries.

It is also permitted to use a .ibs file and a component/define module name to show the part pinout and to document some known rails and digital I/O pins that are supported by IBIS. Pins whose functions are not supported by IBIS could be documented with NC or with Terminator models.

A [Notes] section or a separate readme file should document these unknown parts or parts where certain pins cannot be modeled in IBIS. Some EDA tools may deal with these special cases in a tool-specific manner.

*Example:*

[EMD Parts]

|

| part\_name file\_reference component/define\_module

Processor pp100.ibs Processor

Memory\_16X8 simm.emd 16X8\_SIMM

74LS244 ls244.ibs NoName\_74LS244

Res\_10K r10K.ibs My\_10K\_Pullup

|

ABC NA NA | Undocumented Parts

BCD NA NA | without files

|

C555 timer.ibs X555 | Timer with digital control

|

[End EMD Parts]

*Keyword:* **[End EMD** Parts**]**

*Required:* Yes

*Description:* Indicates the end of the data after [EMD Parts].

*Example:*

[End EMD Parts]

*Keyword:* **[**EMD Designator List]

*Required:* Yes, if [Designator Pin List] is defined below

*Description:* Maps an EMD designator to an IBIS component or EMD define module.

*Usage Rules:* The [EMD Designator List] keyword must be followed by a list of all the EMD designators (also called reference designators in industry). Each EMD designator is followed by a part name.

For the context in thisElectrical Module Description section, a “designator” shall be one line in the data following [EMD Designator List].

The EMD designator and part is separated by white space.

The EMD designator is limited to ten characters. “\*” is an illegal designator name.

*Example:*

[EMD Designator List]

|

| EMD Designator Part Name

u23 Processor

u24 Memory\_16X8

u25 74LS244a

u26 Res\_10K

[End EMD Designator List]

*Keyword:* **[End EMD Designator List]**

*Required:* Yes

*Description:* Indicates the end of the data after [EMD Designator List].

*Example:*

[End EMD Designator List]

*Keyword:* [Designator Pin List]

*Required:* Yes

*Description:* Defines the pin names of the designator pins. It also defines which designator pins are connected to power and ground. Designators are defined in the [EMD Designator List] section and can be instances of either an .ibs [Component] or an .emd [Begin EMD].

*Sub-Params:* signal\_name, signal\_type, bus\_label

*Usage Rules:* Following the [Designator Pin List] keyword are three columns. The first column lists the pin name (in data book this can also be called pin number). Designator Pins shall be the pin\_name preceded by the reference designator with a “.” inserted between the reference designator and the pin\_name (e.g. U2.DQ1).

The second column lists the name of the signal associated with the pin\_name. This signal\_name is the name that is assigned by the top-level EMD and may be reassigned from the signal\_names of the designator .ibs [Component] or of the designator .emd [Begin EMD]. This allows attached components or attached electrical module descriptions with standardized pin\_name positions but with different manufacturer terminology to be interchanged.

The third column is required if the pin is a rail pin or a no connect pin.

The allowed values for this third column are:

POWER - reserved model name, used with power supply pins

GND - reserved model name, used with ground pins

NC - reserved model name, used with no-connect pins

Note, ‘NC’ is sometimes used for non-digital pins that cannot be described by IBIS functions.

The fourth column, bus\_label, is optional for rail pins (signal\_type POWER or GND). The bus\_label entry is a name assigned to a subset of the pins with a rail signal\_name.

The optional bus\_label entry provides a way to describe some routing groupings such as left-hand and right-hand rail paths. If the bus\_label column is not specified for signal\_type POWER or GND, then the bus\_label shall be assumed to be the signal\_name.

The [Designator Pin List] keyword shall be followed by the strings “signal\_name”, “signal\_type”, and “bus\_label” as column headings.

Pin names must be the alphanumeric external pin\_names of the designator. The pin names cannot exceed eight characters in length. In addition, NC is a legal signal\_type and indicates that the pin is a “no connect”. As described in Section 3.2 the reserved words “GND”, “POWER”, and “NC” are case-insensitive.

Note that all EMD Pins and Designator Pins that have the same signal\_name (or subset bus\_label) are “connected”. Connection details between the EMD Pins and any Designator Pins are described by the electrical models under the [EMD Model].

All non-rail pin\_name pins (generically referred to as I/O pins) are required to be listed and have only a signal\_name entry. No signal\_type or bus\_label entry is permitted. The signal\_name entry may be assigned to designate I/O pins on .ibs [Component]s or .emd [Define EMD] that are associated with corresponding [EMD Pin List] I/O pins. In other words, the [EMD Pin List] pin\_names may be different than the corresponding pin\_names of the designator component, but the EMD-level assigned signal\_name entries are used for the association. This association will be useful when describing Aggressor\_Only terminals discussed later.

*Example:*

| A SIMM Module Example:

|

[Begin EMD] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of EMD Pins] 6

[EMD Pin List] signal\_name signal\_type bus\_label

A1 VSS GND

A2 DQ1 | I/O pin

A3 DQ2 | I/O pin

A4 VDD POWER VDD1

A5 VDD POWER VDD2

A6 VDDQ POWER

[End EMD Pin List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.11 VSS GND

U1.12 DQ1 | I/O pin

U1.13 DQ2 | I/O pin

U1.14 VDD POWER VDD1

U2.21 VDD POWER VDD2

U2.22 DQ1 | I/O pin

U2.23 DQ2 | I/O pin

U2.24 VDDQ POWER

[End Designator Pin List]

*Keyword:* [**End Designator Pin List**]

*Required:* Yes

*Description:* Indicates the end of the data after [Designator Pin List].

*Example:*

[End Designator Pin List]

*Keyword:* [Voltage List]

*Required:* No

*Description:* Defines the signal\_names or bus\_labels that are rail signals and their voltage values.

*Usage Rules:* Under the [Voltage List] keyword are four columns:

The first column lists the voltage rail name of a signal\_name or a bus\_label found within EMD Pin List or Designator Pin List.

The second column, V(typ), lists the typ value of the voltage. This entry is required.

The third column, V(min), lists the min (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

The fourth column, V(max) lists the max (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

Not all voltage rail names of signal\_names or bus\_labels found within EMD Pin List or Designator Pin List are required to be listed.

*Other Notes:* This keyword can be used in several ways:

* Provides information about expected voltage source values at [EMD Pin List] and [Designator Pin List] interfaces for any or all the rail signals. The EDA tool can override these values. This might occur in the following cases:
  + With a SPICE netlist that provides its own sources
  + If V(min) and V(max) values are not supplied (as might occur with a SPICE netlist and its sources)
  + With [Model] corner setting using the typ, min, and max sources that are declared within the [Model] keyword
* Declares external sources at the [EMD Pin List] and/or [Designator Pin List] interfaces for the named voltages.

Because the [Voltage List] entries may be incomplete or because V(min) and/or V(max) values may be omitted, combinations of the above options are permitted.

In simulation, [Voltage List] entries shall be selected along with the corresponding corner values in [Model] entries. That is, V(typ) values should be used with typ corner conditions, V(min) with min corner conditions, and V(max) with max corner conditions.

In a power aware simulation, voltages will be supplied by the EDA tool at the EMD pins from voltage sources in the board or module that uses the EMD.

*Example:*

[Voltage List]

| V(name) V(typ) V(min) V(max)

VSS 0.0 0.0 0.0

VDD 1.2 1.1 1.3

[End Voltage List]

*Keyword:* [**End Voltage List**]

*Required:* Yes

*Description:* Indicates the end of the data after [Voltage List].

*Example:*

[End Voltage List]

*Keyword:* [EMD Group]

*Required:* Yes

*Description:*  [EMD Group] has a single argument, which is the name of the associated EMD Group. The length of the EMD Group name shall not exceed 40 characters in length. Blank characters are not allowed. The [EMD Group]/[End EMD Group] keyword pair is hierarchically scoped by the [Begin EMD]keyword. The [EMD Group] keyword is used to define a list of [EMD Set]s by name that shall be used together to define EMD Models to be used in a simulation. A simulation may contain EMD Models from the EMD Sets listed in only one Group.

*Usage Rules:* [Begin EMD] must contain one or more [EMD Group] keywords (identified by a name). Each [EMD Group] must contain at least one [EMD Set] name. EMD Sets contain EMD Models used to describe EMD pin or IBIS designator pin connections to IBIS-ISS subcircuits or n-port networks described by Touchstone files.

EMD Sets that exist for the module shall be listed in one or more EMD Groups. An EMD Group is required even if it references only one EMD Set.

The section under the [EMD Group] keyword shall have two entries per line, with each line identifying one EMD Set associated with the module. The entries shall be separated by at least one white space. The first entry lists the EMD Set name (up to 40 characters long). The second entry is the file reference of the file containing the EMD Set and shall have the extension “ems”. This file reference shall conform to the rules given in Section 3, ‘GENERAL SYNTAX RULES AND GUIDELINES’. If the EMD Set is in the same .ibs file as [Begin EMD], then the second entry shall be “NA”.

The files containing the EMD Sets with the “ems” extension shall be located in the same directory as the .emd file or in a specified directory under the .emd file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’ (i.e., a file reference containing a relative path to a directory below that of the referencing .emd file is permitted). An EMD Set with matching name shall be found in the stated location for each EMD Set named in the [EMD Group] keyword.

Each EMD Set name and its file\_reference may only appear once under each [EMD Group] keyword for a given designator.

Refer to Section 13.6 for connection rules and limitations on the permissible EMD Set links under each [EMD Group] keyword and after some more terms and rules related to [EMD Set] and [EMD Model] keywords are presented.

**TEXT UP TO *Examples:* DELETED AND MOVED TO THE END AFTER TABLE 41 to begin Section 13.6 TO BE MERGED WITH OTHER TEXT**

*Examples:*

| Example 1

|

[EMD Group] Full\_ISS\_PDN\_1

| EMD Set file\_reference

Full\_ISS\_PDN\_1 NA | The [EMD Set] is

| present in the .emd file for

| all pins

[End EMD Group]

|

| Example 2

|

[EMD Group] Full\_ISS\_PDN\_sn\_2

| EMD Set file\_reference

Full\_ISS\_PDN\_sn\_2 NA | The [EMD Set] is

| present in the .emd file for

| all I/O pins and PDN

[End EMD Group]

*Keyword:* **[End EMD Group]**

*Required:* Yes, for each instance of the [EMD Group] keyword

*Description:* Indicates the end of the data for one [EMD Group].

*Example:*

[End EMD Group]

*Keyword:* [End EMD]

*Required:* Yes

*Description:* Marks the end of a module.

*Usage Rules:* This keyword must come at the end of each complete module description.

*Example:*

[End EMD]

**ADD a New Section 13?:**

**13 EMD SET AND EMD MODEL DESCRIPTION**

**13.1 EMD SET KEYWORD DESCRIPTION**

*Keyword:* [EMD Set]

*Required:* No

*Description:* Used to contain EMD Models

*Usage Rules:* [EMD Set] has a single argument, which is the name of the EMD Set. The length of the EMD Set name shall not exceed 40 characters in length. Blank characters are not allowed. The [EMD Set]/[End EMD Set] keyword pair is hierarchically equivalent in scope to [Begin EMD].

The section under the [EMD Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more EMD Models. See the section [EMD Model] for a description of the content of each EMD Model.

An EMD Set contains a list of EMD Models that have a logical association such as:

* All signals in a bus (e.g. DDR4, or PCIeG3)
* Full PDN structures from EMD pins to designator pins
* Full PDN structures from EMD pins to EMD pins
* All I/O structures between EMD pins and designator pins
* I/O structures from designator pins to designator pins
* Combinations of I/O and PDN structures
* Coupled models
* Touchstone electrical models
* Decoupling capacitor models
* IBIS-ISS electrical models

*Example:*

[EMD Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O buffer

[EMD Model] DQ1

…

[End EMD Model]

[EMD Model] DQ2

…

[End EMD Model]

[EMD Model] DQS

…

[End EMD Model]

[End EMD Set]

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [EMD Set] represents.

*Usage Rules:* The description shall fit on a single line and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keyword:* [**End EMD Set**]

*Required:* Yes, for each instance of the [EMD Set] keyword.

*Description:* Indicates the end of the EMD Set data.

*Example:*

[End EMD Set]

**13.2 GENERAL EMD SET AND EMD MODEL FILE SYNTAX REQUIREMENTS**

Terminal lines under the [EMD Model] keyword describe connections.

Pin\_name in this context is either the pin\_name in the [EMD Pin List], or designator.pin\_name in the [Designator Pin List] for designator pins.

I/O terminals shall be connected using only the pin\_name qualifier.

Rail terminal connections have more options to support direct connections to terminals or to groups of terminals using pin\_name, signal\_name, or bus\_label. The rail terminal can connect to:

* a specific designator or [EMD Pin List] rail pin\_name
* all the designator pins of a rail signal\_name within a designator
* all designator pins of a rail bus\_label within a designator
* all the [EMD Pin List] rail pins of a rail bus\_label

One or more EMD Sets may be included in a separate EMD Set file, using a file name with the extension “ems”, or within the .emd file. The [EMD Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [EMD Model] keywords and the [EMD Model] associated subparameters, as listed in Table 40.

TableError! Reference source not found. 40 – EMD Set and EMD Model Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [EMD Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [EMD Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End EMD Model] | (note 7) |
| [End EMD Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [EMD Set].  Note 2 At least one [EMD Model] is required for each [EMD Set].  Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.  Note 4 This subparameter shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.  Note 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.  Note 6 See text below.  Note 7 Required when the [EMD Model] keyword is used.  Note 8 Required when the [EMD Set] keyword is used. | |

When EMD Set definitions occur within a .emd file, their scope is “local”— they are known only within that .emd file and no other .emd file.

Usage Rules for the .ems file:

EMD Models are stored in a file whose file name uses the format:

<stem>.ems

The <stem> provided shall adhere to the rules given for the [File Name] keyword. Use the “ems” extension to identify files containing EMD Models. The .ems file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Begin EMD] and [Model] keywords are not allowed in the .ems file. The .ems file is for EMD Models only.

**13.3 GENERAL EMD MODEL KEYWORD DESCRIPTION**

*Keyword:* [EMD Model]

*Required:* Yes

*Description:* Marks the beginning of an Electrical Module Description that is used to define the interfaces to IBIS-ISS subcircuit or Touchstone files.

*Sub-Params:* Unused\_port\_termination, Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [EMD Model] has a single argument, which is the name of the associated EMD Model. The length of the EMD Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [EMD Model]/[End EMD Model] keyword pair is hierarchically scoped by the [EMD Set]/[End EMD Set] keywords.

The [EMD Model]/[End EMD Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an EMD Model, as well as defining the terminals and terminal usage for the EMD Model in the context of the given [Begin EMD].

An [EMD Model] may contain any combination of designator pins and [EMD Pin List] pins.

An [EMD Model] may contain terminals in the following combinations:

* one or more rails only
* one or more I/O signals
* one or more rails and one or more I/O signals
* one or more rails at the EMD Pin List interface only
* one or more rails at the Designator Pin List interface only

The following subparameters are defined:

Param

File\_IBIS-ISS

File\_TS

Unused\_port\_termination

Number\_of\_terminals = <value>

In addition to these subparameters, the [EMD Model]/[End EMD Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no EMD Model subparameter requires the presence of any other subparameter.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3.2, “SYNTAX RULES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

| into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [EMD Model]/[End EMD Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_reference and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_reference shall be located in the same directory as the referencing .emd file or .ems file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .emd or .ems file is permitted).

*Example:*

| file\_type file\_reference circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [EMD Model]/[End EMD Model] group.File\_TS is followed by one unquoted string argument, which is the file\_reference for a Touchstone file. The Touchstone file under file\_reference shall be located in the same directory as the referencing .emd file or .ems file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .emd or .ems file is permitted).

*Example:*

| file\_type file\_reference

File\_TS typ.s8p

Unused\_port\_termination rules:

The Unused\_port\_termination subparameter is required under this condition:

File\_TS is used and the number of terminal lines (described below) is less than N+1 (where N is the number of ports in the Touchstone file)

Unused\_port\_termination is illegal under these conditions:

File\_IBIS-ISS is used.

File\_TS is used and the number of terminal lines is N+1

If required, only one Unused\_port\_termination subparameter may appear for a given [EMD Model] keyword.

The Unused\_port\_termination subparameter is followed by white space and one of these arguments:

Open

Reference

Resistance

“Open” declares that the unused ports remain unterminated (open-circuited).

“Reference” declares that the EDA tool terminates all unused ports with resistors whose resistance values are equal to the reference impedances provided in the Touchstone file for the respective unused ports, and all connected to the model’s reference terminal.

“Resistance” declares that the EDA tool terminates all unused ports with resistors, all having the same value, and all connected to the model’s reference terminal. The “Resistance” entry is followed by a third column entry with the (non-negative) numerical resistance value.

*Examples:*

Unused\_port\_termination Open

Unused\_port\_termination Reference

Unused\_port\_termination Resistance 43.5

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the EMD Model. The subparameter name shall be followed by a single integer argument on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

Only one Number\_of\_terminals subparameter may appear for a given [EMD Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given EMD Model.

For File\_IBIS-ISS, the Number\_of\_terminals value shall be equal to the number of subcircuit terminals for an IBIS-ISS subcircuit. Because an IBIS-ISS subcircuit requires at least one terminal the Number\_of\_terminals value shall be 1 or greater. The IBIS-ISS subcircuit terminals shall not contain an ideal reference node (SPICE node 0 or its synonyms).

For File\_TS, the Number\_of\_terminals value shall be a value equal to N+1 (where N is the number of ports in the Touchstone file). Because a Touchstone file requires at least one port, the Number\_of\_terminals value shall be 2 or greater.

*Example:*

Number\_of\_terminals = 3

Terminal line rules:

The terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End EMD Model] keyword.

Terminal lines are of the following form, with each identifier separated by whitespace:

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

The Terminal\_number is the identifier for a specific terminal. The value shall be 1 or greater and less than or equal to the Number\_of\_terminals. The same Terminal\_number shall not appear more than once for a given EMD Model.

For File\_IBIS-ISS, the Terminal\_number entry shall match the IBIS-ISS terminal (node) position. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. Each IBIS-ISS terminal shall have a terminal line entry.

For File\_TS, the Terminal\_number entry shall match the Touchstone file port number or reference terminal line, as shown below. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. The terminal line for Terminal\_number N+1 is required as a reference terminal for each port and shall be connected to a rail terminal or A\_gnd in the EMD Model. At least one other terminal line entry is required.

* Terminal\_number Port
* 1                     1
* 2                          2
* …
* N                        N
* N+1 Reference terminal for the Touchstone file

For Touchstone files, each unused port and its corresponding Terminal\_number shall be terminated in simulation with a resistor whose value corresponds to the Unused\_port\_termination subparameter entry. The resistor is connected to the model’s reference terminal.

Terminal\_type  
The Terminal\_type is a string that identifies whether the terminal is a reference, supply or I/O terminal and whether the terminal is connected to a EMD pin or designator pin. (Note that “I/O” in this context is a synonym for “signal”, as opposed to “supply” or “rail”; it is not intended to imply model type as used in the “Model\_type” subparameter).

Terminal\_type A\_gnd defines a connection to the simulator global reference node.  The A\_gnd node can be used at any interface.

Terminal\_type A\_gnd is not required under File\_TS or File\_IBIS-ISS.

If present under File\_TS, Terminal\_type A\_gnd may be used only once on the N+1th terminal line.

If present under File\_IBIS-ISS, Terminal\_type A\_gnd may be used any number of times on any of the terminal lines.

Furthermore, if the terminal is connected to a buffer supply rail, the Terminal\_type identifies to which specific buffer rail the terminal is connected. The Terminal\_type shall be one of the following:

* Pin\_I/O
* Pin\_Rail
* A\_gnd

Terminal\_type\_qualifier   
Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name or bus\_label in the [EMD Pin List], or specific pin\_name, signal\_name, or bus\_label in the [Designator Pin List].

Qualifier\_entry   
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

bus\_label <bus\_label\_entry>

Terminal\_type A\_gnd defines a connection to the simulator global reference node. The A\_gnd node can be used at any interface.

Terminal\_type A\_gnd is not required under File\_TS or File\_IBIS-ISS.

If present under File\_TS, Terminal\_type A\_gnd may be used only once on the N+1th terminal line.

If present under File\_IBIS-ISS, Terminal\_type A\_gnd may be used any number of times on any of the terminal lines.

Terminal\_type\_qualifier   
The Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name, or bus\_label.

Aggressor\_OnlyThe Aggressor\_Only entry is optional and is indicated by the string “Aggressor\_Only” without the quotation marks. Assigning Aggressor\_Only to a pin assigns the Aggressor\_Only properties to all pins of the same signal\_name listed in the [EMD Pin List] and [Designator Pin List] keywords.

Any \*\_I/O Terminal\_type without the Aggressor\_Only column may be considered as an aggressor or a victim.

Multi-line EMD Models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line EMD Model). As a result, while the interconnects at the edges of the EMD Model may induce crosstalk onto other interconnects nearby, being on the edge of the EMD Model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure.

**13.4 TERMINAL\_TYPE ASSOCIATIONS FOR EMD AND DESIGNATOR PINS**

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. Terminals may be at EMD or designator pin interfaces. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the EMD Model subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry, and there is an optional fifth column “Aggressor\_Only”.
* The second column, Terminal\_type is:
  + For I/O connections
    - Terminal\_type must be Pin\_I/O
    - Terminal\_type\_qualifier shall be pin\_name
      * EMD Pins shall be a pin\_name in the [EMD Pin List] list
      * Designator Pins shall be in the form from the [Designator Pin List]:
        + <designator>.< pin\_name>
  + For rail connections
    - Terminal\_type shall be Pin\_Rail
    - Terminal\_type\_qualifier shall be one of the following:
      * pin\_name
        + Qualifier\_entry shall be a rail pin\_name in the [EMD Pin List] or [Designator Pin List] and with signal\_type POWER or GND
      * signal\_name
        + Qualifier\_entry shall be a rail signal\_name in the [EMD Pin List] or of the form <designator\_name>.<signal\_name> entry from the [Designator Pin List]
        + For the [EMD Pin List] entry, the signal\_name should match the data book entry
        + For [Designator Pin List] entries, the signal\_name values can be assigned so that they can be associated with the same signal\_name entries on the [EMD Pin List]. The signal\_name entries do not have to be the same as those in the [EMD Designator List], [Component], or [Define EMD] entries.
        + \*.<signal\_name> shall represent all of the [Designator Pin List] <signal\_name> entries at all [Designator Pin List] interfaces shorted together.
      * bus\_label
        + Qualifier\_entry shall be a rail bus\_label in the [EMD Pin List] or [Designator Pin List]
        + Pin\_Rail bus\_label U7.VDD …
        + The bus\_label entry can be assigned to both the [EMD Pin List] and [Designator Pin List] entries to support a subset of connections that might be associated with a common signal\_name. For example, left-side routing and right-side routing might be isolated from each other.
        + \*.<bus\_label> shall represent all of the [Designator Pin List] <bus\_label> entries at all [Designator Pin List] interfaces shorted together.
    - At any interface
      * Terminal\_type A\_gnd is available at any interface and without any Terminal\_type qualifier

Table 41 summarizes the rules described above and applies to terminals associated with the [EMD Pin List] keyword and with the [Designator Pin List] keyword.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | | | **Aggressor\_Only** |
| --- | --- | --- | --- | --- |
| **pin\_name** | **signal\_name** | **bus\_label** |
| Pin\_I/O | X |  |  | A |
| Pin\_Rail | Y | Y | Y |  |
| Pin\_Rail |  | \*.Y2 | \*.Y2 |  |
| A\_gnd |  |  |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” indicates POWER and GND terminals. The letter “A” designates "Aggressor\_Only".
2. “\*.Y” indicates that all of the “Y” named POWER and GND terminals on each of the [Designator Pin List] interfaces are shorted together

**13.5 RDIMM EXAMPLE ILLUSTRATING SYNTAX AND NET OPTIONS**

**13.5.1 RDIMM Figures for Examples in 13.5.2 thru 13.5.4**

Figure X shows a DDR4 Registered DIMM containing DRAM components labeled by designators U1, U2, U4, U5 (front side) and U7-U11 (back side, not seen) and a Register component labeled by designator U3.

Also shown is pre-register Net A07 connecting from an EMD Pin to a Designator Pin of designator U3 and post-register net BA07 connecting from a Designator Pin of designator U3 to Designator Pins of designators U4, U5, U7, and U8 as well as termination resistor RN13 connecting to the VTT rail.



Figure X

Figure Y (Example 1), a zoomed in area of Figure X, shows an example of an extended net. The extended net A07 can be modeled two ways:

1. One EMD Model defining only terminals for EMD Pin 211 and Designator Pin U3.W1. The EMD Model contains the complete signal path of net A07, the series resistor R123, and net A07r combined as part of the A07.iss electrical model A07\_1) (Example 1)
2. One EMD Model or multiple EMD Models contained with an EMD Set that include terminals for EMD Pin 211 and Designator Pin U3.W1 and two terminals for the pins of the series resistor. The resistor would be assigned a designator (R123) referencing an IBIS component. (Examples 2, 3) The connection between Net A07 and Net A07r through R123 might be determined automatically in some EDA tools or entered manually. Or Net A07 and Net A07r can be treated as two independent nets.



Figure Y

Figure Z (Examples 2, 3), a zoomed in area of Figure X, shows an example of an internal net. The post-register net BA07 connects from the register’s Designator Pin U3.B11 to the DDR4 DRAMs’ Designator Pins U4.M8, U5.M8, U7.M8, and U8.M8 as well as to one Designator Pin of the termination resistor RN13. RN13 terminates the signal to the VTT rail.



Figure Z

**13.5.2 Example 1 (R123 and RN13 Embedded in A07\_1 and BA07\_1)**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 1 (Net A07 with Embedded Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM\_1

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_1

Addr\_07\_1 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_1

[EMD Model] A07\_1

File\_IBIS-ISS A07.iss A07\_1

Number\_of\_terminals = 6

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name U3.W1 | Connection from 211 to U3.W1 includes

| Series Resistor modeled in A07.iss A07\_1

3 Pin\_Rail bus\_label VDD1

4 Pin\_Rail signal\_name VSS

5 Pin\_Rail bus\_label U3.VDD1

6 Pin\_Rail bus\_label U3.VSS

[End EMD Model]

[EMD Model] BA07\_1

File\_IBIS-ISS A07.iss BA07\_1

Number\_of\_terminals = 19

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8 | Termination Resistor to VTT

| included in A07.iss BA07\_1

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail signal\_name VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.5.3 Example 2 (R123 and RN13 modeled as separate IBIS components in A07\_2, BA07\_2)**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 2 (External Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM\_2

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07         |Net A07 Connection

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22ohms

510-501618 resistors.ibs RPACK4\_33ohms

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07r | Net A07r Terminal

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

|

R123.1 A07 | Net A07 Terminal

R123.2 A07r | Net A07r Terminal

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_2

Addr\_07\_2 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_2

[EMD Model] A07\_2

File\_IBIS-ISS A07.iss A07\_2

Number\_of\_terminals = 8

1 Pin\_I/O pin\_name 211 | Net A07 Terminal and Connection

2 Pin\_I/O pin\_name R123.1 | Net A07 Terminal and Connection

3 Pin\_I/O pin\_name R123.2 | Net A07r Terminal and Connection

4 Pin\_I/O pin\_name U3.W1 | Net A07r Terminal and Connection

5 Pin\_Rail bus\_label VDD1

6 Pin\_Rail signal\_name VSS

7 Pin\_Rail bus\_label U3.VDD1

8 Pin\_Rail signal\_name U3.VSS

[End EMD Model]

[EMD Model] BA07\_2

File\_IBIS-ISS A07.iss BA07\_2

Number\_of\_terminals = 19

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

16 Pin\_I/O pin\_name RN13.7

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail signal\_name RN13.VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.5.4 Example 3 (R123 IBIS Model Terminals split into two [EMD Model]s, POWER Rails in a Separate [EMD Model]**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 3 (External Resistors, Separate A07, A07R, and POWER

| Models)

| Using DDR4 RDIMM Example

|

[Begin EMD] DDR4\_RDIMM\_3

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22ohms

510-501618 resistors.ibs RPACK4\_33ohms

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07r | Net A07r Terminal

U3.W3 VSS GND

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

R123.1 A07 | Net A07 Terminal

R123.2 A07r | Net A07r Terminal

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_3

Addr\_07\_3 NA

RIGHT\_SIDE\_POWER NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_3

[EMD Model] A07\_3

File\_IBIS-ISS A07.iss A07\_3

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name R123.1 | Net A07 Terminals and Connection

| Series Resistor is in two [EMD Model]s

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] A07R\_3

File\_IBIS-ISS A07.iss A07R\_3

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name R123.2 | Net A07r Terminal and Connection

2 Pin\_I/O pin\_name U3.W1 | Net A07r Terminal and Connection

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] BA07\_3

File\_IBIS-ISS A07.iss BA07\_3

Number\_of\_terminals = 13

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail signal\_name U3.VSS

3 Pin\_I/O pin\_name U4.M8

4 Pin\_Rail signal\_name U4.VSS

5 Pin\_I/O pin\_name U5.M8

6 Pin\_Rail signal\_name U5.VSS

7 Pin\_I/O pin\_name U7.M8

8 Pin\_Rail signal\_name U7.VSS

9 Pin\_I/O pin\_name U8.M8

10 Pin\_Rail signal\_name U8.VSS

11 Pin\_I/O pin\_name RN13.7

12 Pin\_Rail signal\_name RN13.VTT

13 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

[EMD Set] RIGHT\_SIDE\_POWER

[EMD Model] RIGHT\_SIDE\_VDD1\_VTT\_VSS

File\_IBIS-ISS rdimm\_power.iss RIGHT\_SIDE\_VDD1\_VTT\_VSS

Number\_of\_terminals = 14

1 Pin\_Rail bus\_label VDD1

2 Pin\_Rail signal\_name VSS

3 Pin\_Rail signal\_name VTT

4 Pin\_Rail bus\_label U3.VDD1

5 Pin\_Rail signal\_name U3.VSS

6 Pin\_Rail bus\_label U4.VDD1

7 Pin\_Rail signal\_name U4.VSS

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_Rail bus\_label U7.VDD1

11 Pin\_Rail signal\_name U7.VSS

12 Pin\_Rail bus\_label U8.VDD1

13 Pin\_Rail signal\_name U8.VSS

14 Pin\_Rail signal\_name RN13.VTT

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.6 CONNECTION RULES FOR EMD GROUP, EMD SET, AND EMD MODEL**

At the [EMD Group] level, the connections between the referenced [EMD Set]s (and their encapsulated [EMD Model]s are determined by the following rules:

1. I/O pins (Pin\_I/O terminals by pin\_name entries)
   1. Without Aggressor\_Only:
      1. I/O terminals may exist with or without rail terminals
      2. Within each [EMD Model], pin\_name entries shall be distinct, and signal\_name entries shall be distinct for I/O pins
      3. Within each [EMD Model], <designator>.<pin\_name> and their corresponding signal\_name entries (as listed in the [Designator Pin List] keyword) shall be distinct for I/O pins
      4. At any one interface and for all [EMD Model]s referenced by all [EMD Set]s under an [EMD Group], no duplicate pin\_name entries are permitted for I/O pins
      5. Electrical connections between I/O pins are based on the content of the referenced electrical models (\*.iss or Touchstone files)
      6. Net connections are indicated by identical signal\_name entries available from the [EMD Pin List] and/or [Designator Pin List] entries. For example, Pin\_I/O pin\_name 211 and Pin\_I/O pin\_name U3.W1 are considered connected through the IBIS-ISS subcircuit because they both share the same signal\_name, A07 in Example X (Example 1)
      7. The logical and electrical connections can span several interfaces. In Example X, Pin\_I/O pin\_name U3.W1, Pin\_I/O pin\_name U4.W1, etc. share the same signal\_name BA07 and are therefore in the same net
   2. With Aggressor\_Only:
      1. I/O terminals may exist with or without rail terminals
      2. To permit selection of nets within an [EMD Group], identical pin\_name entries are permitted in different [EMD Model] keywords as long as there is no overlap of pin\_name entries at the same interface without Aggressor\_Only. For example, “Pin\_I/O pin\_name 211” and “Pin\_I/O pin\_name 211 Aggressor\_Only” can exist under different [EMD Model] keywords
      3. The complete I/O net for a given signal\_name entry is deemed Aggressor\_Only if one or more of the pin\_names in the net has an Aggressor\_Only column entry
      4. At least one net shall exist without Aggressor\_Only
2. Rail (Pin\_Rail terminals) connections by pin\_name, signal\_name, bus\_label
   1. Within an [EMD Group] and for all referenced [EMD Set] keywords and their encapsulated [EMD Model] keywords, identically-named rail terminals shall be considered connected based on these rules:
      1. Rail terminals may exist with or without I/O terminals
      2. At an EMD Pin List interface, identical Pin\_Rail pin\_name, bus\_label or signal\_name entries in different [EMD Model]s shall be considered shorted
      3. At a Designator Pin List interface, identical Pin\_Rail pin\_name, bus\_label, or signal\_name entries in different [EMD Model]s shall be considered shorted
      4. For each [EMD Model] and at any one interface, there shall not be any overlap of Pin\_Rail pin\_name, bus\_label and signal\_name entries:
         1. A pin\_name entry shall not overlap with a bus\_label entry
         2. A pin\_name entry shall not overlap with a signal\_name entry
         3. A bus\_label entry shall not overlap with a signal\_name entry
      5. For all [EMD Model]s and at any one interface, where Pin\_Rail pin\_name, bus\_label and/or signal\_name entries in different [EMD Model]s overlap:
         1. A pin\_name entry shall be shorted with a corresponding bus\_label entry
         2. A pin\_name entry shall be shorted with a corresponding signal\_name entry
         3. A bus\_label entry shall be shorted with a corresponding signal\_name entry
   2. Within an [EMD Group] and for all referenced [EMD Set] keywords and their encapsulated [EMD Model] keywords, Pin\_Rail terminals are considered merged into a single terminal across designator interfaces (not the EMD interface) based on these rules:
      1. Pin\_Rail signal\_name \*.<signal\_name> shorts all connections with signal\_name <signal\_name> for all designator interfaces (not the EMD interface)
      2. Pin\_Rail bus\_label \*.<bus\_label> shorts all connections with bus\_label <bus\_label> for all designator interfaces (not the EMD interface)
      3. No corresponding rule for pin\_name entries exists since connected rail pin\_names can differ at different interfaces
   3. Simulator Global Reference:
      1. Terminal\_type A\_gnd can be used for a simulator global reference in any EMD Model
      2. All simulator global references are shorted

-------------------------------------------------------------------------

**DELETE - COPIED FROM EMD GROUP SECTION FOR REFERENCE**

* I/O pin\_name rules
  + A Power Delivery Network (PDN) has one or more connections of rail terminals between EMD terminals and designator terminals.
  + An EMD Model with only rail terminals and two interfaces (no I/O terminals) can be used for a PDN.
  + An EMD Model with only rail terminals (no I/O terminals) and only one interface is permitted for applications such as for modeling rail decoupling circuits.
  + A PDN structure can also exist in an EMD Model with I/O terminals.
  + Rail terminals or A\_gnd can be used in EMD Models to provide a reference node for the electrical interconnections associated with \*\_I/O terminals.
* Rail terminal rules
  + At the pin interface, a rail pin\_name may appear on a terminal line whose Terminal\_type is Pin\_Rail in multiple EMD Models in the EMD Group.
  + A rail terminal in EMD Models can represent a list of EMD pins shorted together, a list of designator pins from one designator shorted together or a list of designator pins from all designators shorted together.

Note that these rules apply to the complete list of EMD Models that are included in each EMD Group, regardless of which EMD Sets contain the EMD Models.

All EMD Models with only rail terminals are available for power delivery simulations.

**ANOTHER WRITEUP TO UPDATE AND INTEGRATE WITH ABOVE**

An [EMD Model] can support terminals from one or more interfaces including those listed in the [EMD Pin List] and/or those listed in the [Designator Pin List].

For I/O terminals, the pin\_name value shall not be repeated at any one interface.  For rail terminals, the rail terminal name shall not be repeated at any one interface.  Also, a rail terminal name that overlaps with another rail terminal name (expressed as pin\_name, bus\_label, signal\_name) shall not be entered at any one interface.  For example, if the [EMD Pin List] keyword contains the following row:

[EMD Pin List]

…

10  VDD POWER

…

then signal\_name VDD overlaps with pin\_name 10.  So, Terminal\_type lines “Pin\_Rail signal\_name VDD” and “Pin\_Rail pin\_name 10” shall not both be entered in a single EMD Model.

For EMD Groups that reference EMD Sets containing several EMD Models, the Terminal\_types at the same interface are considered connected if the terminal names match. For different interfaces,  I/O terminals that share the same signal\_name (as listed in the [EMD Pin List] or [Designator Pin List])  are considered associated with each other and would normally be connected by an electrical model.  The association is used when applying Aggressor\_Only rules.   At least one I/O terminal with the same signal\_name at all of the interfaces documented in the EMD Model shall NOT have the Aggressor\_Only entry.

For I/O terminals in an EMD Group that references EMD Sets, a connection exception exists.  The encapsulated EMD Models can have identical I/O terminals (same signal\_names) at the same interfaces.  However, the EMD Models  would not be used together in simulation because of different Aggressor\_Only entries.  This is illustrated in Figure 47\_XXXX and Figure 48\_XXXX above.   The Aggressor\_Only entry at one interface applies to the full path.  For an EMD Group only one full I/O path (as determined by identical signal names) without any Aggressor\_Only entries shall exist for a combination of EMD Models.  One or more unused EMD Models might be used for another selected I/O terminal if its full path does not contain the Aggressor\_Only entry.  The rails connections and paths in the unused EMD Models are also not used.

In the examples below, the EMD Models have unique Terminal\_type names at each interface. Some examples illustrate several EMD Models within an EMD Set with identical or overlapping Terminal\_type names. During simulations, the EDA tool should connect these terminals.  Comment names show signal\_names for associating I/O terminals

**DELETE, REPLACE, OR INTEGRATE BELOW WITH ABOVE**

Pins may be terminals of the EMD Model that connect directly to a PCB or other type of system connection to an IBIS designator. Pins can be signal pins (Pin\_I/O), or supply pins (Pin\_Rail). An EMD Model can connect supply pins in one of several ways:

1. By specifying terminals for some or all the supply pins.
2. By assuming that all supply pins connected to a supply signal\_name are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins that are connected to a specific signal\_name on at least one supply pin.
3. By assuming that all supply pins connected to a supply signal\_name on a specific designator are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for one or more designator.pin\_names in one or more than one component.
4. By assuming that all supply pins connected to a supply bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins that are connected to a specific bus\_label on at least one supply pin.
5. By assuming that all supply pins connected to a supply bus\_label on a specific designator are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for one or more designator.pin\_names in one or more than one component.
6. Any one pin shall not be included in more than one terminal of an EMD Model.

**END REWRITE AND DELETIONS**

*Examples:*

[Begin EMD] DIMM

[Number of EMD Pins] 9

[EMD Pin List] signal\_name signal\_type bus\_label

A1    DQ1

A2    DQ2

A3    DQ3

D1    DQS+

D2    DQS-

P1    VDD         POWER VDD1

P2    VDD         POWER

G1    VSS         GND

[End EMD Pin List]

[EMD Designator List]

U1 mem.ibs Memory

U2 mem.ibs Memory

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.1 VDD POWER VDD1

U1.2 VDD POWER

U1.3 VSS GND

U1.4 VSS GND

U1.5 DQ1

U1.6 DQ2

U1.7 DQ3

U1.8 DQS+

U1.9 DQS-

|

U2.1 VDD POWER VDD1

U2.2 VDD POWER

U2.3 VSS GND

U2.4 VSS GND

U2.5 DQ1

U2.6 DQ2

U2.7 DQ3

U2.8 DQS+

U2.9 DQS-

[End Designator Pin List]

[EMD Group] Just\_One

SomeDQ NA

[End EMD Group]

[End EMD]

[EMD Set] SomeDQ

[EMD Model] DQ1

File\_IBIS-ISS DQ1.iss DQ1

Number\_of\_terminals = 8

1  Pin\_I/O      pin\_name A1

2  Pin\_I/O      pin\_name U1.5

3  Pin\_I/O      pin\_name U2.5

4 Pin\_Rail bus\_label VDD1

5 Pin\_Rail signal\_name VSS

6 Pin\_Rail pin\_name U1.1

7 Pin\_Rail pin\_name U1.3

8 Pin\_Rail pin\_name U2.1

[End EMD Model]

[EMD Model] VDD\_bus\_label

File\_IBIS-ISS VDD\_bus\_label.iss VDD\_bus\_label

Number\_of\_terminals = 6

1 Pin\_Rail bus\_label VDD | EMD Pin P2

2 Pin\_Rail bus\_label VDD1 | EMD Pin P1

3 Pin\_Rail bus\_label U1.VDD | U1 Pin 2

4 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

5 Pin\_Rail bus\_label U2.VDD | U2 Pin 2

6 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

[End EMD Model]

[EMD Model] VDD\_signal\_name

File\_IBIS-ISS VDD\_signal\_name.iss VDD\_signal\_name

Number\_of\_terminals = 3

1 Pin\_Rail signal\_name VDD | EMD Pins P1 P2

2 Pin\_Rail signal\_name U1.VDD | U1 Pins 1 2

3 Pin\_Rail signal\_name U2.VDD | U2 Pins 1 2

[End EMD Model]

[EMD Model] VDD\_signal\_name\_merged\_pin

File\_IBIS-ISS VDD\_signal\_name.iss VDD\_signal\_name

Number\_of\_terminals = 3

1 Pin\_Rail signal\_name VDD | EMD Pins P1 P2

2 Pin\_Rail signal\_name U1.VDD | U1 Pins 1 2

3 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

[End EMD Model]

[EMD Model] VDD\_signal\_name\_merged\_all

File\_IBIS-ISS VDD\_signal\_name.iss VDD\_signal\_name

Number\_of\_terminals = 2

1 Pin\_Rail signal\_name VDD | EMD Pins P1 P2

2 Pin\_Rail signal\_name \*.VDD | All designator pins

[End EMD Model]

[End EMD Set]

*Keyword:* [End EMD Model]

*Required:* Yes

*Description:* Marks the end of an EMD Model.

*Usage Rules:* This keyword must come at the end of each complete electrical EMD Model.

*Example:*

[End EMD Model]