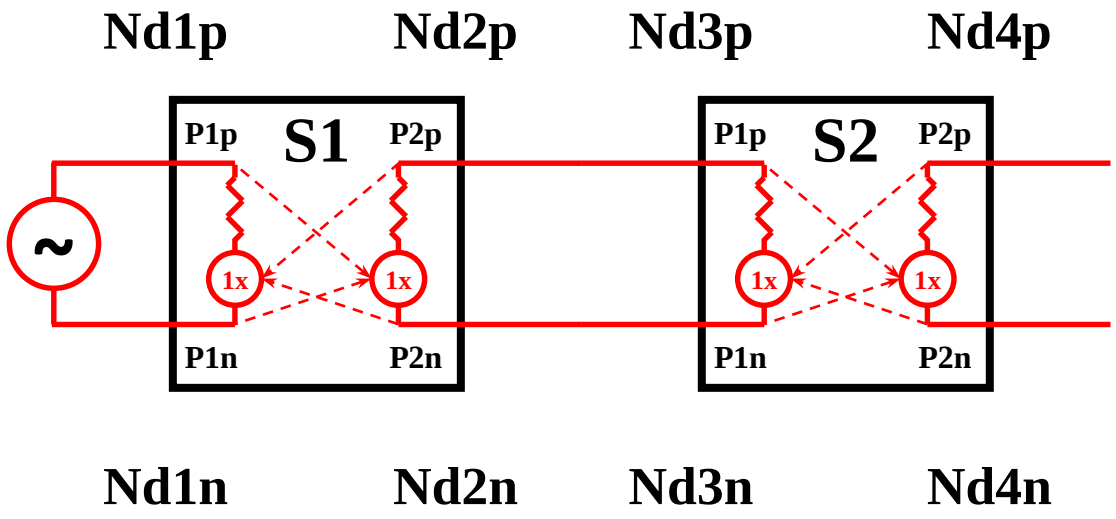
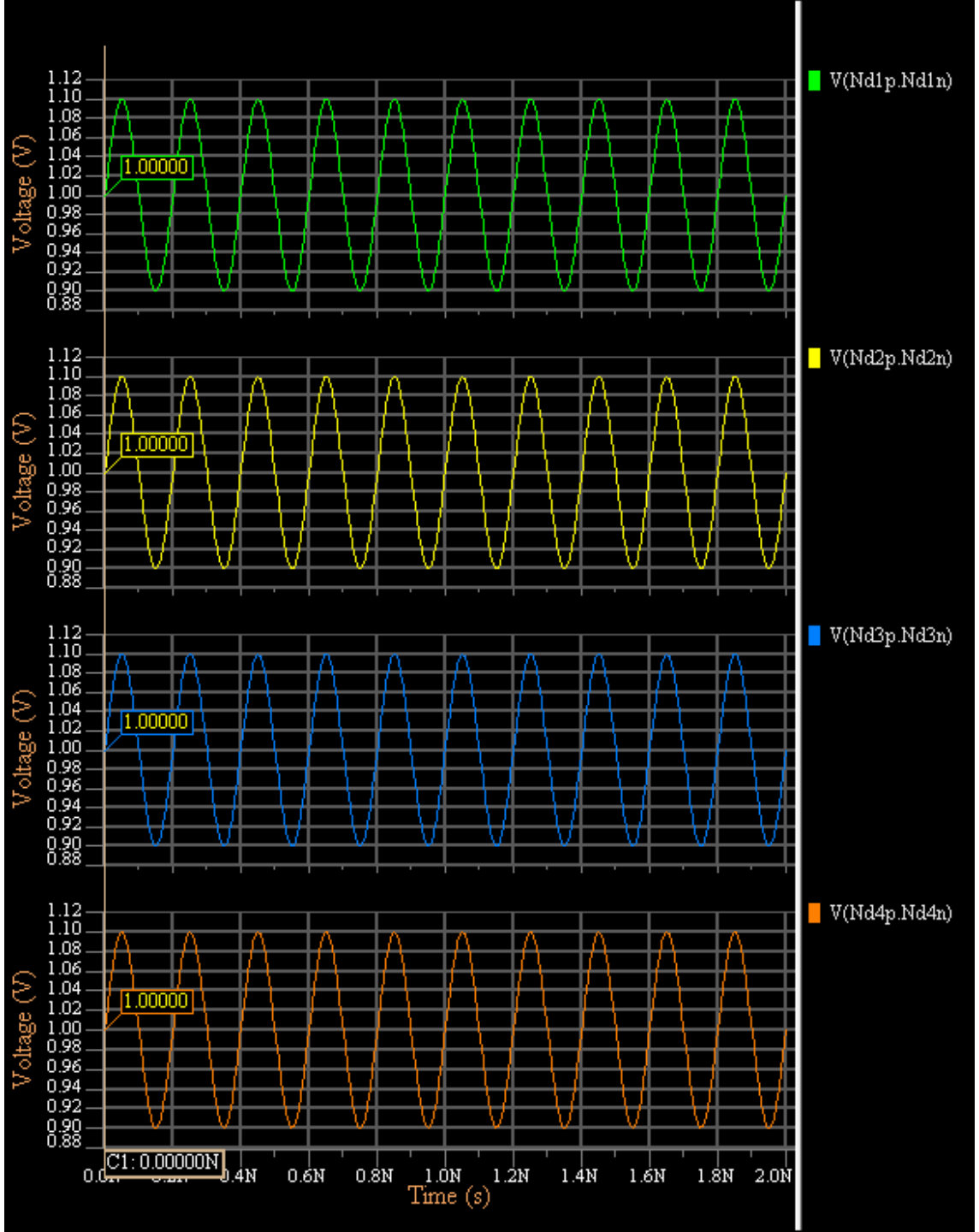
VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}

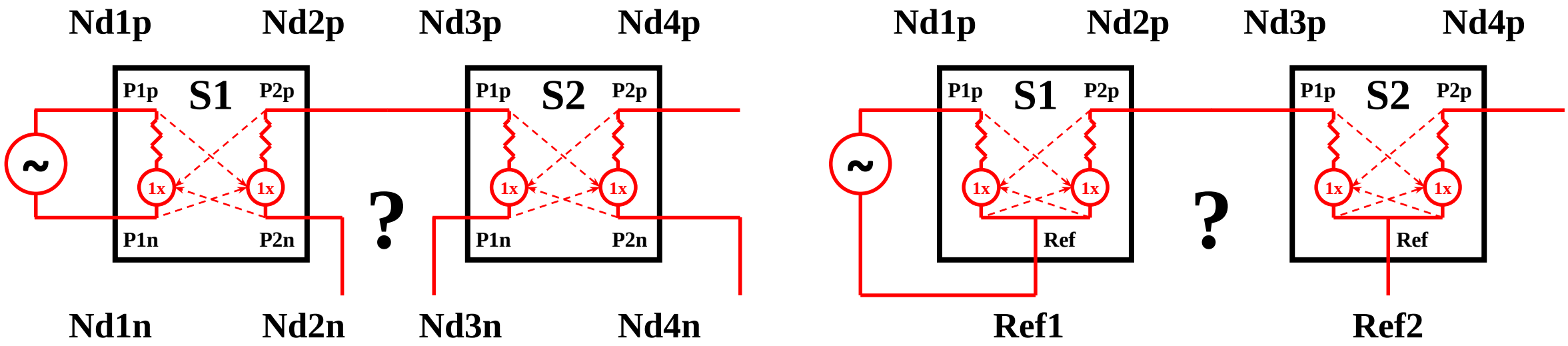




VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}

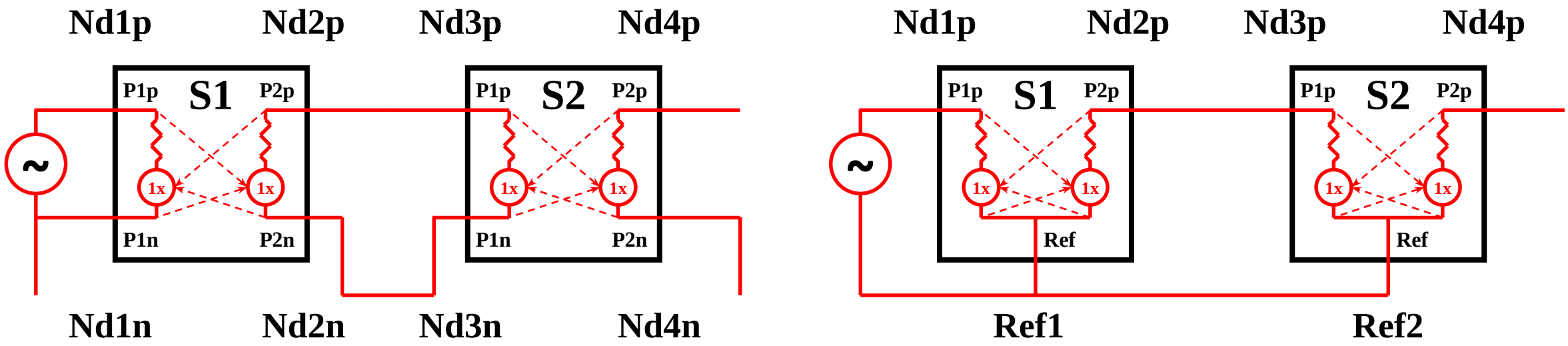


Neither of these circuits will give correct results because the port connection between S1 and S2 does not form a loop

VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}



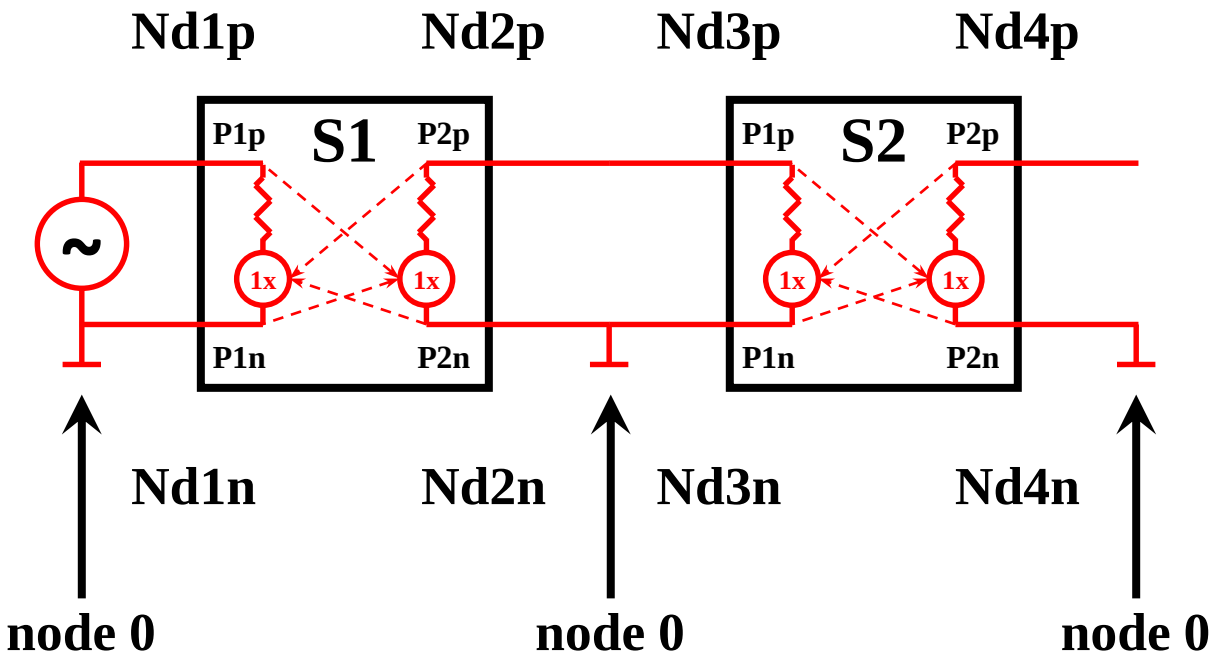
Whether the reference terminals of *<u>all</u>* ports are connected together is not the question…

Both of the above circuits will give correct results

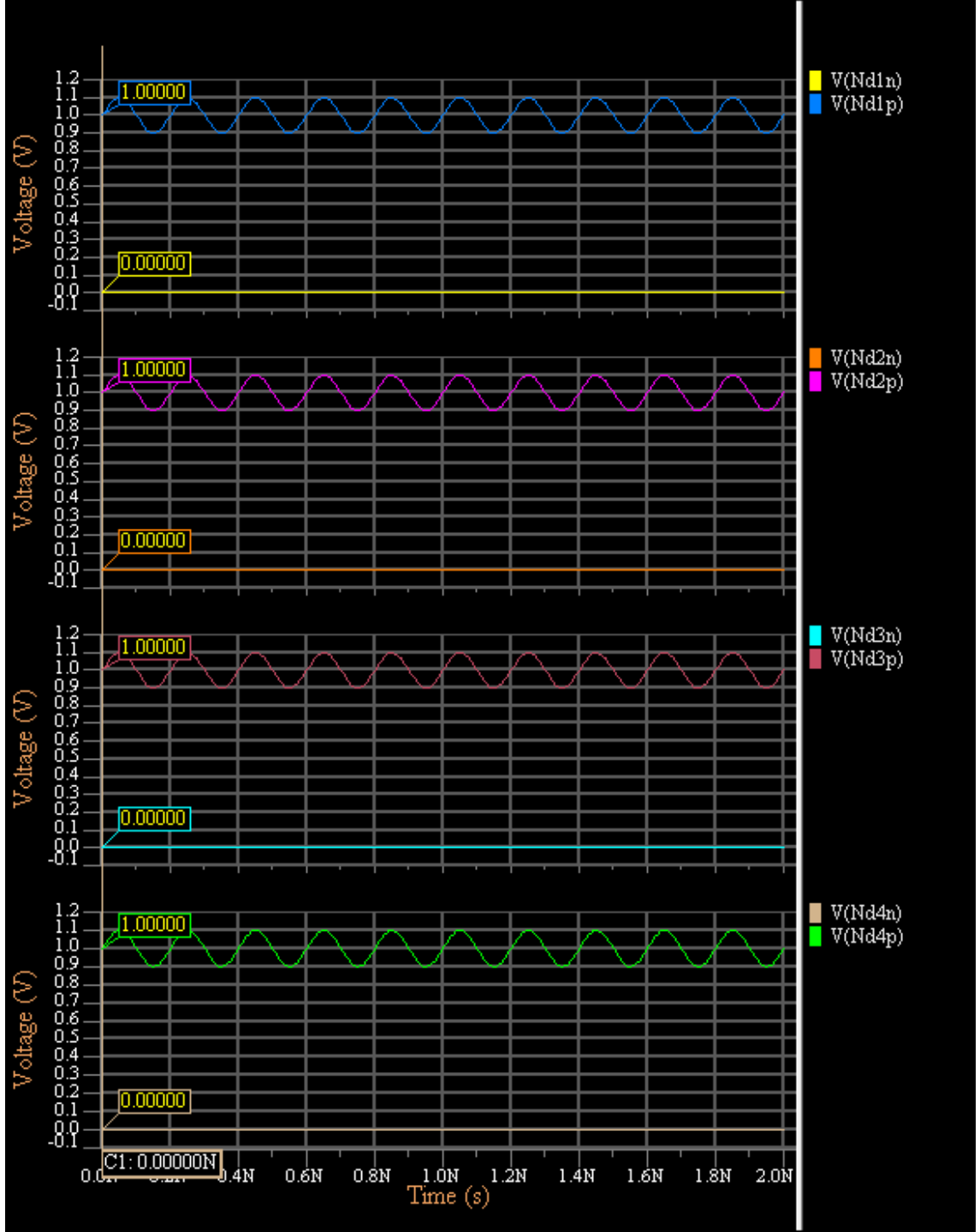
VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}



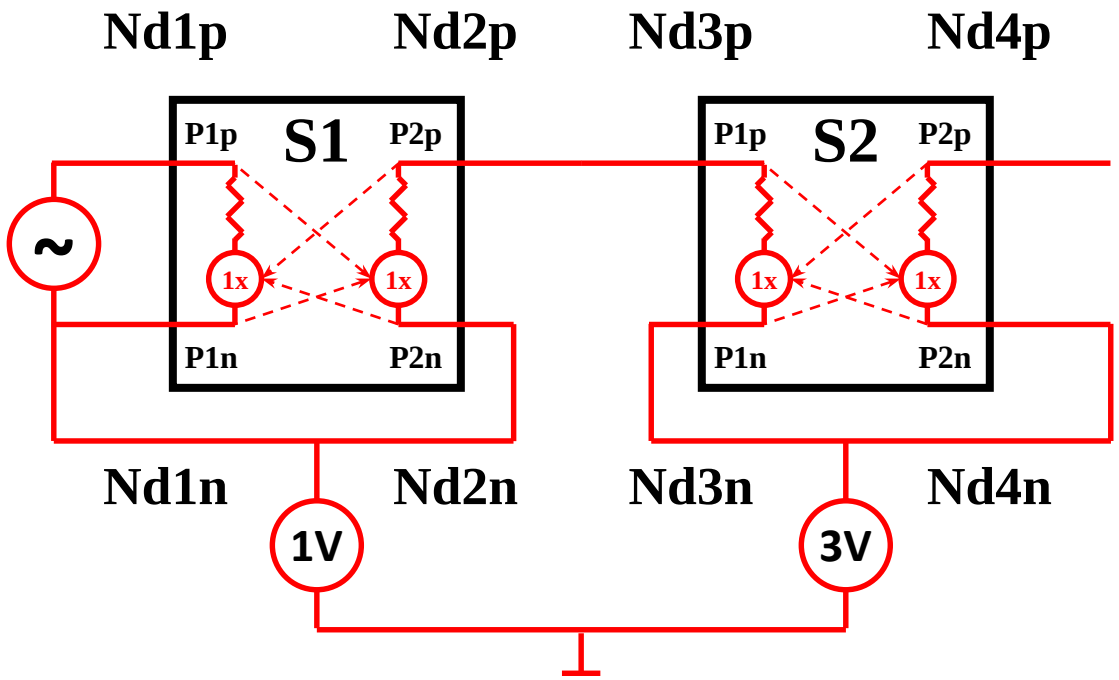
DC path to ground (node 0) must be known for SPICE-like tools



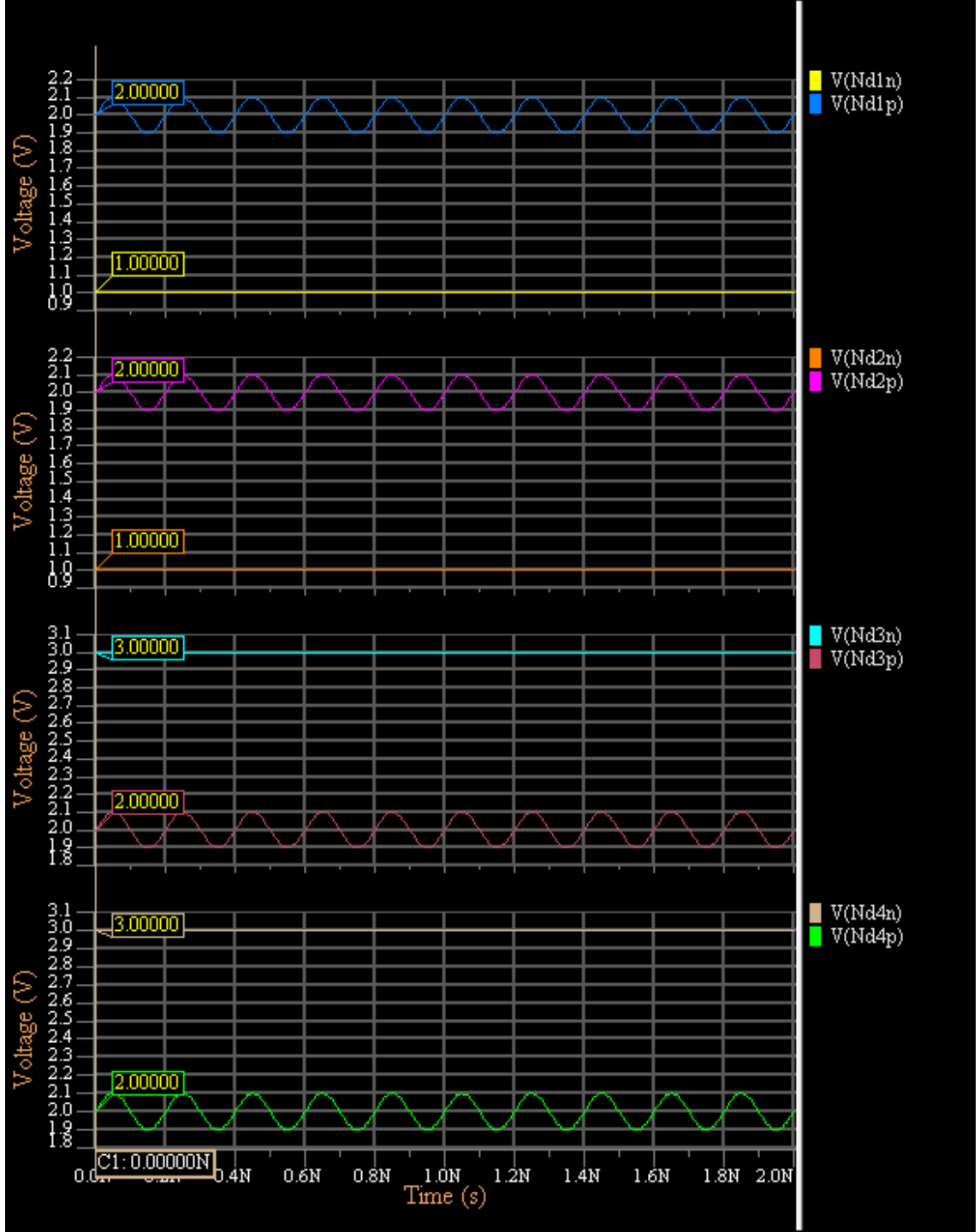
VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}



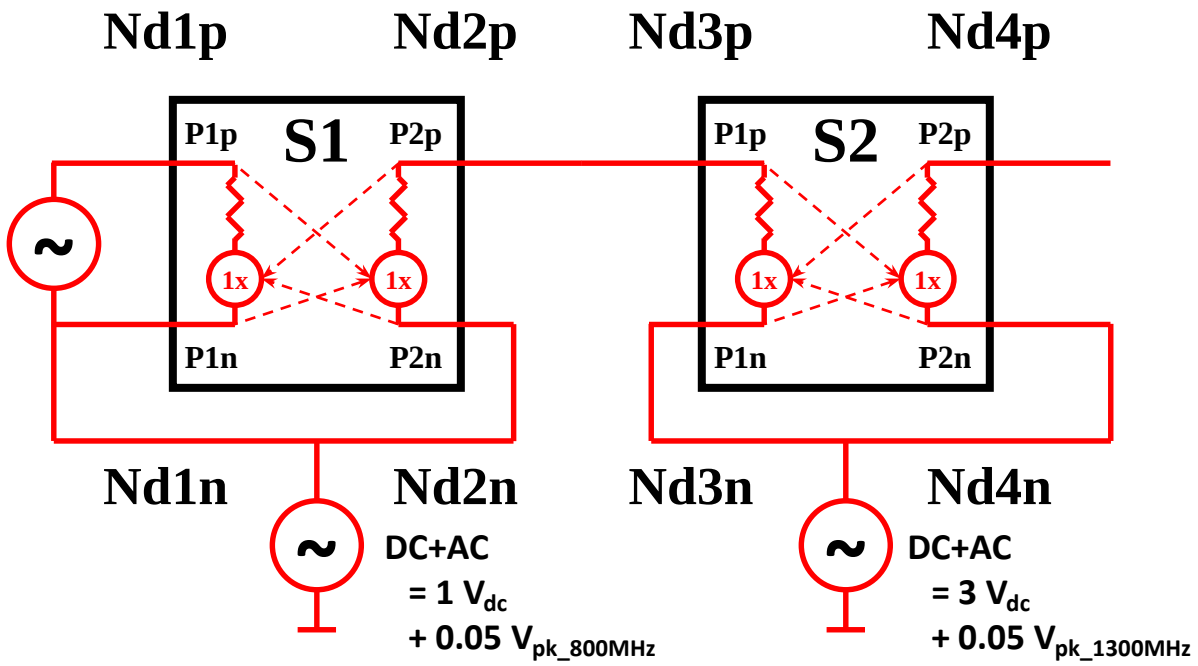
Connecting the "common reference" of S1 and S2 to different nodes will give incorrect results



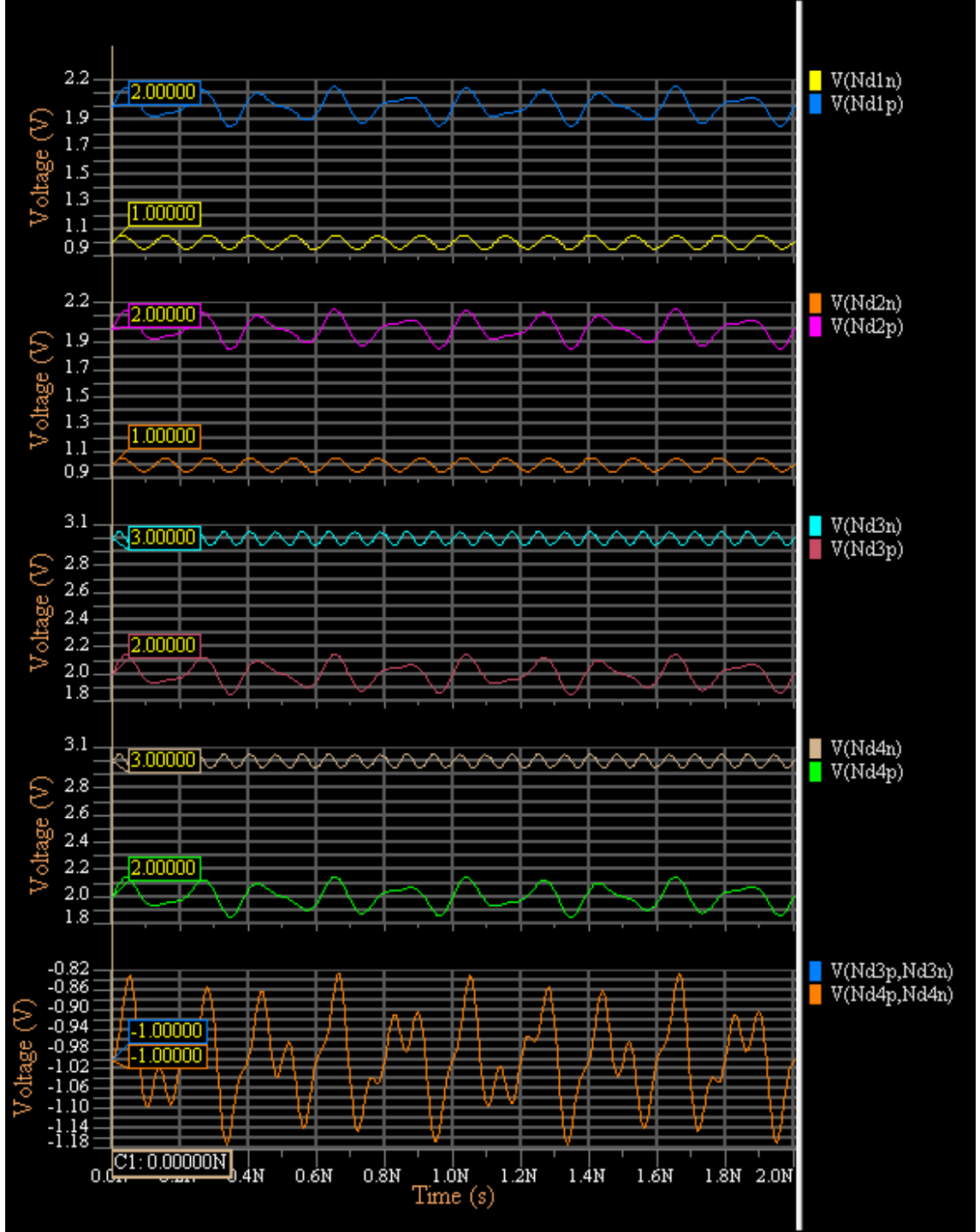
VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}



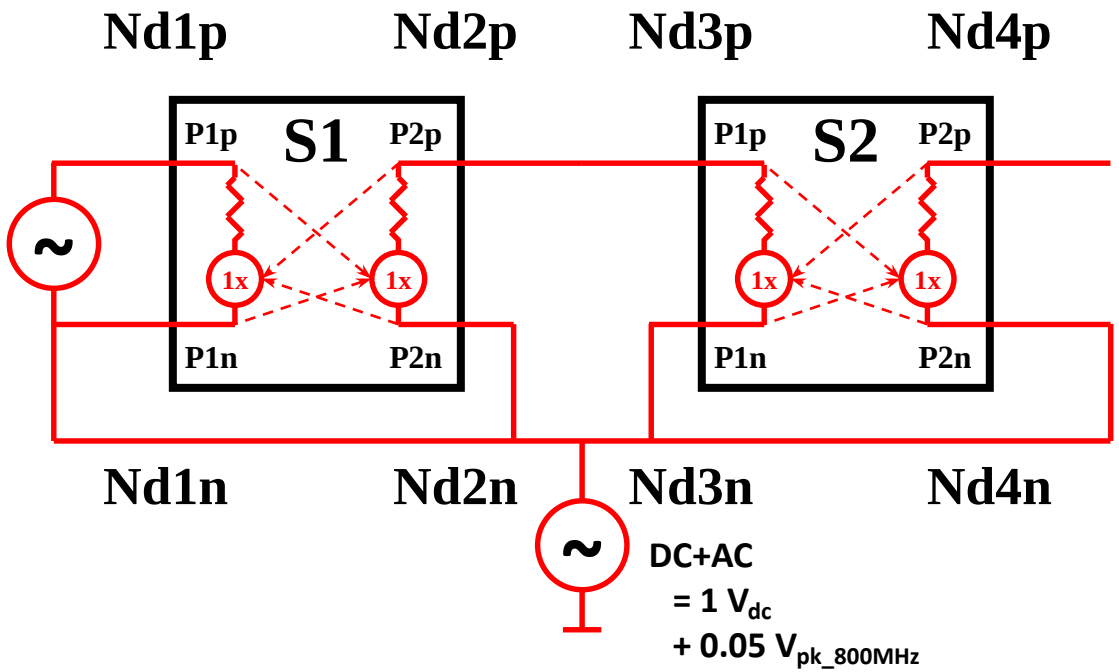
Non-ideal power modeling implies noise on the "independent" reference nodes

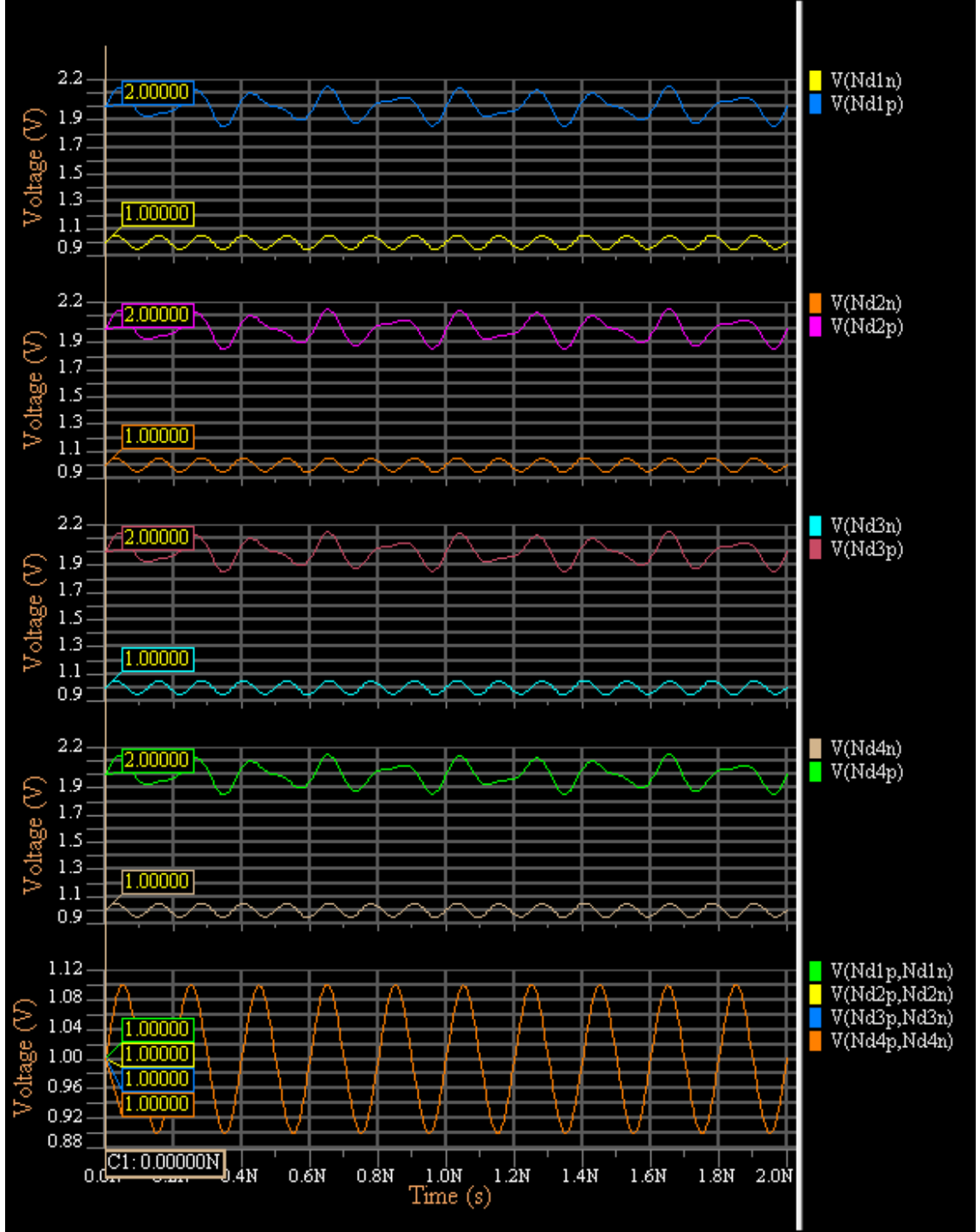


VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}



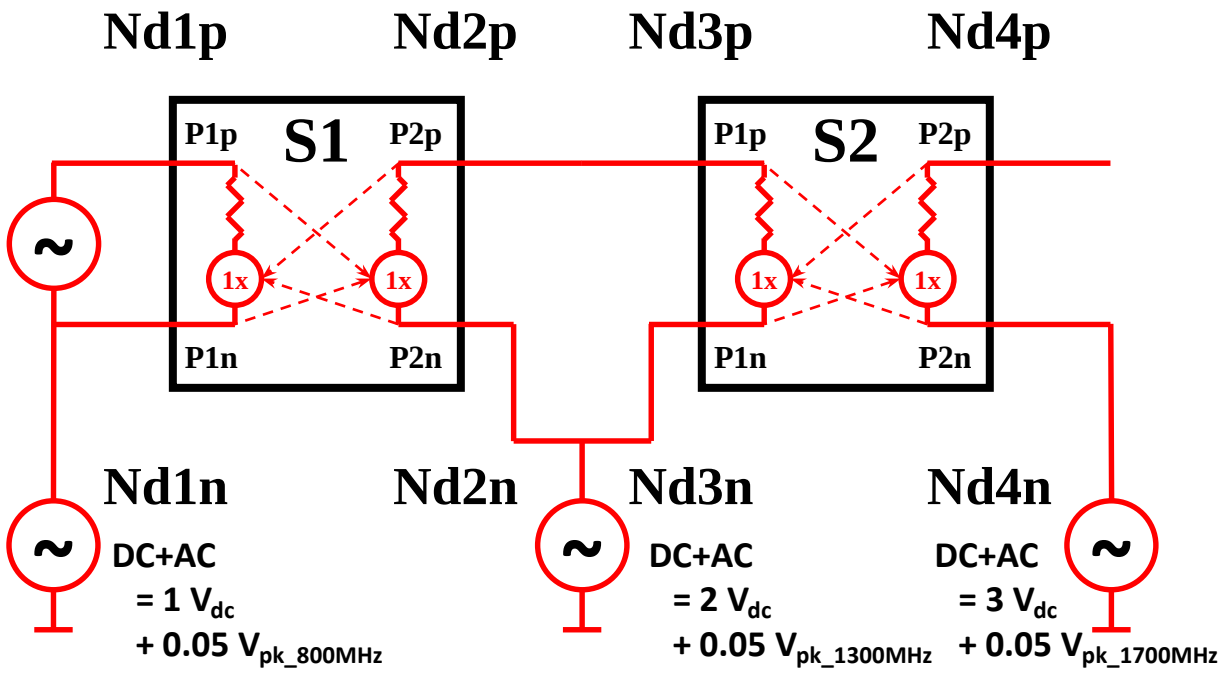


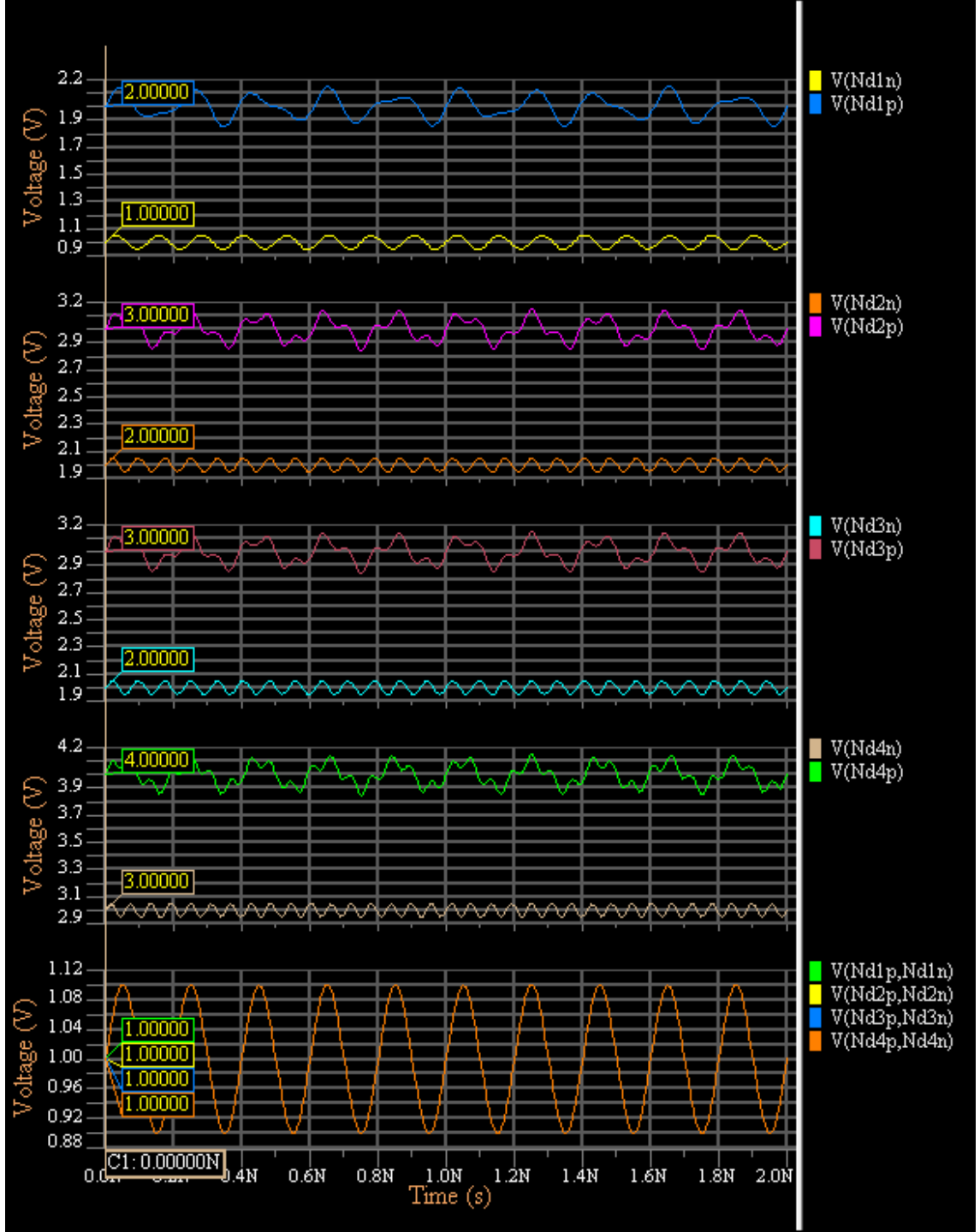
Solution 1 for IBIS: Require *<u>all</u>* reference terminals to be connected *<u>together</u>* (not to node 0)

VCVS Gain = 1

Resistor = 1 Ohm

Stimulus = 1 V_{dc} + 0.1 V_{pk_500MHz}





Solution 2 for IBIS: Require the reference terminals of *touching ports* to be connected *together* (not to node 0)