

**IBIS Open Forum Minutes**

Meeting Date: **November 17, 2017**

Meeting Location: **Tokyo, Japan**

**VOTING MEMBERS AND 2017 PARTICIPANTS**

ANSYS Curtis Clark, Toru Watanabe, Baolong Li, Benson Wei

Miyo Kawata\*, Toru Watanabe\*

Applied Simulation Technology (Fred Balistreri)

Broadcom [Bob Miller], (Cathy Liu)

Cadence Design Systems Brad Brim, Sivaram Chillarige, Debabrata Das

Ambrish Varma, Kumar Keshavan, Ken Willis

Brad Griffin, Aileen Chen, Lanbing Chen

Guoyu Cui, Wei Dai, Zhiyu Guo, Henry He

Jinsong Hu, Liang Jiang, Skipper Liang

Ping Liu, Feng Miao, Zuli Qin, Haisan Wang

Hui Wang, Yitong Wen, Clark Wu, Janie Wu

Susan Wu, Benny Yan, Haidong Zhang

Alex Zhao, Zhangmin Zhong, Kent Ho, Angel Lai

Muse Shao, Candy Yu, Morihiro Nakazato\*

Cisco Systems Lei (Jason) Liu, Cassie (Xu) Yan

CST Stefan Paret, Matthias Troescher, Burkhard Doliwa

Danilo Di Febo, Alexander Melkozerov

Ericsson Zilwan Mahmod, Guohua Wang, Amy X Zhang

GLOBALFOUNDRIES Steve Parker

Huawei Technologies Haiping Cao, Wei (Richard) Gu, Zhenxing Hu

Peng Huang, Hongxing Jiang, Longfang Lv

Luya Ma, Guangjiang Wang, Huichao Weng

Zhengrong Xu, Hang (Paul) Yan, Chen (Jeff) Yu

Xiaojun (Steve) Zhou, Zhengyi Zhu, Huajun Chen

Shengli Wang, Zen Wei

Huawei Technologies (Hisilicon) Fangxu Yang

IBM Luis Armenta, Adge Hawes, Greg Edlund

Infineon Technologies AG (Christian Sporrer)

Intel Corporation Michael Mirmak, Hsinho Wu, Eddie Frie

Gianni Signorini, Barry Grquinovic

Masashi Shimanouchi, Denis Chen, Jimmy Hsu

Cucumber Lin, Zoe Li, Thonas (Yiren) Su

IO Methodology Lance Wang

Keysight Technologies Radek Biernacki, Pegah Alavi, Fangyi Rao

Stephen Slater, Jian Yang, Heidi Barnes

Kuen Yew Lam, Mitsuharu Umekawa\*, T. Kageura\*

Maxim Integrated Joe Engert, Don Greer, Yan Liang, Hock Seow

Mentor, A Siemens Business Arpad Muranyi, Nitin Bhagwath, Praveen Anmula

(formerly Mentor Graphics) Fadi Deek, Raj Raghuram, Dmitry Smirnov

Bruce Yuan, Carlo Bleu, Chao Jiang, David Xu

Micron Technology Randy Wolff, Justin Butterfield, Jeff Shiba, Harry Shin

Micron Memory Japan Masayuki Honda\*, Tadaaki Yoshimura\*, Toshio Oki\*

NXP (John Burnett)

Qualcomm Tim Michalka, Kevin Roselle, Irwin (Zhilong) Xue

Raytheon Joseph Aday

SiSoft Mike LaBonte\*, Walter Katz, Todd Westerhoff

Steve Silva

Synopsys Kevin Li, Ted Mido, John Ellis, Scott Wedge

Wonsae Sim, Xuefeng Chen, Jinghua Huang

Yijiang Huang, Deng Shi, Yuyang Wang

Teraspeed Labs Bob Ross

Xilinx Masao Nakane\*

ZTE Corporation Rongxing Ban, Xinjian Chen, Fengling Gao

Tao Guo, Lili Wei, Yangye Yu, Shunlin Zhu

Zuken Ralf Bruening, Michael Schaeder, Alfonso Gambuzza

Kiyohisa Hasegawa\*, Takayuki Shiratori\*

**OTHER PARTICIPANTS IN 2017**

A&D Print Engineering Co. Y. Yoshida\*

Abeism Corporation Nobuyuki Kiyota\*

Accton Raul Lozano

ADLINK Technology Alvis Hsu

AMD Japan Tadashi Arai\*

Amphenol Fred Shen, Holly Wang

Apollo Giken Co. Satoshi Endo\*

ASR Microelectronics Lili Dia, Shulong Wu

ASRock Rack Eric Chien

ASUS Nick Huang, Bin-chyi Tseng, Andrew Huang

Aurora System Murong Lu, Jiaxin Sun

Avant Technology Jyam Huang, Chloe Yang

Avnet K. Ogasawara\*, M. Hinosugi\*

BasiCAE Kiki Li, Darcy Liu, July Tao, Lisa Wu

Brite Semiconductor Haonan Wang

Calsonic Kansei Corp. K. Hosoya\*

Canon Syoji Matsumoto\*, H. Isono\*

Casio Computer Co. Ikuo Imada\*

Celestica Wilson Chen, Sophia Feng, Lurker Li

Weiqing Liiu, Vincent Wen

Continental AG Stefanie Schatt

Cybernet Systems Hideto Ishikura\*, Shiho Nagae\*, Takayuki Tsuzura\*

Design Methodology Lab M. Tanaka\*

eASIC David Banas

Edadoc Deheng Chen, Bruce (Jun) Wu, Hong Zhang

Eizo Corp. K. Yamada\*

Extreme Networks Bob Haller

Flextronics Renjun Sun

Foxconn Electronics Gino (Chunjen) Chen, Joe (Chienhusn) Chen

Alex Tang

Fujitsu Advanced Technologies K. Teramae\*, M. Nagata\*, H. Kawata\*, T. Kobayashi\*

Fujitsu Interconnect Technologies Masaki Kirinaka\*, Akiko Tsukada\*

Fujitsu Kyushu System Services K. Nabae\*

Fujitsu Ltd. Kohichi Yoshimi\*

Ghent University Paolo Manfredi

H3C Xinming Hu

Hamamatsu Photonics Akahiro Inoguchi\*, S. Fujita\*

Hamburg University of Technology Torsten Revschel, Torsen Wendt

Hewlett Packard Enterprise Passor Ho, Corey Huang, Hellen Lo

Hitachi ULSI Systems Co. Sadahiro Nonoyama\*

IdemWorks Michelangelo Bandinu

Ilia State University Nana Dikhaminjia

Independent Dian Yang, Lawrence Der

Innotech Corp. S. Seki\*

Inspur Technologies Josh Chen, Dane Huang, Nieves Lee, Ian Yu

Institute for Information Industry Joseph Lang

Inventec Ian Chen, Ellen Tseng

Japan Radio Co. Takashi Sato\*

JEITA R. Miyagawa\*, Hirohisa Nakamura\*

John Baprawski, Inc. John Baprawski

Jujube T. Hosaka\*

JVC Kenwood Corp. Y. Ojima\*, A. Kadowaki\*, M. Furuya\*

KEI Systems Shinichi Maeda\*

Keihin Corp. S. Ito\*

Kyoden Co. T. Takauji\*

Lattice Semiconductor Maryam Shahbazi, Dinh Tran

Leading Edge Pietro Vergine

Lenovo Group Shaogao Zheng, Paul Chu, John Lin, Alan Sun

Lexington Consulting Mike Barg

Lite-On Technology Sam (Dongru) Lyu

MD Systems Co. Hideaki Kouzu\*

Megachips Corp. T. Kitamura\*

Missouri Science and Technology Giorgi Maghlakelidze

EMC Lab

Mitsubishi Electric Corp. Yusuke Suzuki\*

Modech T. Ochiai\*

Mostec Nelly Li, Clark Zhang

Murata Manufacturing Co. K. Mukuaiyama\*, Y. Murukami\*

Nanya Technology Corp. Chingfeng Chen, Chiwei Chen, Andy (Weishen) Chih

Minlun Lan, George Lee, Allen Ye

NEC Platforms Y. Onodera\*

Neophotonics Semiconductor GK S. Moribayashi\*

Novatek Jerrcik Cheng, Vincent Lin

Oki Electric Industry Co. Atsushi Kitai\*

Panasonic Corp. N. Manabe\*

Panasonic Industrial Devices, Kazuki Wakabayashi\*

Systems and Technology Co.

Pegatron Corp. Melissa Huang, James Lee

Pioneer Corp. K. Tochitani\*

Politecnico di Torino Claudio Siviero, Stefano Grivet-Talocia, Igor Stievano

PWB Corp. T. Ohisa\*

Quanta Computer Eriksson Chuang, Aaron Lee, Scott Lee, Jerry Syue

Renesas Electronics Corp. M. Suzuki\*, N. Yokoshima\*, Kazunori Yamada\*

M. Hanagiri\*, T. Hayashi\*

Ricoh Company Yasuhiro Akita\*, M. Goto\*, Kazuki Murata\*

Ricoh Industry Co. Kohji Kurose\*, Toshihiko Makino\*

Rise Corp. S. Yanagita\*

Rockchip Junming Shi

Rohm Co. Noboru Takizawa\*

SAE-ITC (Thomas Munns), Jose Godoy

SAIC Motor Corp. Weng Yang

Samsung Jung Hwan Choi

Shanghai Fudan Microelectronics Zhenghui Chen, Liu Lu Fang, Xin Li, Yuezhi Liu

Group Xiao Lei Luo, Canghai Tang

Shinewave Nike Yang

Signal Metrics Ron Olisar

SII Semiconductor Corp. M. Murata\*

SMICS Sheral (Xuejiao) Qi

Socionext Shigeru Nishio\*, Watari Tanaka\*, Yumiko Sugaya\*

Shizue Kato\*, Yu Kamata\*, H. Ohmi\*, F. Kawafuji\*

Y. Sumimoto\*, M. Tomita\*, Megumi Usui\*

Sohwa & Sophia Technologies Tomoki Yamada\*

Sony Global Manufacturing & Taichi Hirano\*, A. Muto\*, T. Yuasa\*, T. Mizoroki\*

Operations Corp.

Sony LSI Design Satoshi Tago\*, Toru Fujii\*

Sony Semiconductor Solutions K. Amano\*

SPISim (Peace Giant Corp.) Wei-hsing Huang, Walter Huang

Spreadtrum Communications Junyong Deng, Ganyue Wang, Shiqing Si

Stanford University Tom Lee

STMicroelectronics Fabio Brina, Olivier Bayet

Tatung Technology Barry Chen, Daniel Chen

Teledyne Lecroy Facun Li, Yifeng Wu

TFF Corp. Katshuhiko Suzuki\*

Thine Electronics S. Ikeda\*, T. Sada\*

TopBrain Ye Li

Toshiba Yasuki Torigoshi\*, Yoshinori Fukuba\*

Toshiba Development & N. Kasai\*

Engineering Corp.

Toshiba Electronic Devices & A. Tomishima\*, Yasunobu Umemoto\*, T. Tsujimura\*

Storage Corp.

Toshiba Memory Corp. Masato Kanie\*

Toshiba Memory Systems Co. E. Kozuka\*, J. Shibasaki\*

Toshiba Microelectronics Corp. Jyunya Masumi\*

TSG Co. S. Mitsuyama\*

U-Creative Amber Wu

Université Blaise Pascal Mohamed Toure

Université de Bretagne Occidentale Mihai Telescu

VIA Labs Shengyuan Lee

VIA Technologies Terence Hsieh, Justin Hsu

Winbond Yumin Hou, Albert Lee

Xpeedic Tuhui Gui

Yamaha Corp. H. Kai\*

Yi Chuan Technology Wei Ming Lu

Zhaoxin Liam Li, Eddrick Wang

Zhejiang Uniview Technologies Busen Cai, Jilun Fang

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

December 1, 2017 624 999 876 IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/zeulerr>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

-------------------------------------------------------------------------------------------------------------------------------

**OFFICIAL OPENING**

The Asian IBIS Summit took place on Friday, November 17, 2017 at the Akihabara UDX building in Tokyo. About 108 people representing 65 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/nov17c/>

Mike LaBonte began with a welcome address from the IBIS Open Forum, in which he thanked JEITA for hosting the IBIS summit and for their work supporting IBIS in general. Mike said IBIS remains the most popular format for describing digital buffers, and most digital electronic devices today are designed using IBIS.

Mike also thanked the sponsors ANSYS, Cadence Design Systems, Cybernet Systems, Keysight Technologies, Ricoh, Toshiba Corporation, and Zuken. He said minutes of the summit would be posted and officially opened the meeting.

Mitsuharu Umekawa gave a welcome address from JEITA, noting that the morning workshop was arranged by the JEITA EDA Model Specialty Committee, and the topic was power aware IBIS simulation.

**IBIS UPDATE**

Mike LaBonte (SiSoft, USA)

Mike LaBonte detailed the activities of the IBIS Open Forum over the past year. He showed a possible timeline for the passage of IBIS 7.0, as well as the status of all current BIRDs that may or may not be part of IBIS 7.0. Mike gave a brief summary of the changes in three BIRDs likely to become part of IBIS 7.0.

Further explanation of BIRD 147 was requested. Mike gave some of the history of BIRD 147, saying that it originally was a more comprehensive proposal, including the BCI file to describe the protocol for communication between buffers. The accepted BIRD does not specify the protocol, leaving model makers to define the contents of the files themselves. It was noted that this posed a challenge for model portability across vendors. Mike said that there was general agreement that protocol descriptions could be submitted and posted on the IBIS website informally, and that this approach should provide for faster adoption of protocols than might be possible if the protocols would have to be described in the IBIS specification itself. A question was asked about what applications need a back channel interface. Mike noted that PCIe was an example.

Shinichi Maeda noted that DDR4 uses training to decide the Vref level. He asked if BCI is available for traditional IBIS too. Mike noted that BCI is an IBIS-AMI protocol and the RX algorithmic model controls the process. A question was asked about IBIS support for DDR4 single-ended equalization. Mike said that although IBIS does not explicitly support single-ended IBIS-AMI, it does not strictly limit IBIS-AMI to differential signaling, and some tools have been using IBIS-AMI to support DDR4.

**WHAT’S EXPECTED FOR IBIS-AMI FROM THE PERSPECTIVE OF END-USER SUPPORT**

Masao Nakane (Xilinx, Japan)

Masao Nakane listed user expectations for IBIS-AMI models. One of these is result matching between different simulators and between simulators and measurement, but there are often problems in that area. Often, the cause of the trouble is not necessarily in the algorithmic models, but in the S-parameters that form the channel. Lack of causality was a common issue. One way to determine if that is the cause of mismatch between simulators is to capture and compare the impulse responses sent by the simulators to the first IBIS-AMI model, which often differ. He said a unified methodology is needed for channel characterization. Mike LaBonte commented that sometimes the algorithmic models were found to be improperly sensitive to samples per bit and block size settings, and that the different defaults for those between tools would sometimes cause differences.

**DDR SYSTEM SIMULATION: WHAT ISSUE TO SIMULATE**

Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda gave an overview of DDR technologies from DDR through DDR4. He described difficulties encountered in producing good package models for DDR4, as well as factors that could make DDR5 difficult to simulate. One of the DDR4 issues was the large number of variable parameters, leading to a large number of simulations that would need to be performed.

**INVESTIGATION OF THE PACKAGE CROSSTALK NOISE TO DDR4-IF SIGNAL BY IBIS [DEFINE PACKAGE MODEL]**

Akiko Tsukada, Masaki Kirinaka (Fujitsu Interconnect Technologies Limited, Japan)

[Presented by Akiko Tsukada (Fujitsu Interconnect Technologies Limited, Japan)]

Akiko Tsukada showed the results of extensive crosstalk simulation across a variety of cases. She said the ability to design out crosstalk on boards has improved, leaving package crosstalk as a more significant factor. The [Define Package Model] matrix formats were explained, as well as equivalent IBIS-ISS circuits that can be used. In crosstalk testing the victim net is held static while a stimulus pattern is applied to the aggressors, allowing crosstalk to be measured in the voltage domain. The timing skew effect of crosstalk on active signals can also be measured. It was found that even mode aggressors had more crosstalk-induced skew effect than odd mode aggressors, and that board coupling produced less skew than package coupling.

A question was asked about how the aggressor signal location is selected for a victim line. Tadashi Arai commented that crosstalk skew is dynamically changed by signals. So it’s relatively averaged. Generally, IC vendors factor in skew induced by IC packages and budgets as part of jitter in advance.

**ON DIE DE-CAP MODELING PROPOSAL**

Kazuki Murata (Ricoh Company, Japan)

Kazuki Murata noted that the LSI Package Board (LPB) format is an IEEE standard format produced by the JEITA Semiconductor Design Technology Subcommittee. The subcommittee had surveyed people involved in LSI design, and found that while on-die decoupling is considered very important, availability of models including that decoupling was poor. Measurements of decoupling do not all use the same circuit topology, and that should be standardized. IBIS offers no specific support for modeling decoupling. He showed how [Series Model] could be used to define capacitance between power and ground pins. He felt that that was not a good choice for describing a power delivery network model, however, due to topology differences. Alternatively, [External Model] and [External Circuit] could be used, but these were considered too complex. The LPB modeling working group is proposing a new IBIS syntax to describe on-die decoupling capacitors. A forum on the topic will be held March 9, 2018.

Mike LaBonte asked if the IBIS checker passes the series De-cap configuration. Kazuki responded yes. A comment was made that from the IC design house side, they don’t feel comfortable revealing the on-die de-cap in IBIS format because it may reveal internal system design.

**IBIS INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE**

Michael Mirmak (Intel Corporation, USA)

[Presented by Mike LaBonte (SiSoft, USA)]

Mike LaBonte presented on behalf of Michael Mirmak. The concepts found in BIRD189.x were summarized. The new format is an improvement over existing IBIS [Define Package Model] in several ways, allowing for both cascaded model sections as well as coupling in any combination. The Touchstone format and the ability to separately model buffer to pad and pad to pin connections would be helpful for the high speed signals used today. The addition of die pads for rails allowed for circuit topologies suitable for modeling the power and ground rails in chips.

A question was asked about the modeling extensions not covered by the presentation. Mike said that bus labels had not been covered in any detail. He added that while BIRD189 was not designed for modules or stacked die, extensions to support that and multi-chip modules were planned.

Mitsuharu Umekawa commented that it’s good to have freedom for inter-connect representation. Besides, factoring in end-user scenarios of simulations may be important to have this new standard become popular.

**CLOSING REMARKS**

Mike LaBonte closed the meeting, thanking JEITA, the sponsors, the speakers, and all who attended. Mitsuharu Umekawa thanked the audience, encouraging support for the LPB effort.

**NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held December 1, 2017. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 15, 2017.

The Asian IBIS Summit in Tokyo will be held November 17, 2017. No teleconference will be available for the Summit meeting.

========================================================================

**NOTES**

IBIS CHAIR: Mike LaBonte

[mlabonte@](mailto:mlabonte@)sisoft.com

IBIS-AMI Modeling Specialist, SiSoft

6 Clock Tower Place, Suite 250

Maynard, MA 01754

VICE CHAIR: Lance Wang (978) 633-3388

[lwang@iometh.com](mailto:lwang@iometh.com)

President/CEO, IO Methodology, Inc.

PO Box 2099

Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764

[rrwolff@micron.com](mailto:rrwolff@micron.com)

Principal Engineer, Silicon SI Group Lead, Micron Technology, Inc.

8000 S. Federal Way

P.O. Box 6, Mail Stop: 01-711

Boise, ID 83707-0006

TREASURER: Bob Ross (503) 246-8048

[bob@teraspeedlabs.com](mailto:bob@teraspeedlabs.com)

Engineer, Teraspeed Labs

10238 SW Lancaster Road

Portland, OR 97219

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40

[ibis-librarian@ibis.org](mailto:ibis-librarian@ibis.org)

Digital Modules Design, PDU Base Stations, Ericsson AB

BU Network

Färögatan 6

164 80 Stockholm, Sweden

WEBMASTER: Mike LaBonte

[mlabonte@](mailto:mikelabonte@eda.org)sisoft.com

IBIS-AMI Modeling Specialist, SiSoft

6 Clock Tower Place, Suite 250

Maynard, MA 01754

POSTMASTER: Curtis Clark

[curtis.clark@ansys.com](mailto:curtis.clark@ansys.com)

ANSYS, Inc.

150 Baker Ave Ext

Concord, MA 01742

This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to [info@ibis.org](mailto:info@ibis.org). Examples of inquiries are:

* To obtain general information about IBIS.
* To ask specific questions for individual response.
* To subscribe to the official [ibis@freelists.org](mailto:ibis@freelists.org) and/or [ibis-users@freelists.org](mailto:ibis-users@freelists.org) email lists (formerly [ibis@eda.org](mailto:ibis@eda.org) and [ibis-users@eda.org](mailto:ibis-users@eda.org)).
* To subscribe to one of the task group email lists: [ibis-macro@freelists.org](mailto:ibis-macro@freelists.org), [ibis-interconn@freelists.org](mailto:ibis-interconn@freelists.org), or [ibis-quality@freelists.org](mailto:ibis-quality@freelists.org).
* To inquire about joining the IBIS Open Forum as a voting Member.
* To purchase a license for the IBIS parser source code.
* To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>   
[http://www.ibis.org/ bugs/ibischk/bugform.txt](http://www.ibis.org/%20bugs/ibischk/bugform.txt)

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>   
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>   
<http://www.ibis.org/bugs/icmchk/icm_bugform.txt>

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>   
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>   
<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

Other trademarks, brands and names are the property of their respective owners.

**SAE STANDARDS BALLOT VOTING STATUS**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Organization** | **Interest Category** | **Standards Ballot Voting Status** | **October 27, 2017** | **November 13, 2017** | **November 15, 2017** | **November 17, 2017** |
| ANSYS | User | Active | X | - | X | X |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Broadcom Ltd. | Producer | Inactive | - | - | - | - |
| Cadence Design Systems | User | Active | - | X | X | X |
| Cisco Systems | User | Inactive | - | X | - | - |
| CST | User | Inactive | - | - | - | - |
| Ericsson | Producer | Inactive | - | X | - | - |
| GLOBALFOUNDRIES | Producer | Inactive | X | - | - | - |
| Huawei Technologies | Producer | Inactive | - | X | - | - |
| IBM | Producer | Inactive | - | - | - | - |
| Infineon Technologies AG | Producer | Inactive | X | - | - | - |
| Intel Corp. | Producer | Active | X | - | X | - |
| IO Methodology | User | Active | X | X | X | - |
| Keysight Technologies | User | Active | X | - | X | X |
| Maxim Integrated | Producer | Inactive | - | - | - | - |
| Mentor, A Siemens Business | User | Inactive | X | X | - | - |
| Micron Technology | Producer | Inactive | X | - | - | X |
| NXP | Producer | Inactive | - | - | - | - |
| Qualcomm | Producer | Inactive | - | - | X | - |
| Raytheon | User | Inactive | - | - | - | - |
| SiSoft | User | Active | X | X | X | X |
| Synopsys | User | Inactive | X | X | - | - |
| Teraspeed Labs | General Interest | Inactive | X | - | - | - |
| Xilinx | Producer | Inactive | - | - | - | X |
| ZTE Corp. | User | Inactive | - | X | - | - |
| Zuken | User | Inactive | - | - | - | X |

Criteria for SAE member in good standing:

* Must attend two consecutive meetings to establish voting membership
* Membership dues current
* Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

* Users - members that utilize electronic equipment to provide services to an end user.
* Producers - members that supply electronic equipment.
* General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.