EIA IBIS Open Forum Summit Minutes

Meeting Date: **April 19, 2007**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2007 PARTICIPANTS

Actel	(Prabhu Mohan)
Agere	(Nirav Patel)
Agilent	Radek Biernacki, Saliou Dieye*, Riccardo Giacometti*
AMD	Nam Nguyen, Tadashi Arai
Ansoft Corporation	(Michael Brenneman)
Apache Design Solutions	(Ji Zheng)
Applied Simulation Technology	(Fred Balistreri)
Apple Computer	(Bill Cornelius)
Cadence Design Systems	Lance Wang, C. Kumar, Hemant Shah, Patrick dos Santos*
Cisco Systems	Syed Huq, Tram Bui, AbdulRahman Rafiq, Huyen Pham, Darja Padilla, Mike LaBonte, Paul Ruddy, Gurpreet Hundal, Luis Boluna, Ehsan Kabir, Jehyoung Lee, Susmita Mutsuddy, Eddie Wu
Ericsson	Anders Ekholm*, Ole Segtum
Fluent	(Chetan Desai)
Freescale	Jon Burnett
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji*
Huawei Technologies	ChunXing Huang, Bob He
Integrated Circuit Systems (ICS)	(Dan Clementi)
Intel Corporation	Michael Mirmak, Arpad Muranyi
LSI Logic	Frank Gasparik, Kim Helliwell, Dinh Tran, Praveen Soora
Mentor Graphics	John Angulo, Ian Dodd, Eric Rongere*, Stephane Rousseau*
Micron Technology	Randy Wolff, Pavani Jella
NEC Electronics Corporation	Hock Seow, Huy Tran
Nokia Siemens Networks GmbH[1]	Eckhard Lenski*, Flavio Maggioni*, Roberto Preatoni*, Umberto Gatti*, Massimo Ceppi*
Panasonic	(Atsuji Ito)
Samtec	(Corey Kimble)
Siemens AG [1]	[Eckhard Lenski], Manfred Maurer*
Signal Integrity Software	Barry Katz, Douglas Burns, Mike Steinberger, Walter Katz, Todd Westerhoff

Sigrity	Sam Chitwood, Sandy Dung
Silego	(Joe Froniewski)
STMicroelectronics	Antonio Girardi*, Giacomo Bernardi, Roberto Izzi
Synopsys	Ted Mido
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Texas Instruments	Otis Gorley, Richard Ward, Bonnie Baker
Toshiba	(Yasumasa Kondo)
Xilinx	Bruce Bandeli, David Banas
ZTE	(Shunlin Zhu)
Zuken	Michael Schaeder*, Ralf Bruening*

[1] Nokia Siemens Networks is a new company formed by the merger with a former group at Siemens active with the IBIS Committee. Both companies are temporarily carried as voting members until the official membership and voting status is resolved.

OTHER PARTICIPANTS IN 2007

74ze Engineering	Linc Jepson
Altera	Hui Liu, Zhe Lin, Ravindra Gali, Salman Jiva
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Cavium Networks	Johann Nittmann
ChipX	Jay Hidy, Oren Dvir
Cybernet Systems	Kazuhiki Kusunoki
EFM	Ekkehard Miersch*
Enterasys	Robert Haller
Extreme Networks	Kevin Ko
Force10 Networks	Robert Badal
GEIA	(Chris Denham)
Hewlett Packard	Shafiq Rahman
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Infineon	Christian Sporrer*
Leventhal Design	Roy Leventhal
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NXP	H N Sudarshan
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Politecnico di Torino	Igor Stievano*, Michelangelo Bandinu*
Renesas Technology	Takuji Komeda
Samsung	Sang-Soo Park
Sedona International	Joe Socha
Sun Microelectronics	Leon Yang

Tiburon Design Automation	Patirick Challacn
White Electronics Designs	John Perez
Xyratex	Paul Levin, Joseph Chan

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
April 20, 2007	1-916-356-2663	3	231-4253

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

WELCOME AND INTRODUCTIONS

The European IBIS Summit Meeting was held in Nice, France at the Novotel Nice Centre during the Design Automation and Test Exhibition (DATE) conference. About 22 people attended representing 14 companies.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/pub/ibis/summits/apr07/

Thanks to Eckhard Lenski for supplying the notes used for this set of minutes.

Ralf Bruening hosted the meeting and opened the meeting noting that this is the tenth IBIS summit in Europe. He noted that IBIS is the fuel for SI-analysis and also a standard. But, a standard has to live, and the best way of doing so is through the exchange of ideas and information at the summit. He thanked the four co-sponsors: Agilent Technologies, Cadence Design Systems, Mentor Graphics and Zuken and also the people who keep the spirit of IBIS alive. Attendees introduced themselves.

The presentations were then given.

FROM IBIS TO ELECTROMAGNETIC COMPATIBILITY PREDICTION OF INTERGRATED

CIRCUITS

Etienne Sicard, National Institute of Applied Science (INSA), France

Etienne started with an overview of technology scaling down and its impact on complexity (number of transistors per chip) and packaging (from a small 16bit microchip up to a package on package (POP) with multiple die). Going forward, the gate length is shrinking and also the supply voltage, with corresponding reduction in noise margin. He assumes that, because of the saturation effect, Vcc will not get smaller than 0.7V. He explained the example of a usual car today where there are a lot of possible interferences for the control CPU's, coming either from the on board local bus or from external devices like mobiles and computers. He continued by showing how in the near future the conducted emission of the parts will increase more than the tolerable emission level from the customers. There is need for guidelines to manufacture IC's with lower emission.

He explained that today, in the manufacturing process, there is the necessity to do EMC simulations and compliance checks before fabrication of the IC. EMC problems are the third largest cause of redesign of IC's. At this point, IBIS can be a great help for modeling the package and the core. For the package, IC-EMC creates a 3-D reconstruction of the package, and is using about 10 hidden keywords, which gives precise info about the leads. He showed results, where the comparison of simulation and measurements of the radiated emission showed good correlation of the emission level.

He finished his presentation showing an outlook for the future of EMC models. For frequencies of less than 3 GHz, the emission is well understood, but with increasing frequencies (e.g. 10-40 GHz, nowadays there exists no solution). But he is confident that within the next 10 years a solution will be found. He pointed out that the tool and the manual are available online.

The first question was how he gets the information about the die size. Etienne answered that either the vendor is supporting the info or an X-ray is made of the die and the bond wire. The next question was whether he is using from an IBIS model only the ramp-section or the exact information of the rising and falling waveforms. Etienne said that he is using the waveform information. And he pointed out that the clamp I-V curves are of high importance for EMC. The next question was about the driver for EMC and Etienne answered that the automotive industry is the main driver, but that also for the telecomm industry, EMC is getting more important. The next question was about the ideal power supply for his simulations. Etienne answered that he is working on the problem, that for future releases the power supply will no longer be modeled as ideal, but with parasitics. The last question was about the field solver he is using, and he pointed out that he is using a 'simple one' as, at the moment, the switching frequencies are not that high.

IDEM AND MPILOG: MACROMODELING TOOLS FOR SYSTEM-LEVEL SIGNAL INTEGRITY AND EMC ASSESSMENT

Flavio Canavero, Michelangelo. Bandinu, S. Grivet-Talocia, Ivan Maio, and Igor Stievano, Politecnico di Torino, Italy

Igor Stievano explained that at his university two modeling tools are available. The first is the well-known Mpilog for creation of macromodels for active circuits. The second, IdEM, can be used for the modeling of interconnects.

Igor began with a review of how the model creation is realized in Mpilog. He creates a 2-piece

model representation of the output, which contains information about the fixed logic High and Low state and weighting signals for the state switching (these corresponds to the IBIS static and dynamic curves). This approach is a parametric relation to approximate a nonlinear dynamic system, which as an equation is now compliant with IBIS 4.1, as the equation can be implemented in SPICE or VHDL-AMS. He showed the graphical interface for the Mpilog tool, which helps you during the necessary steps to create and validate the macromodel.

In the second part of his presentation he explained the tool IdEM, which is suitable to create models for interconnects and vias. The process is to make measurements of the parts and also to do EM simulations. The results are used for the computation of the transfer function, which will then be 'transformed' to a macromodel description. He also showed the GUI of the IdEM tool.

Igor invited all participants to come to the university booth in the afternoon, where there will be presentations of the tools in the afternoon.

The first question following the presentation was whether his tools are stand alone or require any additional third party tool. Igor explained that the tools can be downloaded for free and that both tools can be used as stand alone tools. The second question referred to causality, and Igor explained, that causality is not yet implemented, but also that this needs to be enforced by measurements.

FORWARD LOOKING TRENDS IN SERDES MODELING

Eric Rongere and Stephane Rousseau, Mentor Graphics Corporation, France

Eric Rongere opened his presentation with examples that showed that, with the appearance of state of the art communications channels, there are features which can not be adequately modeled with IBIS, like equalization and receivers with slew rate sensitivity. He continued by showing the multilingual extensions of IBIS 4.2, which could address almost all of the limitations, and that for a particular solution there exist different options to realize these extensions. For the first option, using transistor level SPICE models, there exist some cons like encryption to hide IP and that complicated models are prone to hidden problems and instability. He continued with the second option, using macro-models, which will be faster than SPICE models, but the current building blocks are only proven for IBIS 3.2. The third option would be using analog-only AMS. AMS is a language to which almost each vendor has access, but the problem might be the complexity of the language. Another option is VHDL-AMS or Verilog-AMS, as they are international standards and simulation is relatively fast. But at the moment only one vendor supports full AMS in their SI tool. The last option would be algorithmic modeling, which is vendor neutral. Measurements could be defined and encryption would also be possible. On the other side there is no EDA vendor supporting this feature at the moment.

Eric then continued with the results of two studies of AMS. The first study used a VHDL-AMS driver with pre-compensation, S-parameter models for the packages and a VHDL-AMS receiver with an eye-mask for measurements. In the second study it was possible to create automated DDR2 measurements for the complicated DDR2 electrical and timing constraints, which are not part of normal IBIS keywords. He ended his presentation with the conclusion that IBIS 4.2 with his multi lingual extensions gives the user the possibility to use SPICE and/or VHDL-AMS. But, there are still a lot of measurement facilities which should be defined in IBIS or be described with the multilingual approach.

One question was whether for the second study, the power supply was an ideal one. Eric answered yes and then pointed out that the modeling of a non-ideal power supply is under development. The next question was about the influence of cycles for the eye-diagram shown. The answer was that for an eye-diagram the ISI phenomena and the jitter plus the reflections have an influence on the results. Furthermore, the main reason for using VHDL-AMS was to show that a 10 million pattern simulation could be done in a reasonable time. The next remark was about the ODT, because taking care of this feature would increase the necessary pattern amount tremendously. The next question was about VHDL-AMS and the way it is used. For getting the speed advantage an abstract model is necessary (not Kirchhoff-like) and a defined subset will be needed. The last question was on how to use algorithmic modeling: how can it be assured that for an approach such as C-based, the vendor will support all different kinds of compiled versions like that for Windows, Linux, Solaris etc., as the IP must be protected? Nobody had an answer.

The meeting adjourned for a break.

GATE MODULATION SOLUTION VALIDATED BY VHDL-AMS IMPLEMENTATION

Antonio Girardi, Giacomo Bernardi, and Roberto Izzi, STMicroelectronics, France

Antonio Girardi started with an explanation of the gate modulation problem in IBIS. He pointed out that in normal operation and/or SPICE simulation, the effective working point is moving (horizontally) along the different Vgs curves for the different Vdd voltages. In IBIS this is not possible, and therefore the working point moves along the curve with a fixed Vgs (vertically). He then showed a comparison between SPICE and IBIS, where there exists large discrepancies in delay, overshoot and power supply behavior. Therefore, ST introduces two coefficients that will modulate the standard IBIS currents for pullup and pulldown curves. These coefficients must be supplied in table format, and then the problem appears of how many tables are necessary and how can the interpolation between the tables be described?

Antonio showed that in the saturation zone the coefficients are independent from the Vds voltage and that in the linear zone this is approximately also valid. He said that, as it is not possible to change the algorithm of how the tools are treating/using IBIS models, the calculation of the effective pullup/pulldown currents have to be done with VHDL-AMS inside the IBIS model, and the tools then use these effective currents. Antonio then explained that the correlation between SPICE and the modified IBIS are now very good. He said that the gate modulation algorithm was implemented in VHDL-AMS and also the correct power supply parasitics (as used by BIRD95.6) were modeled. In his last slides he showed a way for IBIS BIRD98 and the ST proposal to converge by making two additional changes to the BIRD. The first is to take into account that the control logic and the final stage might be at different supply voltages. Therefore, the Vgs-voltage of the output transistor is independent of VDDcore. The second is a change to the measurement method. This would mean that the opposite transistor should be disconnected during the measurement. (e.g. for measuring pulldown-curve, the high –transistor should be switched off.) He ended his presentation with the remark that at the moment the miller capacitances are not included and that the proposal works now only for CMOS.

The first question asked if the points in the table should be ‘combined’ with splines or just linear. Antonio answered that more investigation is necessary. The second question asked about the

influence of the coupling capacitors of the power supply. The answer was that the inductance and also the capacitance have to be taken into account, because it is not possible to have ideal currents on a board. Especially, the enhancements of BIRD96.8 for the power network must be added to get reasonable results for BIRD95.

EXPERIENCES WITH DRIVER SCHEDULES

Eckhard Lenski, Nokia Siemens Networks, Germany

Eckhard Lenski began his presentation with a short overview and reminder about the [Driver Schedule] keyword. He explained the different parts of such a model, which consist of the parameters (found in a normal IBIS model), the scheduled models, and the top level model information, which is there to give an approximate description of the model for tools which do not understand the [Driver Schedule] keyword. Then, he showed an example that consisted of three I/O models. He showed how at different times according to the values for Rise_on_dly and for Rise_off_dly, the I/O models are switched on and off. In the second part of his presentation he showed his different experiences with driver schedules. For a schedule that consists of pure CMOS push-pull drivers, it was seen very clearly how, with the use of [Driver Schedule], the slew-rate and the drive strength of the output changed with time. His second example was of an open-sink model, which used an additional pullup-driver for an amount of time. Furthermore, he compared the delivered top level model with the results of the open-sink driver alone and with the behavior of the correct driver schedule. It could be seen that in the correct driver schedule behavior, the additional pullup-drive showed a voltage that was about 10% higher compared to the main model alone.

In his last example, which was used for pre-emphasis modeling, he showed some problems that occurred when he compared static and dynamic waveforms. In addition, the scheduled model showed the expected pre-emphasis behavior, but the voltage level was not correct. He pointed out that he is still examining what happened with the model. He ended his presentation with the conclusion that [Driver Schedule] can be used to model multistage drivers, but still they have to be checked more carefully than normal IBIS models. He suggested that maybe the ibischk tool should be enhanced to check [Driver Schedule] more thoroughly.

There was only one question on how the extraction of the different driver stages was done. He answered that each driver stage must be modeled on its own, and than the tools have to put them together.

MIXED SIGNAL CHANNEL MODELING APPROACH TO SI ANALYSIS

Saliou Dieye and Riccardo Giacometti, Agilent Technologies, France

Saliou Dieye started his presentation with an overview of a complete transmission path, which starts with the preconditioning of the driver signal, continues with the analog driver itself, then comes the physical channel, and at its end is the analog receiver, where inside the chip the signal recovery has to take place. Then, he continued with a look at the different model types that can be used to model passive components; there are S-parameters, analytical models, IBIS models and SPICE models. For example, for the transmission line, measurement based models can be used. For the vias, connectors and packages, with the help of a field solver, basic analytical models can be created. The models for active parts can also look different depending on the model the IC vendor is supplying, such as IBIS, HSPICE or Verilog-A. Showing the topology of the channel which was analyzed, he explained for which components

which models were used. He mentioned that nowadays a simulator should have the possibility to use all kinds of models. He listed the analog components of a channel: transmission lines, connectors, packages and I/O models on one side, and the digital signal processing (DSP) components such as the equalizer, clock and data recovery and the SerDes models on the other side. He asked if both can used together in a single simulation. He said that DSP components can be described, e.g in C/C++, Matlab, or HDL.

At the end of his presentation, he explained, with the help of a schematic overview, which parts of the channel were DSP and which were analog. He showed that the simulation results not only can be shown in an eye diagram, but also statistical analysis can be done and even bit error ratios can be calculated. He explained that the impact of crosstalk between multiple channels had been analyzed.

It was asked which engine he was using, and Saliou explained that his tool can do simulation in the time domain, but also by use of a convolution engine, he can do analysis in the frequency domain. The next question was about S-parameters and how to use them in the time domain analysis. Saliou said that the tool can create SPICE models out of the S-parameters.

IBIS MODELS WITH REACTIVE LOADS

Manfred Maurer, Siemens AG, Germany

Manfred .Maurer started his presentation with the remarks that he is working on everything from development of ICs to the SI-analysis of whole PCBs. Normally the loads in PCB applications are resistive, but in one of his tasks he had to work with reactive loads. He explained that this is mainly the case for the automotive industry, where there exist coils and reactive loads for motors. Furthermore, the voltage slopes are moderate, but there exist high voltage swings and high currents. So, the main focus here is on EMI radiation and susceptibility. He showed an application where big differences between measurement results, transistor based model simulations and analysis with the use of IBIS models occurred. And, these results could also be shown in the frequency domain.

He mentioned that Arpad Muranyi had identified the problem with reactive loads in his presentation at DesignCon 2006, where he showed that the normal algorithms are only valid for resistive loads. This is because the calculation of the current with a resistive load can be done using Ohms law, but for inductance and capacitance, the deviation for time has to be used to calculate the current.

Manfred continued that he then tried to combine the loads for R_fixture, C_fixture and L_fixture by modeling everything with voltage controlled voltage sources (VCVS), and the results were very surprising. He made five different models, one transistor based, one with the above-mentioned VCVS, and three IBIS models which contained an R_fixture, a C_fixture or an L_fixture value. He said that there is no unique way to get the right parameters and nothing can be found in the cookbook. His results showed large differences between the different loads, especially for the three IBIS models, whereas the transistor based models and the VCVS showed more comparable results. He said he found it more surprising that when he used the model with the same reactive load as the load he expected in the application, the agreement was very good, but that for a slightly different reactive load, the results were unpredictable. This implies that for each application there should be a unique model, but this is not practical, as a large number of waveforms would be needed. The superposition of different models with

different reactive loads is not simple, and more investigation is needed. He concluded that, at the moment, only transistor based models and VHDL-AMS models can handle reactive loads.

The first question was about the possible simplification of the models used in his application. Manfred pointed out that the simplification for the drivers (e.g. using just ramp values) is only valid for reactive loads and could not be used in his analysis. The second question was about the value of the inductive loads. He said that in automotive applications loads of 1mH are common (compared to ~10nH in other applications). The last question was about the polynomial coefficients for the VCVS and how to get them. Manfred pointed out that at the moment there are no general rules, and most have to be figured out by trial and error and with the help of intuition.

CLOSING REMARKS

Ralf Bruening thanked once again the sponsors and the presenters and said it was a very successful meeting. He invited everyone who had time to stay longer. He also invited everyone to the next DATE2008 summit, which will take place in Munich in March 2008.

Afterwards, the discussions continued until 2:30pm (although the official meeting ended at 1:00pm).

NEXT MEETING

The next teleconference will be held April 20, 2007 from 8:00am to 10:00am US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org
In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda-stds.org
To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda-stds.org)
IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org
To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	February 16, 2007	March 9, 2007	March 30, 2007	April 19, 2007
Advanced Micro Devices	Producer	Active		√	√	
Agere Systems	User	Inactive				
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive				
Apache Design Solutions	User	Inactive				
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
Cadence Design Systems	User	Active			√	√
Cisco Systems	User	Active	√	√	√	
Ericsson	Producer	Active		√	√	√
Fluent	Producer	Inactive				
Freescale Semiconductor	Producer	Inactive				
Green Streak Programs	General Interest	Inactive	√			
Hitachi ULSI Systems	Producer	Inactive				√
Huawei Technologies	User	Inactive				
Integrated Circuit Systems	Producer	Inactive				
Intel Corp.	Producer	Active	√	√	√	
LSI Logic	Producer	Inactive				
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Active	√	√	√	
NEC Electronics Corp.	Producer	Inactive				
Nokia Siemens Networks	Producer	Inactive				√
Panasonic	Producer	Inactive				
Samtec	Producer	Inactive				
Siemens AG	Producer	Active		√	√	√
Signal Integrity Software	User	Inactive				
Sigrity	User	Inactive				
Silego	Producer	Inactive				
STMicroelectronics	Producer	Active	√	√	√	√
Synopsys	User	Inactive				
Teraspeed Consulting	General Interest	Active	√	√	√	
Texas Instruments	Producer	Inactive	√	√		
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive	√			
ZTE	User	Inactive				
Zuken GmbH	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
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