IBIS Open Forum Minutes

Meeting Date: **August 28, 2020**
Meeting Location: **Online Virtual Summit**

VOTING MEMBERS AND 2020 PARTICIPANTS

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Dassault Systemes (CST)	Stefan Paret
Ericsson	Anders Ekholm, Sungjoo Yu, Thomas Ahlstrom
Google	Zhiping Yang*, Shuai Jin*, Zhenxue Xu, Hanfeng Wang* Songping Wu*, Yimajian Yan*
Huawei Technologies	(Hang (Paul) Yan)
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Infineon Technologies AG	(Christian Sporrer)
Instituto de Telecomunicações	(Abdelgader Abdalla)
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SerDesDesign.com	John Baprawski
SiSoft (MathWorks)	Mike LaBonte*, Walter Katz*, Graham Kus
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SPISim	[Wei-hsing Huang]
Teradyne	Dongmei Han, Edward Pulscher, Sheri Zhuang Tomoo Tashiro, Paul Carlin, Tao Wang
University of Florida	Shuo Wang*
Unaffiliated	Colin Brench*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
September 18, 2020	627 261 744	Friday1

For teleconference dial-in information, use the password at the following website:

https://tinyurl.com/IBISfriday-new

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IEEE EMC+SIPI 2020 IBIS Summit took place on Friday, August 28, 2020 as an online virtual meeting. About 45 people representing 27 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/aug20/

Randy Wolff opened the summit by welcoming everyone and thanking them for joining. He noted that this was the first collaboration between IBIS and the IEEE EMC Society and that he looked forward to more as we all work on standardizing PI modeling. Randy briefly reviewed the agenda and introduced the first speaker.

INTRODUCTION TO THE EMC SOCIETY AND PI STANDARDIZATION

Alistair Duffy (De Montfort University) (President, IEEE EMC Society)

Alistair thanked IBIS for hosting its first summit in conjunction with the EMC+SIPI symposium and remarked that it would be even better to have it in person. He noted that Vignesh Rajamani has been working with IBIS on a memorandum of understanding to foster this collaboration. He said there was a movement within the society toward standardization in a unified SIPI context, and IBIS was a key stakeholder in this area.

Alistair introduced the EMC Society and noted that its mission statement is associated with the exchange of knowledge to benefit the industry, the profession, and humanity. It is interested in topics that benefit the industry as well as academic pursuits. It aims to be a respected global organization and leading provider of scientific and engineering information on EMC.

Alistair said the society's field of interest is quite broad and covers components, systems, measurement techniques, standardization, education, and anything related to compatibility and interoperability. It has 12 Technical Committees and 5 Special Committees. He suggested TC10, Signal and Power Integrity, might be of most interest for cooperation with IBIS, but it is certainly not the only one.

Alistair introduced IEEE P370, Electrical Characteristics of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz, as a first step in SIPI standardization. He said Xiaoning Ye, et. al., had done a fantastic job with this, and it represents a great example of a well led standard in that it's good for the profession, introduces new material, and has collaboration and support amongst members who were otherwise competitors. He joked that 50 GHz might not be high enough for everyone and that some attendees considered it close to DC.

He reported that a PI Standard Sandpit is planned for the October-November timeframe. The goal is to identify potential standardization activities for the IEEE, and it will be funded and sponsored by the Standards Society. Its aim is to draw a diverse group to focus on novel approaches to addressing the dearth of standards for PI. He invited IBIS members to take part.

In summary, he mentioned that TC10 might be a natural point of communication with IBIS, but there are others and Zhiping Yang is driving the collaboration efforts. He also mentioned the EMC Society's Letters on EMC Practice and Application (L-EMCPA). He said that if IBIS felt there would be benefit in having a special issue or special section related to the IBIS work, he would speak with Frank Sabath, Editor in Chief and Past President of the EMC Society, about organizing it.

Bob Ross asked if a Sandpit had been used before for standards activities within EMC. Alistair said he thought it was the first time it had been used for this purpose within EMC. Randy Wolff asked if IBIS members interested in joining the Sandpit also had to be IEEE members. Alistair said they did not. Ed Hare, VP Standards of the EMC Society, said being a member of a working group does not require IEEE membership. He said that Chairing a working group requires IEEE membership and membership in the Standards Committee, but that the incremental cost of adding things on top of an IEEE membership is worth the price given the power to influence standards in one's field. Vignesh Rajamani, VP Member Services of the EMC Society, introduced himself and thanked Zhiping for his work setting up the meeting.

IBIS CHAIR'S REPORT

Randy Wolff (Micron Technology)

Randy provided an introduction to IBIS itself. He noted that IBIS membership is based on organizations not individuals. IBIS currently has 27 members and is made up of corporate members and academic members, the latter of which is a newly created reduced-cost category. Membership is a mix of EDA software companies, device vendors who produce IBIS models for their customers, system designers who use IBIS models in their design work, and others

interested in improving IBIS modeling. The IBIS year runs from June to May, with annual elections held in the May timeframe.

Randy described the status and activities of the IBIS Open Forum. SAE ITC is the parent organization of IBIS, providing financial and legal services. SAE works a lot in automotive and aerospace standards. IBIS has four task groups holding weekly teleconferences. The ATM and Interconnect task groups discuss new technical content, the IBIS quality task group focuses on the ibischk syntax parser and overall model quality, and the Editorial task group, which meets only as needed, works on new IBIS specification documents. Most technical and editorial changes (BIRDs) are discussed in task groups prior to introduction at the main IBIS Open Forum, which holds a teleconference every 3 weeks. This is the first Summit in conjunction with the EMC + SIPI symposium, but IBIS holds annual Summits associated with DesignCon (USA, January-February), with IEEE SPI (Europe, late spring), and in Shanghai, Taipei, and Tokyo (with JEITA) in November. IBIS Summits had 368 participants in 2019.

The latest IBIS milestone is the release of IBIS 7.0 and the ibishchk7 parser to support it. Beyond IBIS 7.0, there are currently 9 approved BIRDs with three more expected to be approved in time for the next IBIS version (likely called 7.1). Randy reviewed IBIS milestones from its creation in 1993 as the I/O Buffer Information Specification (IBIS), which provided faster behavioral simulations of buffers and protection of IP as opposed to transistor level SPICE simulations, through additions over the years for package modeling, boards, AMS languages, Algorithmic Modeling Interface (AMI) for SerDes simulations, power-aware simulations, and the recently added ability to include Touchstone and SPICE models for interconnects. Randy noted that the upcoming IBIS 7.1 includes extensions for AMI to better handle single-ended signaling standards like DDR5 memory, enhancements in PDN modeling (on-die capacitance in particular), back-channel optimization for statistical simulation, and a major improvement EMD (electrical module description) allowing improved modeling for stacked-die packaging, multi-chip modules and system level boards.

Randy noted that IBIS started with I/O buffers and interconnect, and the main use of IBIS was in EDA simulations for SI issues. He said we see an increasing demand for PI modeling, as increasingly SI engineers need to understand PI issues as well. IBIS must evolve to meet the SI and PI demands of new signaling technologies. PDN modeling is critical to system design, and he said we see potential for IBIS to enable improved modeling of voltage regulators and chip power. Randy thanked everyone in attendance for their interest and reviewed the process of submitting a BIRD (Buffer Issue Resolution Document), the vehicle for introducing a change to the specification.

Zhiping Yang noted that anyone can participate in IBIS discussions and even submit a BIRD. Participation in task groups and discussions is open to everyone. Randy said this was a good point and noted that only members can vote on BIRDs, but anyone is free to create or contribute to them.

BRIEF REVIEW OF PDN IN IBIS

Bob Ross (Teraspeed Labs)

Bob presented an introduction to IBIS topics and the history of PDN specific constructs. He noted that an IBIS model is largely made up of “measured values,” either physical measurements or the results of transistor level SPICE simulations. Algorithms to be used by

simulators are generally not specified in IBIS, with one exception that is noted later.

Bob reviewed high level element keywords including [Component], its [Package], and [Model]s for I/O buffers. He noted that this information is sometimes available in forms other than IBIS, but they may have issues with availability, widespread compatibility, or simulation speed.

Bob reviewed [Model] elements including transistor I-V tables, V-T tables for device output transitions under different loads, and typ/min/max corners following process, voltage, temperature (PVT). He noted that C_comp, effective capacitance, is one quantity for which typ/min/max is magnitude based not process corner based, as capacitance typically is a function of the metallization not PVT. However, there is a C_comp_corner that follows PVT if that is required. Bob noted that 21 [Model] types are supported for modeling various types of buffers.

Bob reviewed the history of packaging constructs in IBIS starting with [Package], which provided a single R, L, C model of parasitics for all of a [Component]'s pins. This was later followed by the [Pin], which provided per-pin R, L, C models, and later the [Package Model], which provided coupled R, L, C matrices or uncoupled multi-element transmission line paths.

Bob described the required [Pin] keyword, which gives pin to buffer mapping information, and the [Pin Mapping] keyword, which can be used to map PDN rails to individual buffers and was IBIS' first foray into simultaneous switching noise (SSN) analysis.

IBIS buffer modeling started with static I-V tables for transistors, and V-T tables for output transitions were later added. The 2-equations 2-unknowns algorithm, which is commonly used to convert the V-T table information into Kpu(t) and Kpd(t) waveforms that modulate the static I-V table information, provides a way to simulate behavior during device transitions. Gate modulation effects were later modeled by further modulating the I-V table values, and this is one instance when the IBIS specification essentially prescribed the algorithm for doing so. [Composite Current] tables were introduced to provide information on a buffer's overall current draw, not just current delivered to the output. In IBIS 7.0, a new general [Interconnect Model] documents pin, die pad, and buffer interfaces and allows high fidelity models connecting the various interfaces with Touchstone or IBIS-ISS (IBIS Interconnect SPICE Subcircuit) models. BIRD198.3, recently approved for the next version of IBIS, provides a simple fixed topology PDN model that is sufficient in many cases. Finally, the upcoming [Electrical Module Set] provides high fidelity interconnect modeling for boards, modules, stacked dies, etc.

Zhiping Yang thanked Bob for an excellent overview of the history of PDN constructs in IBIS.

IMPROVING POWER SUPPLY INDUCED JITTER SIMULATION ACCURACY FOR IBIS MODELS

Yin Sun, Chulsoon Hwang (Missouri S&T)
[Presented by Yin Sun (Missouri S&T)]

Yin Sun introduced the topic of PSIJ as the variation in output transition edge timing due to fluctuations in the power rail. She then presented comparisons of SPICE and power-aware IBIS simulations demonstrating that current power-aware IBIS models do not capture the shift in the

timing of the output edge. Power-aware IBIS models using the [ISSO PU] and [ISSO PD] tables for the gate modulation effect produce only a multiplicative scaling of the Kpu(t) and Kpd(t) time varying waveform scalers. Therefore, they can model amplitude and edge rate changes but not time shifts.

Yin introduced a new behavioral model proposal in which the existing Kpu(t) and Kpd(t) scalers are augmented with two additional additive terms with time varying coefficients. These terms are linear and second order functions of the time averaged power rail voltage Vcc(t). Additional data necessary to compute the new coefficients was described, and an implementation of the new behavioral model in Ngspice was presented. Yin then reviewed simulation results under several different Vcc waveform variations including very low frequency Vcc noise and Vcc noise frequency corresponding to the propagation delay through the device. The results demonstrated good agreement with SPICE simulation results.

Bob Ross commented that in some of the results comparisons (e.g., slide 10) the time axes on the plots were different. He noted, however, that the difference was merely a shift, and the total time range and scales of the plots were consistent. So, the comparisons of edge rate, shifts between the 3 cases, etc., were still perfectly valid.

Walter Katz asked about slide 9 and whether it referred to multiple buffers (e.g. M=128) switching in parallel, for example 128 DQs switching at the behest of a controller. Yin and Chulsoon Hwang said the schematic and factor M referred to the length of the inverter chain in an individual buffer, and they noted that delay was a function of the length of the chain. Randy Wolff said the results presented would be accurate given the Vcc noise were local to the individual buffer. Walter said solving for the individual buffer is important, but an important problem is understanding the on-die decoupling and how the voltage rail reacts when 128 DQs are in various states and switching asynchronously. He said the frequency of that noise tends to be what's important to people, and the high frequency noise from an individual buffer transitioning is something that would likely be filtered out of the signal by the time it left the package.

Zhiping Yang said that this was an excellent presentation and could be used to help IBIS modeling deal with edge shifting effects. He said that the current IBIS model extraction techniques explicitly excluded the pre-driver edge timing effects from appearing in a typ/min/max waveforms comparison. They are removed from the waveforms because of the definition of t=0 in the IBIS extraction process.

STANDARD POWER INTEGRITY MODEL (SPIM) WITH UNIFIED PI TARGET (UPIT)

Kinger Cai*, Baolong Li**, Suomin Cui***, Ji Zheng****, Zhiping Yang*****, Songping Wu*****
(Intel Corp.*, ANSYS**, Cadence Design Systems***, Aurora System****, Google*****)
[Presented by Kinger Cai (Intel Corp.)]

Kinger noted that the foundations of IBIS itself were first developed by Intel for internal use and then advanced as an industry standard. This presentation described PI design challenges that face the industry, largely the result of a lack of standardization, and described some methodologies Intel had developed. These have been adopted by some EDA vendors, and the goal would be to have them widely adopted in the industry by device vendors, EDA platforms, and system designers.

Kinger noted that PI design is often an inefficient process for the platform designer. It often involves adapting reference designs, performing time-consuming what-if simulations, and a complicated non-standard review and sign off process. The goal is to provide a standardized framework that is flexible and efficient, protects vendors' IP, and still guarantees accuracy.

Fast PI is a platform PI design standard that could be adopted and implemented by EDA platforms. It utilizes SPIM (standardized PI Model), which provides a PI Model for each power rail in a SoC/Pkg to the customer. It also utilizes UPIT (unified PI target), which provides an impedance target for each power rail.

The chip vendor would provide the SPIM and UPIT to its customers. This collateral is minimal and standardized. It is sufficient to allow the system designer to design the PDN, but it protects sensitive IP. Kinger noted that the UPIT would typically extend from essentially DC to about the 10s of MHz. He said board level capacitors can only influence behavior through this range. The platform designer has no influence on the package or on-die design, and they will assume that the chip designer has provided sufficient caps to take care of the high frequency, and the package designer has enough to take care of the middle frequencies.

The SPIM itself typically contains an S-parameter model from the BGA/pins to the bumps. A vendor might choose to include on-die power distribution information as well, but this typically isn't necessary for the platform PI designer. Kinger said the chip vendor would also typically want to provide a weighted and normalized AC source, as the chip vendor understands the current distribution on the chip. The SPIM would also define the sensing/observation port, at which the UPIT impedance target is observed. Lastly, the SPIM model is Pin/BGA aware, so it can be directly merged as a virtual PKG database with the physical BRD data base. The SPIM protects IP and is compatible with SPICE simulation.

Kinger presented some correlation data showing good agreement between the UPIT-SPIM results with SPICE simulation and post-Si measurements. He noted that SPIM and UPIT have been standard PI collateral from Intel since Ice Lake in 2017. He said two leading EDA vendors now fully support it, and it has been adopted by Intel's customers. They hope to make it the first PI standard in the industry, similar to the way IBIS supports SI design. He presented a mock-up IBIS BIRD draft example showing how the port grouping, the package .sNp, and the observation port .s1p might be specified, and he noted that specifying the weighted source would be defined in the future.

Kinger said the call to action included forming a platform PI design standardization working group, getting chip vendors to support FastPI, getting EDA vendors to support FastPI, getting system designers to adopt SPIM and UPIT, and ultimately submitting a BIRD so IBIS could provide SPIM and UPIT information.

Shuo Wang noted that this proposal was for a comprehensive model, and he asked how it is provided and how we can prove its results are correct. Kinger referred to slide 11, which illustrates correlation between measured and predicted results, and he noted that Intel had been using this methodology for a long time and demonstrated good results.

Shuo asked about the VRM model blocks that appeared in the presentation, and he asked if the details of VRM design, which might affect mutual impedance and inductance effects at higher frequencies, were considered. Kinger said this was a good question, and that from the point of

view of platform design they spend time figuring out how to simplify the VRM model. Kinger noted that they typically get SPICE or SIMPLIS models from their VRM vendors, but those are still too complicated for what they're trying to achieve with this platform PI design process. After a VRM is well defined from a PD perspective (parameters like Vnom, etc.) and tuned, they create what they call a compact model of the VRM. This model might be a very simple model with a few discrete components, or it might involve something more complicated like a feedback loop. Kinger said Intel has a lot of experience with this, and this conversion process is a mature methodology for them. He said this topic may be the subject of a future presentation. He noted that they have demonstrated good correlation in frequency domain between their compact VRM models and the original vendor-provided models.

Yimajian Yan noted that Kinger had mentioned good correlation of the compact VRM models in "frequency domain", and he asked if there were any concerns about time domain and non-linear response. Kinger said this was a good question, and that as part of this platform design process they are modeling and correlating a worst-case design scenario.

IBIS BASED BUCK CONVERTER DC MODELING

Zhiping Yang, Songping Wu, Shuai Jin, Zhenxue Xu (Google)
[Presented by Shuai Jin, Zhenxue Xu (Google)]

Shuai Jin described the simulations involved in system-level power delivery network design. These include system-level DC simulations including IR drop and DC resistance, AC simulations such as PDN impedance, transient simulations of load response and power noise, system power consumption and efficiency, and power/thermal co-simulation. Shortcomings of DC simulation come from having no DC-DC converter model information and no power consumption and power efficiency information. A model was proposed for a DC-DC Buck converter that could be provided by vendors through a new IBIS model format. The model would be used to simulate switching behavior and conduction power loss. With the model, system power consumption and efficiency can be evaluated. With an IBIS model, DC simulation for all power rails could be set up automatically.

The Buck converter is a step-down DC-DC converter and is a type of switching mode power supply, providing much higher power efficiency than a linear regulator. The switching and conduction power loss could be modeled through a set of key parameters. The simulation tool would calculate the power consumption in its own solver. The equations for calculating buck converter power consumption in continuous current mode (CCM) were shown. Discontinuous current mode (DCM) is the second mode of operation, and the boundary between continuous and discontinuous current modes was defined. Equations for DCM were defined. A comparison was shown between simulation and measurement for DCM and CCM power efficiency.

Randy Wolff asked which material was new relative to the presentation at the DesignCon IBIS Summit. Shuai said the earlier presentation proposed a method for CCM, and this new presentation also includes DCM. The buck converter IBIS model format proposal itself has not changed. New equations were added for DCM. He noted that in the future they may also propose ways to support a boost converter and other typical DC-DC converters.

Shaowu Huang asked about slide 21 and the correlation between measurement and calculation. He asked if there were plans to improve the correlation, particularly in the DCM

region. Zhiping Yang noted that this is a first step, and there are secondary effects that are not yet accurately modeled. He said one of the benefits of a keyword based IBIS model is that you can add more keywords as necessary and improve the models over time.

John Yan said he liked the direction of this proposal, but he wondered if there had been any pushback from vendors on providing the information. For example, he could see a vendor being reluctant to share their body diode loss. Zhiping said this was a great question, and that typically they'd tried to use parameters that came from a data sheet. He said in his experience the PMIC information was the most sensitive information for most DC-DC converter vendors. That hadn't been addressed here, but IBIS AMI might be a good vehicle if there is sensitive modeling information that has to be hidden. He said they are working with SC5 to help get more vendors to support the proposal.

Meilin Wu asked about how the power efficiency measurement was done. Zhiping said he wasn't familiar with the exact setup used for the measurement here, but he thought it was done with an industry standard process for measuring the efficiency under different load conditions. He noted that Zhenxue (Aaron) Xu had taken the measurements and would be able to answer any more detailed questions offline.

IBIS BASED BEHAVIORAL MODELING FOR BUCK CONVERTER

Anfeng Huang*, Jingdong Sun*, Hongseok Kim*, Jun Fan*, Chulsoon Hwang*, Zhiping Yang**, Yimajing Yan**, Hanfeng Wang**, Songping Wu**, Shuai Jin**, Zhenxue Xu** (Missouri S&T*, Google**)
[Presented by Anfeng Huang (Missouri S&T)]

Anfeng Huang noted that PDN design is influenced by the voltage regulator module (VRM). The presentation detailed modeling of a current mode buck converter VRM. The impedance of the VRM dominates the PDN at low frequencies below about 100KHz. The current mode buck converter is a type of switching mode device. There is a feedback control loop that influences the steady state output voltage variance under different input and loading conditions. Voltage droop and recovery time relate to the feedback response. There are two methods of controlling the VRM, pulse width modulation (PWM) and pulse frequency modulation (PFM).

Existing VRM models are directly provided by device vendors and are typically encrypted due to IP concerns. These models are limited as they are not compatible with typical IBIS simulators, and simulation speed and convergence concerns exist. The proposal for an IBIS model is an equation based averaged model with the same behavior. Advantages are an equivalent transfer function not revealing the exact circuit implementation and simulation speed that is much faster than existing models for switching behavior. The analytical equation includes parameters related to the power stage, the current feedback loop, and the voltage feedback loop. This proposal is only valid for the current mode buck converter, and only the PWM controller is discussed. The model could be easily modified for a PFM controller, and equations for that are found in the backup slides. Other parameters not related to the device physical parameters are system-controlled parameters that come from the system designer and other optional parameters coming from the vendor or the system designer.

For validation of the model, the steady state output voltage response was compared between the SPICE model and the proposed averaged model, with good agreement for the PWM

controller. The transient output voltage was also shown. The rise time of the output voltage matched well. A large difference in voltage ripple was due to switching, but a smaller difference would be observed if the SPICE simulation results were filtered. The steady state output voltage response was also shown for the PFM controller, and simulation results also matched well. The voltage drop generated during the load transient was shown to be accurately captured by the averaged model of the PFM controller. Finally, simulation speed was compared between a SIMPLIS model, and simulation of the SPICE model and the proposed model. The proposed model was significantly faster to simulate than the SPICE model. It was also noted that the SIMPLIS model does not support S-parameter blocks and IBIS models commonly used in PDN analysis.

Future work will look at discontinuous current mode operation, AC simulations, and inclusion of DC and switching loss characteristics.

Arpad Muranyi asked about the intended use of these VRM models and whether they would be used as part of traditional IBIS SI simulations or just for PI analysis. He said his concern was that you had to run a simulation for ms to see the effects of the regulator on what the buffers see for power, and this is an incredibly long simulation to run when you need ps time steps to deal with buffers switching in the GHz range. Arpad referred to slide 4, which shows the frequency ranges over which the VRM, PCB, and Die & PKG dominate the impedance. Chulsoon Hwang agreed that a typical SI simulation might not care about this low frequency noise on the power rail. However, if you're worried about PSIJ, which provides a connection between PI and SI, then you have to simulate these low frequency VRM effects. He agreed that this could produce very long simulations, but he said that's an issue we can work on addressing. Zhiping Yang said that the figure on slide 4 is for a typical on-board DC-DC converter. He noted that there is a trend to move the DC-DC converter into the package or even on the die. As they move closer to the die you typically see the switching frequencies increasing and more overlap in the SI frequency range. Zhiping said he was aware of some 100MHz switches on die. Arpad agreed.

Usman Saeed asked about how we could incorporate min, max, typ corners for these models and also parasitics and their process variations. Zhiping noted that IBIS model keywords typically provide typ/min/max values, and he asked if we needed more ways to specify corners for these. Randy asked if the parameters used in these behavioral VRMs would typically have ranges associated with them.

Shuo Wang noted that the equations presented for CCM and DCM were quite different and asked if it was possible to model mode switching between the two modes. Arpad suggested that the authors might consider implementing their behavioral model in Verilog, and then the multi-lingual extensions in IBIS could handle it already.

MODEL FOR INDUCTOR LOSS IN SYSTEM-LEVEL POWER INTEGRITY ANALYSIS AND OPTIMIZATION

Yimajian Yan*, Stephen Ellsworth** (Google*, ABC Taiwan Electronics Corp.**)
[Presented by Yimajian Yan (Google)]

Yimajian explained that an inductor is one component of a DC-DC converter. Modeling inductor loss improves the accuracy of a DC-DC converter model. The inductor loss is composed of

copper loss related to DC and AC current, and core loss related to eddy current and hysteresis. Core loss is related to frequency and peak flux density. An improved general form of the Steinmetz equation for core loss was shown. The change in flux density is related to the number of turns in the inductor, the relative permeability of the material, and the change in current through the inductor (ripple current). A final equation for core loss was shown and compared to measurement results. Inductor copper loss was described. The AC resistance will be larger than DC resistance due to skin effect losses. An equation described the AC conductor loss as it related to the ripple current. A final equation for inductor loss was shown, composed of the core loss and AC and DC conductor loss. Inductor vendors should be able to provide 5 of the coefficients in the equation.

Yimajian concluded that when switching frequency increases, core loss decreases, AC copper loss decreases, and the voltage regulator loss increases. In system-level simulation, trade-offs between voltage regulator loss and inductor loss should be considered.

Shuo Wang asked what type of core was being used in this example. Yimajian said a ferrite material known as N7, but he was not sure exactly what the core material was. Shuo asked under what assumptions the conclusion that core loss and AC copper loss decrease with increasing switching frequency was made. Yimajian stated that it was for fixed duty cycle and a fixed input voltage.

Usman Saeed commented that one might want to include radiation losses too, as high frequency content may radiate since the inductor is like a helical antenna. Yimajian noted that there will be some radiation from the L gap, but the fraction is very small and likely not significant in terms of power loss.

CLOSING REMARKS

Mike LaBonte said he was excited about the quality of the presentations. Randy Wolff agreed and noted that it had been a great experience. He said he had enjoyed working with the IEEE-EMC and Zhiping Yang in particular. He thanked everyone for attending and thanked the presenters.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held on September 18, 2020. The following teleconference meeting is tentatively scheduled for October 9, 2020.

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NOTES

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This meeting was conducted in accordance with SAE ITC guidelines.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.

- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	June 26, 2020	July 17, 2020	August 07, 2020	August 28, 2020
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	X	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	-	-	X
Dassault Systemes	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	-
Google	User	Active	X	-	X	X
Huawei Technologies	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Instituto de Telecomunicações	User	Inactive	-	-	-	-
IBM	Producer	Inactive	X	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
Keysight Technologies	User	Active	X	X	X	-
Marvell	Producer	Active	X	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
MST EMC Lab	User	Inactive	-	-	-	X
NXP	Producer	Inactive	-	-	-	X
SerDesDesign.com	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
Synopsys	User	Active	X	X	X	-
Teraspeed Labs	General Interest	Active	X	X	X	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Active	X	X	X	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.