IBIS Model Simulation Accuracy Improvement by Including PSIJ Effect

Yifan Ding*, Yin Sun#, Randy Wolff+, Zhiping Yang^, Chulsoon Hwang*

*Missouri S&T EMC Laboratory, #Zhejiang Lab, +Micron, ^Waymo

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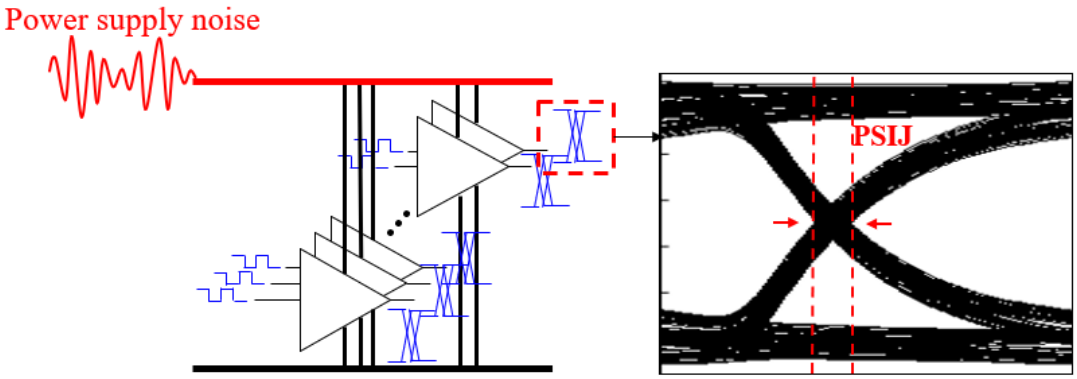
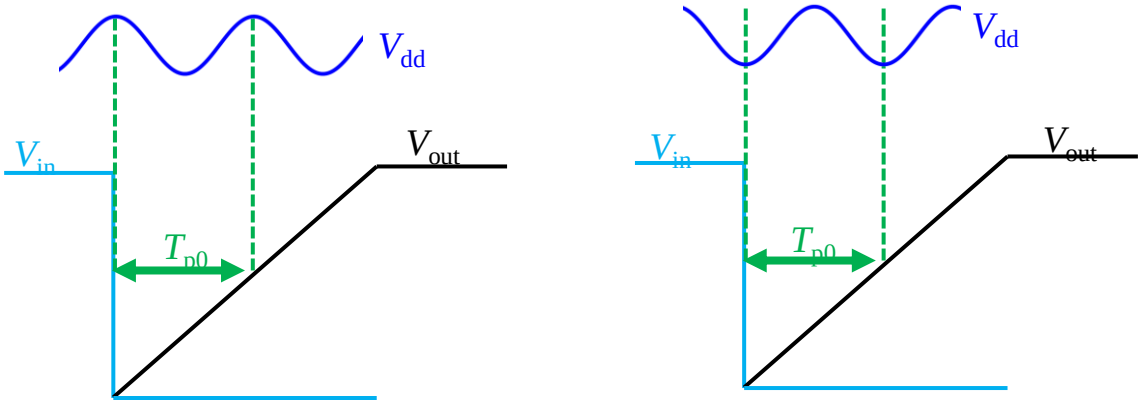
Power Supply Induced Jitter (PSIJ)

Power supply induced jitter (PSIJ):

- The time variation in the output transition edges from ideal positions due to the voltage fluctuations on power rail.



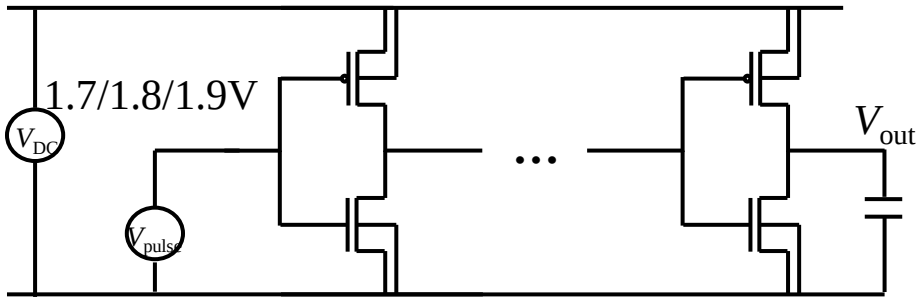
- The Vcc noise can take effect during the propagation delay time range;
- The influence is accumulated, just considering instantaneous voltage value is not accurate.



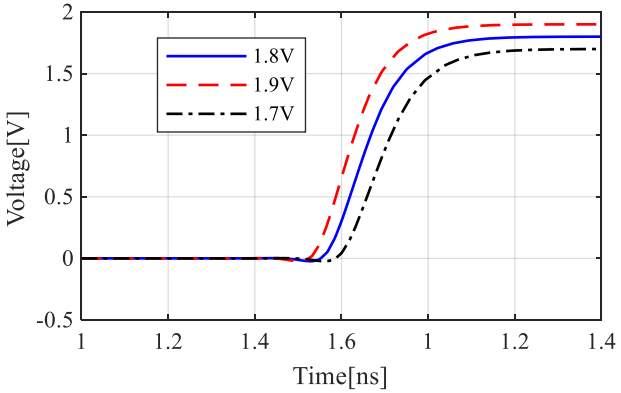
Limitations of the Current Power-Aware IBIS Model

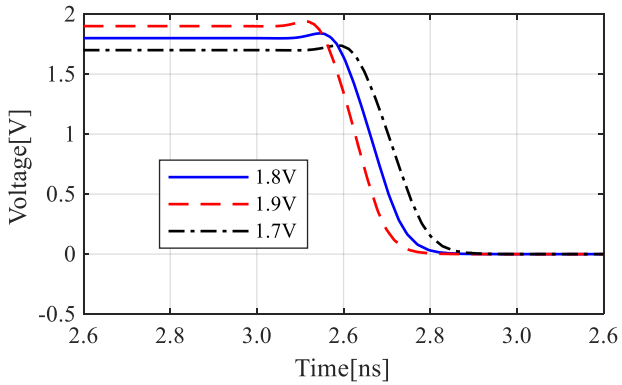
- **<u>Cannot</u>** account for the delay change caused by power noise correctly.

➢ Example: an inverter chain output, change power voltage to 1.7/1.8/1.9V, respectively

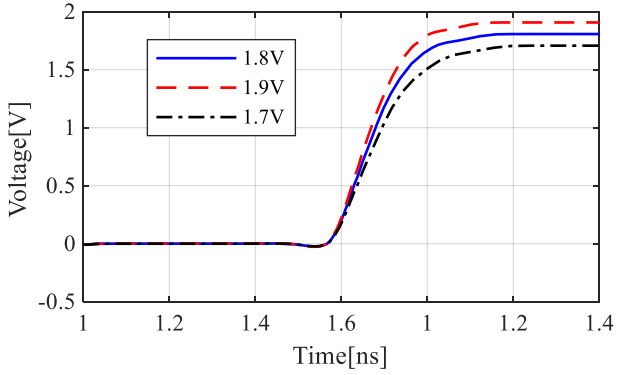


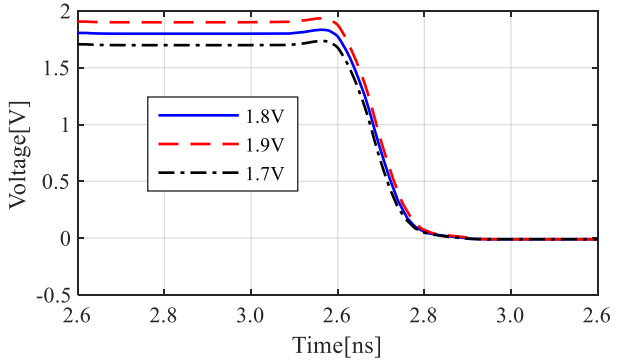
SPICE Results





Power-aware IBIS model Results
(ver5.1,generated with EDA tool)





Limitations of the Current Power-Aware IBIS Model

- Power-aware IBIS model considers gate modulation effect, ratio modification on Ku, Kd based on power rail voltage value

Gate Modulation Coefficients

The ST "Gate Modulation" solution is based on the introduction of two coefficients, one for the Pullup and one for the Pulldown stage, which modulate properly the IBIS standard current (I_IBIS-STD) when a bouncing noise occurs on the power and ground nodes

I(Vgs, Vds) = Kssn(Vgs,Vds)*I(Vgs=VDD,Vds)

Effective SPICE current — IBIS standard current

I_effective = Kssn(Vgs,Vds)*I_IBIS-STD

$$K_d(t)I_{pd} -> K_{sspd}(V_{pd})K_d(t)I_{pd}$$

$$K_u(t)I_{pu} -> K_{sspu}(V_{pu})K_u(t)I_{pu}$$

$$K_{sspd}(V_{pd}) = \frac{V_{pd}}{I_{sspd}(0)}$$

$$K_{sspu}(V_{pu}) = \frac{V_{pu}}{I_{sspu}(0)}$$

Source: "BIRD 98 and ST 'Gate Modulation' Convergence", IBIS Open Forum Teleconference, Jan. 26th, 2007
http://www.ibis.org/docs/BIRD98&ST_Proposal_Convergence.ppt

- The ratio modification Ksspd, Ksspu on Ku, Kd is only a function of V_{pd} (Vcc-Vout) or V_{pu} (Vout-Vgnd), it cannot reflect the effect of power rail voltage noise on switching edge timing change

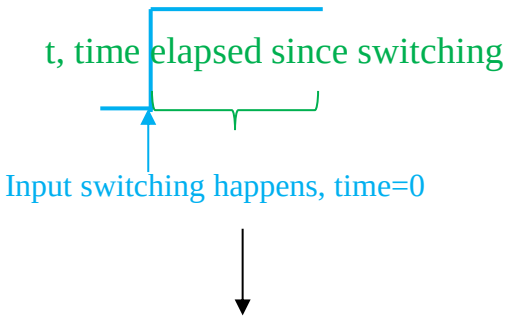
Previous method on modification of Ku, Kd does not consider the time averaged effect;
Source: Behavioral modeling of jitter due to power supply noise for input/output buffers (US Patent 9842177B1)

Previous Proposed Behavior Model

- Modify Ku(t), Kd(t) as a function of **<u>time averaged</u>** power rail voltage Vcc(t); introduce correction coefficient B and A as a function of **<u>time</u>**

$$K_u(t) = K_{u0}(t) + B_u(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_u(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

$$K_d(t) = K_{d0}(t) + B_d(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_d(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$



Ku, Kd under nominal Vcc

Linear fitting coefficient

Quadratic fitting coefficient

Averaged Vcc(t) after the switching event happens;

Achieved by adding delay elements that store

- The time of switching edges
- Time averaged Vcc since switching event happens

- 2 equations, 2 unknowns' algorithm to extract Ku(t), Kd(t) for typ/min/max

$$K_u(t)*I_u(V_1) + K_d(t)*I_d(V_1) = I_{out}(V_1)$$

$$K_u(t)*I_u(V_2) + K_d(t)*I_d(V_2) = I_{out}(V_2)$$

- 2 equations, 2 unknowns' algorithm to extract Bu(t), Au(t) and Bd(t), Ad(t)

$$K_{u\_max}(t) = K_{u0}(t) + B_u(t)(V_{cc\_max} - V_{cc0}) + A_u(t)(V_{cc\_max} - V_{cc0})^2$$

$$K_{u\_min}(t) = K_{u0}(t) + B_u(t)(V_{cc\_min} - V_{cc0}) + A_u(t)(V_{cc\_min} - V_{cc0})^2$$

- Ku/Kd correction coefficients B and A are related to Process, Voltage and Temperature instead of only the supply voltage fluctuation.

Y. Sun and C. Hwang, "Improving Power Supply Induced Jitter Simulation Accuracy for IBIS Model," 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium, 2021, pp. 1127-1132, doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559139.

DC Jitter Sensitivity

- Jitter sensitivity can be applied to calculate the total jitter

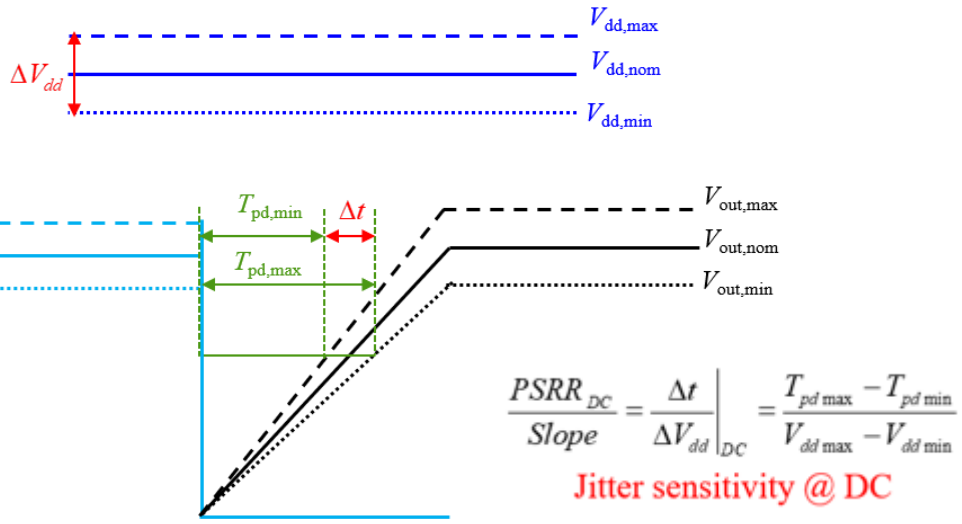
$$\text{Jitter Impact}(f) = \text{Jitter Sensitivity}(f) \cdot V_{noise}(f)$$

$$\text{Jitter Sensitivity}(\omega) = \frac{T_{pd\,\max} - T_{pd\,\min}}{V_{dd\,\max} - V_{dd\,\min}} PSRR'(\omega) e^{j\pi f T_{p0}} \sin c(\pi f T_{p0})$$

*Jitter sensitivity @ DC

Frequency dependency due to time averaged effect (already considered by averaging the Vcc)

Frequency dependency due to PSRR (Power Supply Rejection Ratio)



$$\frac{PSRR_{DC}}{Slope} = \left.\frac{\Delta t}{\Delta V_{dd}}\right|_{DC} = \frac{T_{pd\,\max} - T_{pd\,\min}}{V_{dd\,\max} - V_{dd\,\min}}$$

Jitter sensitivity @ DC

Y. Sun, J. Lee and C. Hwang, "A Generalized Power Supply Induced Jitter Model Based on Power Supply Rejection Ratio Response," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 6, pp. 1052-1060, June 2021, doi: 10.1109/TVLSI.2021.3072799.

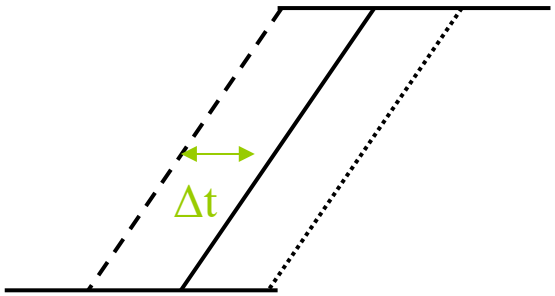
Ku/Kd Modification Based on PSIJ Sensitivity

- Propose to use Jitter sensitivity to do modification

$$Ku/Kd_{max/min}(t) = Ku/Kd_{typ}(t \pm \textbf{DC Jitter sensitivity} \times \Delta Vdd)$$

- Should exclude the original IBIS effect.
- Can include pre-driver PSIJ effect.

Ku for output rising edge:

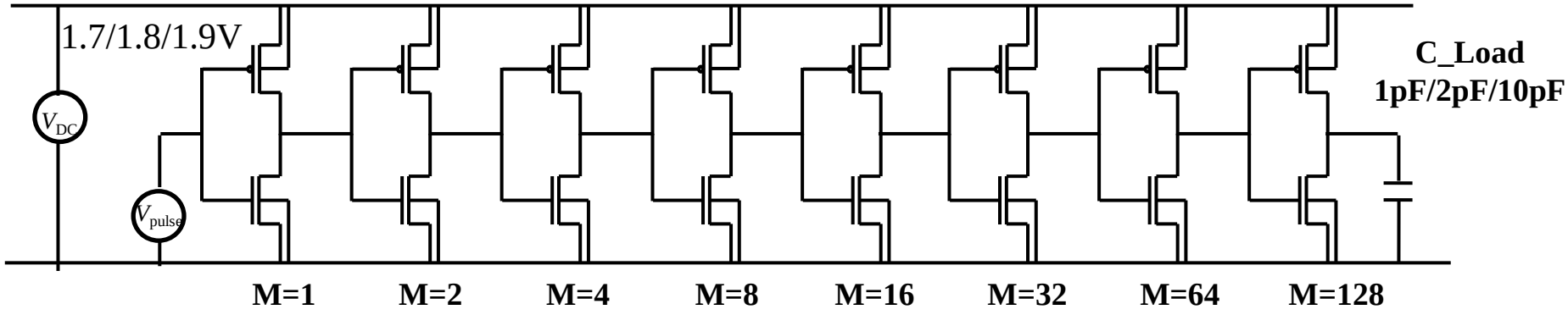


—— typical Ku
------ max Ku
…… min Ku

Δt = (Driver output PSIJ sensitivity – original IBIS PSIJ sensitivity + pre-driver PSIJ sensitivity) * (Vdd_max – Vdd_typ)

Simulation Validation – Inverter Chain

- 8 stage inverter chain with different load capacitance



180nm technology, nominal voltage 1.8V

< All NMOS>
nch_tn
W = 1 um
L = 180 nm

< All PMOS>
pch_tn
W = 2 um
L = 180 nm

Results Comparison – Inverter Chain Output Rising Edge

- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

	PSIJ Sensitivity (ps/V)		
	Load 1pF to V_{SS}	Load 2pF to V_{SS}	Load 10pF to V_{SS}
SPICE	**184.45**	**207**	**350**
Non-Power-aware IBIS	6.5	9.5	39.5
Power-aware IBIS	35.5	54	217
Proposed Algorithm	**187**	**210.5**	**355**

	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	177.95	96.48	197.5	95.41	310.9	88.71
Power-aware IBIS	148.95	80.75	153	73.91	133	38
Proposed Algorithm	**2.55**	**1.38**	**3.5**	**1.69**	**5**	**1.43**

Results Comparison – Inverter Chain Output Falling Edge

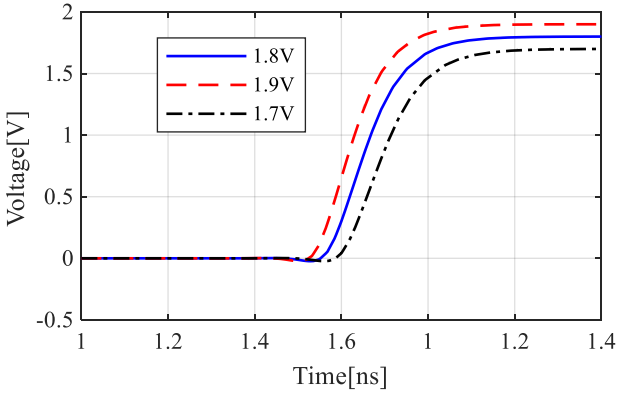
- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

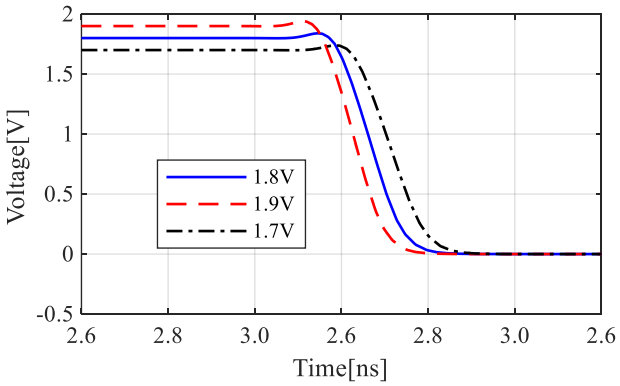
	PSIJ Sensitivity (ps/V)		
	Load 1pF to V_{SS}	Load 2pF to V_{SS}	Load 10pF to V_{SS}
SPICE	**193.91**	**194.16**	**188.71**
Non-Power-aware IBIS	-24.41	-36.07	-123.21
Power-aware IBIS	-25	-35	-135
Proposed Model	**188.95**	**186.75**	**175.85**

	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	218.32	112.59	230.23	118.58	311.92	165.29
Power-aware IBIS	218.91	112.89	229.16	118.03	323.71	171.53
Proposed Model	**4.96**	**2.56**	**7.41**	**3.82**	**12.86**	**6.81**

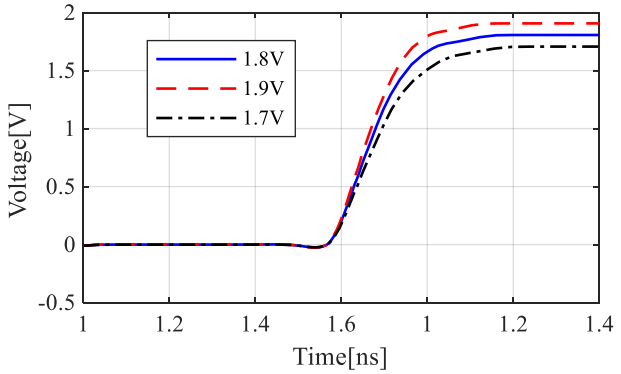
Output Waveform Comparison

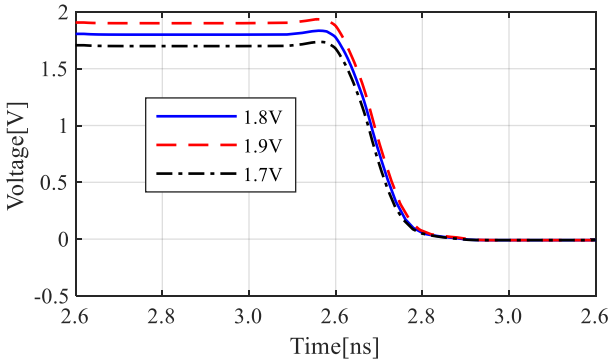
SPICE model



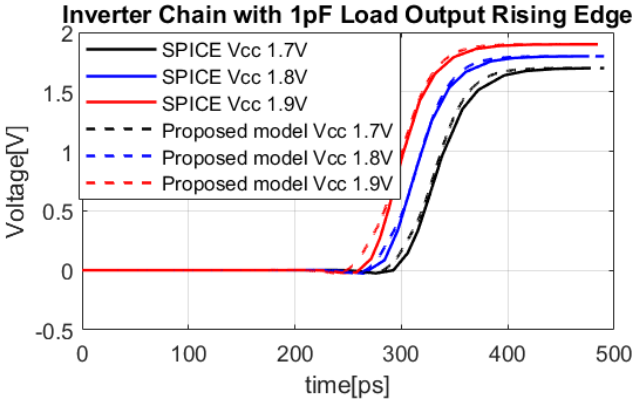


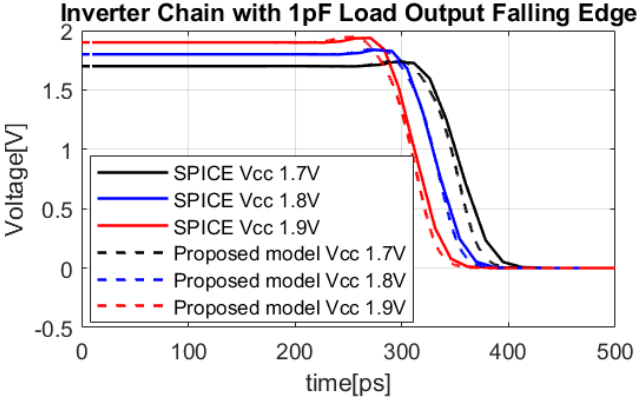
Power-aware IBIS model





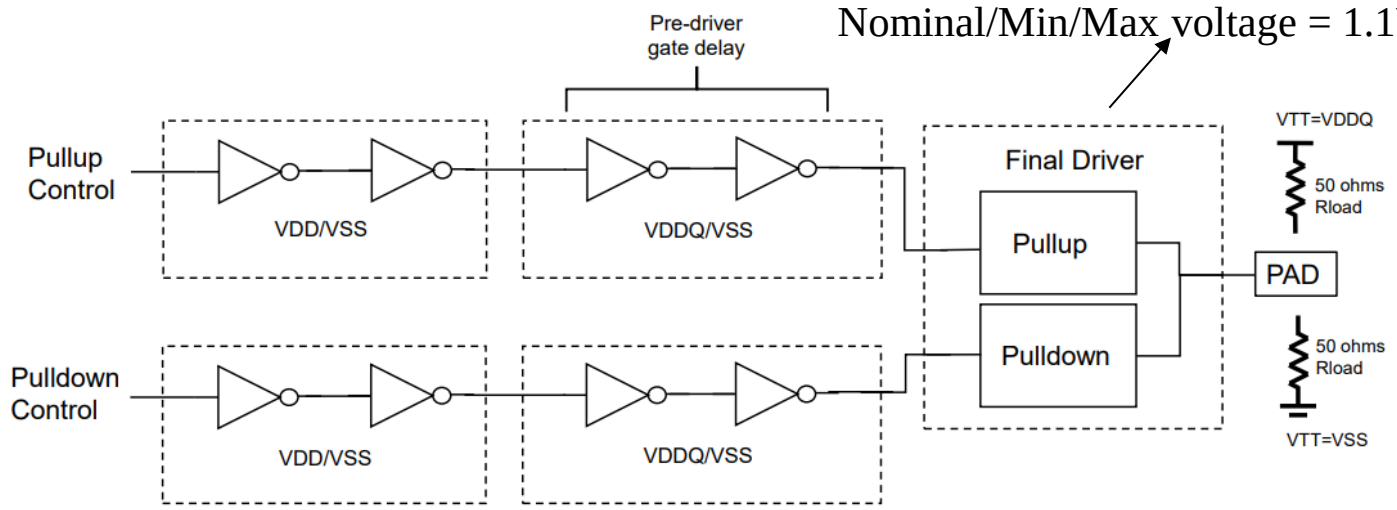
Proposed model compared with SPICE model



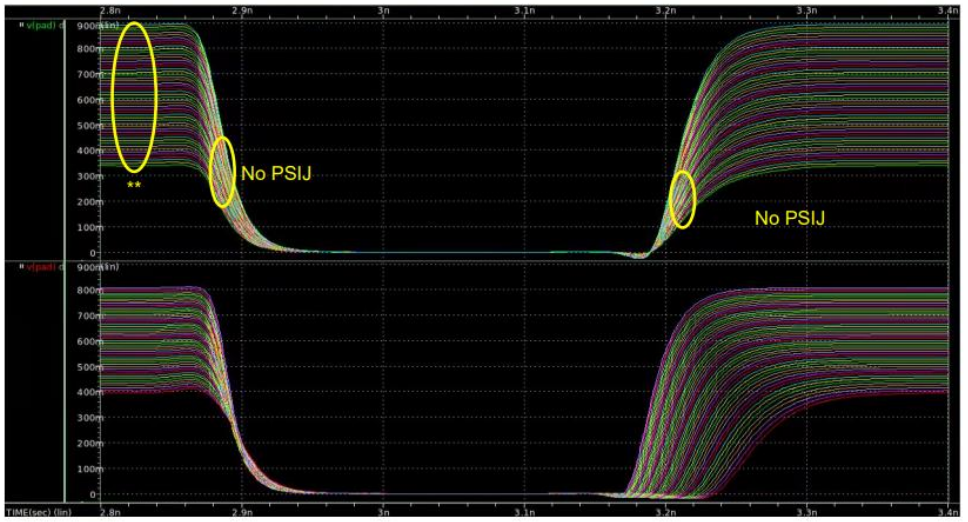


Simulation Validation -- DDRx DQ Tx Buffer

- DDRx DQ Tx Buffer with Pre-driver



IBIS



- VDDQ Sweep 0.85-1.35V
- Typ Corner
- R_Load = 50 ohm
- $V_{TT} = V_{SS}$

SPICE

https://ibis.org/atm_wip/archive/20211026/randywolff/Output%20Buffer%20PSIJ%20Analysis/Micron_PSIJ_Analysis_for_IBIS_ATM.pdf

Pre-driver Included in Model

SPICE transistor level simulation

IBIS behavior model simulation can not simulate with pre-driver

Proposed model simulation

Results Comparison – DDRx DQ Tx Buffer Output Rising

- DDRx DQ Tx Buffer with Pre-Driver
- DC power noise 1.045V/1.1V/1.155V

	PSIJ Sensitivity (ps/V)					
	Load 50 ohm to V_{SS}		Load 50 ohm to V_{DDQ} (variable)		Load 50 ohm to V_{DDQ} (Fixed 1.1V)	
SPICE	**156.65**		**134.17**		**95.45**	
Non-Power-aware IBIS	15.45		38.18		6.36	
Power-aware IBIS	60		45.45		14.55	
Proposed Model	**159.09**		**147.27**		**107.27**	
	Δ (to SPICE)					
	Absolute error (ps/V)	%	Absolute error (ps/V)	%	Absolute error (ps/V)	%
Non-Power-aware IBIS	141.2	90.14	95.99	71.54	89.09	93.34
Power-aware IBIS	96.65	61.70	88.72	66.13	80.9	84.76
Proposed Model	**2.44**	**1.56**	**13.1**	**8.9**	**11.82**	**12.38**

Conclusion

- A behavior model based on driver DC jitter sensitivity is proposed to improve the IBIS simulation accuracy in time domain.
- Time averaged effect on power rail is considered.
- Pre-driver PSIJ effect can be included in IBIS simulation.