IBIS Open Forum Minutes

Meeting Date: August 05, 2022
Meeting Location: Hybrid IBIS Summit at EMC-SI/PI 2022

VOTING MEMBERS AND 2022 PARTICIPANTS

AMD (Xilinx)	Bassam Mansour
Analog Devices (Maxim Integrated)	Tushar Pandey, Jermaine Lim
ANSYS	Curtis Clark
Applied Simulation Technology	Fred Balistreri
Broadcom	Yunong Gan
Cadence Design Systems	Zhen Mu, Jared James, Ken Willis*, Baolong Li*
Celestica	Sophia Feng
Cisco Systems	Stephen Scearce*
Dassault Systemes	Stefan Paret
Google	Hanfeng Wang*, Jianmin Zhang*
Huawei Technologies	Hang (Paul) Yan
Infineon Technologies AG	Christian Sporrer
Instituto de Telecomunicações	Abdelgader Abdalla
Intel Corporation	Hsinho Wu, Michael Mirmak*, Jingbo Li, Liwei Zhao, Chi-te Chen*, Kinger Cai*,
Keysight Technologies	[Radek Biernacki], Ming Yan, Fangyi Rao, Majid Ahadi Dolotsara*, Pegah Alavi, Saish Sawant
Luminous Computing	David Banas
Marvell	Steven Parker
MathWorks	Graham Kus*, Walter Katz, [Mike LaBonte]
Micron Technology	Randy Wolff*, Aniello Viscardi, Justin Butterfield
MST EMC Lab	Chulsoon Hwang*, Hanyu Zhang*, Haran Manoharan*, Jiahuan Huang*, Junho Joo*, Reza Yazdani*, Seunghun Ryu*, Seungtaek Jeong*, Xiangrui Su*, Xu Wang*, Yuanzhuo Liu*, Zhekun Peng*, Yifan Ding*
SerDesDesign.com	John Baprawski
Siemens EDA	Arpad Muranyi*, Weston Beal*, Amin Maher, Scott Wedge, Steve Kaufer, Todd Westerhoff, Vladimir Dmitriev-Zdorov
Synopsys	Ted Mido
Teraspeed Labs	Bob Ross*
Waymo	Zhiping Yang*, Joe Li*
ZTE Corporation	Shunlin Zhu
Zuken	Michael Schäder
Zuken USA	Lance Wang

OTHER PARTICIPANTS IN 2022

Amazon Lab126	Ashkar Hashemi
Altair	Junesang Lee*
Ciena	Hugues Tournier*, Kaisheng Hu*

Cornelis Networks	Champion Kao*
De Montfort University	Alistair Duffy*
GE HealthCare	Balaji Sankarshanan*
	Sarah Salvador*
IBM	Greg Edlund
Imperial College	Cong Ling
Mercury Systems	Vincent Tam
National Central University, Taiwan	Chiu-Chih Chou
NXP Semiconductors	Jon Burnett*
OVT	Sirius Tsang
Rivos	Yansheng Wang*
SAE ITC	José Godoy
SeriaLink Systems	Aleksey Tyshchenko, David Halupka
STMicroelectronics	Olivier Bayet
University of Colorado, Boulder, ECEE	Eric Bogatin
University of Illinois	José Schutt-Aine
University of L'Aquila	Francesco De Paulis*

In the list above, attendees at the meeting are indicated by *. Those submitting an email ballot for their member organization for a scheduled vote are indicated by ^. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS
The connection information for future IBIS teleconferences is as follows:

Microsoft Teams meeting
Join on your computer or mobile app
Click here to join the meeting

Join with a video conferencing device
106010980@teams.bjn.vc
Video Conference ID: 114 666 897 5
Alternate VTC dialing instructions

Or call in (audio only)
+1 267-768-8015,554664847#   United States, Philadelphia
Phone Conference ID: 554 664 847#
Find a local number | Reset PIN
Learn More | Meeting options

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

Randy Wolff declared the start of the IBIS Summit meeting at the IEEE EMC-SI/PI meeting at Spokane Washington on August 8, 2022. Randy announced this is a hybrid meeting with in-person and online attendees. About 46 individuals and 28 organizations attended.
He outlined that the Summit involved presentations, along with time for questions, and then an open discussion period at the conclusion of the presentations.

Note: a summit recording has been uploaded and is available by direct link:
http://www.ibis.org/summits/aug22/summit_recording.mp4

Randy announced the ibis.org web page has a listing of previous IBIS summit minutes.

IBIS CHAIR'S REPORT

Randy Wolff (Micron Technology, USA)
(Chair, IBIS Open Forum)
(Start 00:03:05, Duration 18:00)

Randy Wolff introduced the chairs report and also the list of officers of the IBIS organization. Randy also shared slides on the IBIS Meetings, outlining when meetings are regularly scheduled for each task group, as well as the Open Forum meeting where official voting and planning occurs. Summit meetings such as this are usually held multiple times a year, including at DesignCon in Santa Clara, California, European IBIS Summit with IEEE Workshop on SPI, IEEE Workshop on EMC+SIPI, and Asian IBIS Summits from Japan, Taiwan and China. The parent organization of IBIS is SAE-ITC. He showed a slide detailing the task groups as well.

Randy showed IBIS Milestones since inception in 1993, including work and topics up to the present date. He said the latest IBISCHK parser is version 7.1.0 with a bug fix release 7.1.1 expected in September. He also said IBIS Interconnect Task group in charge of the Touchstone specifications and called for volunteers to join that group if so desired. He announced IBIS Version 7.2 will include BIRD213.1 for PAMn support and BIRD21.4 for major work in flow issues in re-drivers, BIRD219.1, would be the final BIRD for that release.

Future Work:
Randy showed a slide outlining future work, such as equalization with DDR5, clock/data relationships, and a renewed focus on power integrity such as power supply induced jitter modelling, modelling voltage regulators, and other topics. Randy also said the interconnect group has in development a pole-residue format for an upcoming Touchstone format. Also further improvements to IBIS-ISS which started as a donation of syntax from Synopsys HSPICE.

Call for Volunteers:
Randy presented a slide calling for volunteers and outlined which roles are available to make contributions and participate in collaboration, as well as the email reflector and website information. He further announced that presentations are always welcome.

Official Proceedings:
Randy announced the processes to express a technical idea as part of a Task Group, and mentioned that experienced members can assist with formatting and syntax for creating technical proposal documents such as in BIRD format.

Randy presented the website and outlined the available resources provided by the IBIS organization [available at this link: http://Ibis.org/].

IBIS-ATM TASK GROUP REPORT
Arpad Muranyi (Siemens EDA, USA)
(Start 00:21:50, Duration 12:15)

Arpad Muranyi reported that due to Covid [and associated public/group event shutdowns] he has not presented slides on this topic since the IBIS Summit during DesignCon 2020. He proceeded to report that progress since DesignCon 2020 includes IBIS v7.1, along with a slide showing the approved and rejected BIRDs involved in that release. He specifically mentioned the clocked RX models, which involve clock-forwarding, and BIRD217 clarifies that Clocked RX models must return clock times. Also called out that BIRD218 Designator Pin List Relaxation can help simplify pin listings and reduce file size. He went into detail about the BIRDs and why some were approved and others were rejected.

Pending BIRDs:
Arpad presented a slide on the pending BIRDs and discussion topics. These included the following:
- Standard Power Integrity Model (SPIM) in IBIS
- Power Supply Induced Jitter (PSIJ) study
- VRM, diode and inductor modeling
- Multi-level analog buffer modelling (PAMn, C-phy, etc.)

Task group material can be found at:
> http://www.Ibis.org/macromodel_wip/

PRESENTATIONS

EXPANDING IBIS FOR POWER INTEGRITY

Zhiping Yang*, Aaron Xu**, Hanfeng Wang**, Chulsoon Hwang***, Songping Wu****, Yansheng Wang****, Kinger Cai*****, Chi-te Chen*****
(Waymo*, USA; Google**, USA; Missouri University of Science and Technology***, USA; Rivos****, USA; Intel Corp.*****, USA)
[Presented by Hanfeng Wang (Google, USA)]
(Start 00:35:05, Duration 26:10)

Synopsis: Objective is to expand the IBIS simulation capabilities on power integrity, power consumption, and SI/PI co-simulations.

Q&A session: Arpad Muranyi asked if Verilog or other existing features could be leveraged to avoid inventing new keywords. He commented that if you look at external keywords, the guts of a model can be replaced by Verilog-A model syntax. Hanfeng replied that is good information. Randy Wolff asked if we have a model type that allows modelling of these devices now, or if it does not fit in the model types that we have currently. Hanfeng replied he was no sure. Discussion occurred on how to standardize things such as passive components and also how to classify controllers perhaps as a component so that the differences can be accommodated.

Ken Willis commented that he and colleagues have used Verilog-A for transient simulations with power integrity- external models is very powerful and underused in IBIS- even just straight up SPICE and external models in SPICE as well. Maybe SPICE context.
Arpad asked would VRM and power integrity be two different simulations- how to do resolution of time steps considering bandwidth of kilo-Hertz vs. giga-Hertz? Hanfeng replied that on the die, they would have very low frequency loads. But out in the bus / memory interface, they care about giga-Hertz. It can take overnight or perhaps days to model. This motivates a behavioral model. He said they do actually these simulations every day, with core power supplies- and not only consider high frequency components, but also take into account the loop response- sometimes this can be the dominant effect in the Voltage-droop analysis.

SPIM (STANDARD PI MODEL) IN IBIS
Kinger Cai, Chi-te Chen (Intel Corp., USA)
[Presented by Kinger Cai (Intel Corp., USA)]
(Start 01:01:55, Duration 51:00)

Synopsis: Presentation agenda as follows:
- Industry Platform PI Design Challenges
- Platform PI design Architecture Standardization
  - SPIM – Standard Power Integrity Model
  - SPIM stimulus and target definition
  - FASTPI – Platform PI design Framework
- Keywords definition for .spim filein BIRD
- One example .spim file
- FastPI Roadmap
- Next Steps

Q&A session:
Kinger commented: "Why we started:" recently we went through first wave of supply chain shortage- we could specify certain caps and value and size- could not find caps for the PDG, and customers could not either. The challenge arose, how to change reference design to show other caps that are allowed? With this fast PI, we could. So if the customer impedance met our targets, we could sign off on their alternatives. This will also help VRM designers to create products that can drive our CPUs. A BIRD for SPIM will be submitted in IBIS Open Forum.

Questioner: how does CPM model relate to this?
Kinger: this is more represented on-die level and package design. This has more focus on-die, Some of our vendors tape out a board every week. They need to quickly sign off. CPM can allow competitors to guess chip architecture by looking at the details of a CPM model. Yes, CPM is comparable to this. CPM can behave like a SPICE model. This would protect the IP, and this would be more general. CPM is like SPICE, you can [implement many topologies] but it exposes details. SPIM would require a cookbook update for IBIS, and this is planned.

BREAK

(10 Minutes)

IBIS MODEL SIMULATION ACCURACY IMPROVEMENT BY INCLUDING PSIJ
Yifan Ding*, Yin Sun**, Randy Wolff***, Zhiping Yang****, Chulsoon Hwang* (Missouri University of Science and Technology*, USA; Zhejiang Lab**, PRC; Micron Technology***, USA; Waymo****, USA)
[Presented by Yifan Ding (Missouri S&T, USA)]
(Start 01:54:00, Duration 27:50)

Synopsis: Presentation agenda as follows:
- Introduction
  - Account for Power Supply induced jitter
  - Limitation of the current power-aware IBIS Model
- Jitter Sensitivity Based Modification
  - Ku/Kd Modification Based on PSIJ Sensitivity
- Simulation Validation
  - 8 Stage Inverter Chain with Different Loads
  - DDRx DQ Tx Bufffer with Pre-driver with Different Terminals
- Conclusion

Q&A session:
Yifan commented that the present model of current model in IBIS is not able to model delay difference caused by voltage difference.
Bob Ross asked if this is proposing any new key words? Yifan responded, yes it would be PSIJ keyword or PSI_Sensitivity.

Randy Wolff commented, excluding the IBIS effect- on slide 8- if you change the voltage and measure the timing, you will get a how much the final driver is moving, slew rates may change, you can also see the effect on the pre-driver which moved the timing. But then if you take an IBIS model and simulate it, you will see the final driver jitter… and we only want the pre-driver jitter- the pre-driver sensitivity. You kind of have to do two measurements- one with SPICE, and one with IBIS, and if you take the difference, you get the pre-driver only, by itself. That is what this is trying to do, to show the timing difference and not to model the final driver.

Randy mentioned that the IBIS model used in this study was provided by Micron.
Randy clarified that a BIRD would have to be written for this and any keywords.
Michael Mirmak commented: the keyword would have to be defined, and how to extract it would be helpful. Randy said the ISSO pull up and pull down tables or something similar would help- might be a 2 step process to find the PSIJ value, and it is not trivial.

[PSIJ SENSITIVITY] IN IBIS
Kinger Cai, Fern Nee Tan, Chi-te Chen (Intel Corp., USA)
[Presented by Kinger Cai (Intel Corp., USA)]
(Start 02:22:15, Duration 36:10)

Synopsis: Presentation agenda as follows:
- Background
- HSIO architecture: Serial & Parallel
- Status Quo, for jitter analysis
- New system jitter analysis methodology
- [PSIJ Sensitivity] in IBIS
- [PSIJ Sensitivity] application
- Next Steps

Q&A session:
Arpad Muranyi asked if simulations could be run in order to proof of concept. Kinger replied to show some behavior curves, where it was evaluated theoretically.
General/group discussion held about creating a new task group for Power modelling, power integrity and related concerns.
Randy Wolff concluded the discussion stating that this could be discussed in the ATM group in more detail.

K.T. WANG (WANG ALGEBRA) - UPDATED EXPANDED HISTORY
Bob Ross*, Cong Ling** (Teraspeed Labs*, USA; Imperial College**, UK)
[Presented by Bob Ross (Teraspeed Labs, USA)]
(Start 02:59:35, Duration 29:00)

Synopsis: Presentation agenda as follows:
- Wang Algebra
- T-coils
- Wang's Biography
- References

Q&A session:
Bob Ross commented: Wang Algebra is useful for nodal analysis. If poles are spaced 30 degrees you get 0.40% aberrations and a factor of about 2.x bandwidth improvement. Wang Algebra works for small circuits. The IBIS package of L's and C's, the diagonal is composed of at least off-diagonal components. The use of this method is exactly the same result at the end. The simplifications are mathematically valid, there are no loss of accuracy. The full equations could be expressed but it is easier to express them as parametric equations. The constant resistance constraint variables are solved and then they are used to simplify parameters in other equations. The derivations are not shown here.

OPEN DISCUSSION AND CLOSING REMARKS
(Start 03:28:45, Duration 13:50)

A question was asked, whether connector vendors could be interested in adopting some of the IBIS standards regarding connectors. Michael Mirmak responded that it used to be covered by the task group ICI, but was overtaken by some other standards, such as IEEE 370, some of which is being fed back into Touchstone right now.

Randy Wolff thanked presenters and sponsors. He encouraged people to volunteer to help in the work of advancing the IBIS specification. He also hoped to see everyone in person in a future summit.

NEXT MEETING
The next IBIS Open Forum teleconference meeting would be held on August 12, 2022. The following IBIS Open Forum teleconference meeting was tentatively scheduled for September 9, 2022.

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NOTES

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This meeting was conducted in accordance with SAE ITC guidelines.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to or unsubscribe from the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org):
    - https://www.freelists.org/list/ibis
    - https://www.freelists.org/list/ibis-users
- To subscribe to or unsubscribe from one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, ibis-editorial@freelists.org, or ibis-quality@freelists.org:
    - https://www.freelists.org/list/ibis-macro
    - https://www.freelists.org/list/ibis-interconn
    - https://www.freelists.org/list/ibis-editorial
    - https://www.freelists.org/list/ibis-quality
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS (attendance X absent -)

Organization	Interest Category	Standards Ballot Voting Status	May 26, 2022	June 3, 2022	June 24, 2022	July 22, 2022	August 5, 2022
AMD (Xilinx)	Producer	Inactive	-	-	-	-	-
Analog Devices (Maxim Integrated)	Producer	Inactive	X	-	-	-	-
ANSYS	User	Active	-	X	X	X	-
Applied Simulation Technology	User	Inactive	-	-	-	-	-
Broadcom Ltd.	Producer	Inactive	X	-	-	-	-
Cadence Design Systems	User	Inactive	-	X	-	-	X
Celestica	User	Inactive	-	-	-	-	-
Cisco Systems	User	Inactive	-	-	-	-	X
Dassault Systemes	User	Inactive	X	-	-	-	-
Google	User	Inactive	-	-	-	-	X
Huawei Technologies	Producer	Inactive	-	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-	-
Instituto de Telecomunicações	User	Inactive	-	-	-	-	-
Intel Corp.	Producer	Active	-		=	X	X
Keysight Technologies	User	Active	-	X	-	X	X
Luminous Computing	General Interest	Inactive	-	-	-	-	-
Marvell	Producer	Active	-	X	X	-	-
MathWorks	User	Active	-	X	X	X	X
Micron Technology	Producer	Active	X	X	-	X	X
MST EMC Lab	User	Inactive	-	-	-	-	X
SerDesDesign.com	User	Inactive	-	-	-	-	-
Siemens EDA (Mentor)	User	Active	X	X	X	X	X
STMicroelectronics	Producer	Inactive	-	-	=	=	=
Synopsys	User	Active	-	X	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X	X
Waymo	User	Active	-	X	X	X	X
ZTE Corp.	User	Inactive	-	-	-	-	-
Zuken	User	Active	X	X	X	X	X

= Temporarily not a voting member

Criteria for SAE member in good standing:
- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings (voting by email counts as attendance)

Interest categories associated with SAE standards ballot voting are:
- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations, and associations, and/or consumers.