# How to Make Good EMD Models 

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## Outline

General Overview
The anatomy of EMD files
What do we need to make an EMD file?
Notes on power-aware modeling
The S-parameter reference terminal problem Illustrations

## General Overview

- The IBIS v7.1 specification introduced a major improvement for multi-die package and multi-chip module modeling
- The new capability is known as Electrical Module Description (EMD) modeling which was proposed in BIRD202.3
- https://www.ibis.org/birds/bird202.3.docx
- EMD is functionally very similar to EBD in the IBIS specification, with significant improvements
- Supports SPICE subcircuits and Touchstone files (with or without coupling)
- Supports signal only, power delivery only, or combined signal and power delivery modeling
- EMD can be used to model the "package" of stacked-die or multi-chip devices as well as the PCB of DIMM modules and other plug-in boards
- EMD models can be nested (i.e., reference other EMD models)
- Up to six levels of hierarchy for nested .emd files are supported


## The anatomy of EMD files

- The header section
- [IBIS Ver], [File Name], [File Rev], [Date] , [Source], [Disclaimer], [Copyright], [Notes]
- [Begin EMD] / [End EMD]
- [Manufacturer], [Description], [Number Of EMD Pins], [EMD Pin List], [EMD Parts], [EMD Designator List], [Designator Pin List], [Voltage List], [EMD Group]
- [EMD Set] / [End EMD Set]
- [Manufacturer], [Description]
- [EMD Model]


## EMD Model

- Contains a pointer to a Touchstone or IBIS-ISS (SPICE subcircuit) file
- Contains as many "terminal lines" as the number of ports ( +1 ) or subcircuit terminals
- Unused ports for Touchstone files are supported with three pre-defined automatic termination options
- The terminal lines define the type of the port or terminal (signal or power rail) and what they are connected to (EMD pin or Designator pin)
- These connection definitions can use signal names or bus label names to make connections to groups of pins


## What do we need to make an EMD file?

- One or more Touchstone or IBIS-ISS (SPICE subcircuit) files
- These files contain the interconnect models which connect the EMD pins with the "Designator Pins", i.e., the pins of the IBIS files
- They may contain signals only, power delivery network (PDN) only, or both
- One or more IBIS files
- These files contain the buffer models
- They may be bare-die models (e.g., for MCMs) or packaged models (e.g., for DIMMs)
- Pin list and signal names for the EMD model
- These are the pins which connect the EMD model with the outside world
- These pin names and signal names should match the corresponding names in the data sheet
- The EMD signal names do not need to match with the signal names inside the IBIS file
- Information about what the Touchstone ports or SPICE terminals are connected to
- Connections can only be made to EMD pins or Designator pins


## Notes on power aware modeling

- A power-aware IBIS model must contain the following keywords
- [ISSO PU], [ISSO PD], [Composite Current] (in the scope of a [Model] keyword)
- [Pin Mapping] (in the scope of a [Component] keyword)
- If the EMD file contains non-power-aware IBIS model(s)
- It is useless to include PDN models in the EMD file
- It is not prohibited, but doesn't do any good
- Simulators will most likely power the buffer models with ideal sources
- If the EMD file contains power-aware IBIS model(s)
- All power and ground pins should be included in [EMD Pin List]
- All power and ground pins should be included in [Designator Pin List]
- Connectivity between all power and ground pins should be defined in [EMD Model]
- This may be done using individual pin names, signal names, or bus label names
- Try not to use A_gnd (the IBIS equivalent of the SPICE node 0) for ground connections


## The Touchstone reference terminal problem

Consider two cascaded 2-port Touchstone models

- $I_{1}=I_{2}$
- From "port regularity" $l_{1}=I_{1}$ and $l_{2}=I_{2}$
- Consequently $l_{1}=l_{2}$, and
- $\mathrm{I}_{\text {gnd }}=0$
- Hence adding a connection to ground doesn't change the port voltages and currents, it may only affect their absolute potential


## https://www.ibis.org/summits/feb18/dmitriev-zdorov.pdf (slide 8)



## The Touchstone reference terminal problem (cont'd)

## Now consider a simple 2-port Touchstone PDN model for a motherboard (.s2p)

- One of the ports is connected to the voltage regulator (VRM)
- The other port is connected to the integrated circuit (IBIS buffer)
- The S-parameter model describes the full PDN loop, i.e., includes the power and ground planes
- Since the IBIS buffer is a 3-terminal device, $\mathrm{I}_{2} \neq \mathrm{I}_{2}$, consequently $\mathrm{I}_{\text {gnd }} \neq 0$
$>$ When the buffer is driving 'high': $I_{\text {gnd }}=I_{1}=I_{1}=I_{2}=I_{\mathrm{Vtt}}$ and $I_{2}=0$
$>$ When the buffer is driving 'low': $I_{1}=I_{1}=I_{2}=0$ and $I_{2}=I_{\mathrm{gnd}}=I_{\mathrm{Vtt}}$
- This violates the fundamentals of S-parameters
- The PDN model will have no effect on the signal when driving low and will have "double" the effect when driving high (because it includes both the power and ground planes)



## Double-counted path

- When "Ground" net is used as the negative terminal, its effect on the circuit is pushed to the positive terminal

- S matrices are the same in these 3 cases
- Impedance, and hence voltage, between negative terminals of the 2 ports is not equal
- Impedance between positive terminals of



## More on referencing in EMD files

- When using power-aware IBIS model(s) with one or more PDN models, all of the power and ground pins of the IBIS model(s) must be properly connected
- It is also important to include all of the power and ground pins of the EMD model in the [EMD Pin List] keyword and connect them to the corresponding ports of the PDN model(s)
- How should the S-parameter reference terminals be connected?
- Note: The EMD specification only supports a single reference terminal ( $\mathrm{N}+1$ ) for Touchstone models


## S-parameter examples

- The next two examples illustrate common mistakes which result in bad EMD files
- The $3^{\text {rd }}$ example illustrates an acceptable (but not the best) way to define ground connections
- The $4^{\text {th }}$ example illustrates the best way to define the ground connections
- Note: In these examples the S-parameter model does not include explicit ports for the ground plane(s) of the PCB
- The $5^{\text {th }}$ example might be the most ideal method because it has explicit ports for the ground net


## Example 1 - Missing ground pin connections on both sides of the Touchstone model (wrong)

| PORT 1 | (PIN U1.R94, A0, S) |
| :--- | :--- |
| PORT 2 | (PIN U2.R94, A0, S) |
| PORT 3 | (PIN U3.R94, A0, S) |
| PORT 4 | (PIN U4.L94, A0, S) |
| PORT 5 | (PIN U5.L94, A0, S) |
| PORT 6 | (PIN BGA.K2, A0, S) |
|  |  |
| PORT 7 | (PIN U1.R95, A1, S) |
| PORT 8 | (PIN U2.R95, A1, S) |
| PORT 9 | (PIN U3.R95, A1, S) |
| PORT 10 | (PIN U4.L95, A1, S) |
| PORT 11 | (PIN U5.L95, A1, S) |
| PORT 12 | (PIN BGA.J2, A1, S) |
|  |  |
| PORT 163 | (GROUP:VDD.U1, VDD, P) |
| PORT 164 | (GROUP:VDD.U2, VDD, P) |
| PORT 165 | (GROUP:VDD.U3, VDD, P) |
| PORT 166 | (GROUP:VDD.U4, VDD, P) |
| PORT 167 | (GROUP:VDD.U5, VDD, P) |
| PORT 168 | (GROUP:VDD.BGA, VDD, P) |
| PORT 169 | (GROUP:VTT.BGA, VTT, P) |


| GROU | PORT | 163 | NAME:VDD.U1, | U1.L4, | U1.L8, | 17, | 20, | U1.L33, | U1.L36, | U1.L40, | U1.L45, | 49, | U1.L52, |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GROU | PORT | 164 | NAME:VDD.U2, | U2.L4, | U2.L8, | U2.L17, | U2.L20, | U2.L33, | U2.L36, | U2.L40, | U2.L45, | U2.L49, | U2.L52, |  |
| GROU | PORT | 165 | NAME:VDD.U3, | U3.L4, | U3.L8, | U3.L17, | U3.L20, | U3.L33, | U3.L36, | U3.L40, | U3.L45, | U3.L49, | U3.L52, |  |
| GROU | PORT | 166 | NAME:VDD.U4, | U4.L1, | U4.L13, | U4.L16, | U4.L25, | U4.L30, | U4.L48, | U4.R4, | U4.R8, | U4.R17, | U4.R20, |  |
| GROU | PORT | 167 | NAME:VDD.U5, | U5.L1, | U5.L13, | U5.L16, | U5.L25, | U5.L30, | U5.L48 | U5.R4, | U5.R8, | U5.R17, | U5.R20, |  |
| GRO | PORT | 168 | NAME:VDD. BGA, | BGA.A | BGA. A | BGA.A7, | BGA. AB | GA. AB | GA. A | GA. AB | BGA. AC | BGA. B1 | BGA.B5, |  |
| GRO | PORT | 69 | AM | B | BGA | G | BG | BGA. ABI | BG | BGA | BGA.AB4 |  | BGA |  |

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Example 1 - Missing ground pin connections on both sides of the Touchstone model (wrong)


## Example 2 - Missing ground pin connections on the IBIS side (wrong)

```
\begin{tabular}{|c|c|c|}
\hline PORT 1 & (PIN U1.R94, A0, S) & \\
\hline PORT 2 & (PIN U2.R94, A0, S) & \\
\hline PORT 3 & (PIN U3.R94, A0, S) & \\
\hline PORT 4 & (PIN U4.L94, A0, S) & \\
\hline PORT 5 & (PIN U5.L94, A0, S) & \\
\hline PORT 6 & (PIN BGA.K2, A0, S) & - (GROUP: GND. BGA, GND, P) \\
\hline PORT 7 & (PIN U1.R95, A1, S) & \\
\hline PORT 8 & (PIN U2.R95, A1, S) & \\
\hline PORT 9 & (PIN U3.R95, A1, S) & \\
\hline PORT 10 & (PIN U4.L95, A1, S) & \\
\hline PORT 11 & (PIN U5.L95, A1, S) & \\
\hline PORT 12 & (PIN BGA.J2, A1, S) & - (GROUP: GND.BGA, GND, P) \\
\hline PORT 163 & (GROUP:VDD.U1, VDD, P) & \\
\hline PORT 164 & (GROUP:VDD.U2, VDD, P) & \\
\hline PORT 165 & (GROUP:VDD.U3, VDD, P) & \\
\hline PORT 166 & (GROUP:VDD.U4, VDD, P) & \\
\hline PORT 167 & (GROUP:VDD.U5, VDD, P) & \\
\hline PORT 168 & (GROUP:VDD.BGA, VDD, P) & - (GROUP: GND.BGA, GND, P) \\
\hline PORT 169 & (GROUP:VTT.BGA, VTT, P) & - (GROUP: GND.BGA, GND, P) \\
\hline
\end{tabular}
```



```
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline & PORT & & DD.U1, & U1.L4, & 1.L8, & 1.L17, & U1.L20, & U1.L33, & U1.L36, & 40, & 45, & U1.L49, & U1.L52, & U1. & 1. \({ }^{\text {a }}\), \\
\hline GROUP & PO & 164 & NAME:VDD. U2, & U2.L4, & U2.L8, & U2.L17, & U2.L20, & U2.L33, & U2.L36, & U2.L40, & U2.L45, & U2.L49, & U2.L52, & U2.L57 & U2.L62, \\
\hline ROUP & PORT & 165 & NAME:VDD.U3, & U3.L4, & U3 & U3.L17, & U3.L20, & U3.L33, & U3.L36 & U3.L40, & U3.L45, & U3.L49, & U3.L52, & U3.L57, & U3.L62, \\
\hline GROUP & PORT & 166 & NAME:VDD.U4, & U4.L1, & U4.L13, & U4.L16, & U4.L25, & U4.L30, & U4.L48, & U4.R4, & U4.R8, & U4.R17, & U4.R20, & U4.R33, & U4.R36, \\
\hline ROUP & PORT & 67 & NAME:VDD.U5, & U5.L1, & U5.L13, & U5.L16, & U5.L25, & U5.L30, & U5.L48, & U5 & U5.R8, & U5.R17, & U5.R20, & U5.R33 & U5.R36 \\
\hline GROUP & PORT & 168 & NAME:VDD.BGA, & BGA. A3, & BGA.A4, & BGA.A7, & BGA.AB5, & BGA.AB9, & BGA.AB11, & BGA.AB13, & BGA. AC7, & BGA.B1, & BGA. B5, & BGA.B9, & BGA.B11, \\
\hline GROUP & PORT & 168 & NAME:GND.BGA, & BGA.A5, & BGA.A9, & BGA.A1 & GA.A14, & GA.AA5, & GA.AA13, & BGA.AC5, & BGA.AC9, & 3GA.AC11, & BGA. AC14, & BGA.B2, & BGA.C1, \\
\hline GROUP & PORT & 169 & NAM & A1 & 2 & BGA. AA3, & BGA.AA4, & BGA. AB1, & GA.AB2, & BGA. AB3, & BGA. AB4, & GA. AC2, & BGA. AC3, & BGA. AC4 & \\
\hline GROUP & PORT & 169 & NAME: GND.BGA, & BGA.A5, & BGA.A9, & BGA. A11, & GA.A14, & BGA. AA5, & BGA.AA13, & BGA.AC5, & GA. AC9, & BGA. AC11, & BGA.AC14, & BGA.B2, & BGA. C1 \\
\hline
\end{tabular}
```


## Example 2 - Missing ground pin connections on the IBIS side (wrong)



## Example 3 - Missing ground pins on the EMD side with grounded IBIS side (better)

| PORT | (PIN U1.R94, A0, S) | - (GROUP: GND.U1, | GND, P) |
| :---: | :---: | :---: | :---: |
| PORT 2 | (PIN U2.R94, A0, S) | - (GROUP: GND.U2, | GND, P) |
| PORT | (PIN U3.R94, A0, S) | - (GROUP:GND.U3, | GND, P) |
| PORT | (PIN U4.L94, A0, S) | - (GROUP: GND.U4, | GND, P) |
| PORT | (PIN U5.L94, A0, S) | - (GROUP:GND.U5, | GND, P) |
| PORT 6 | (PIN BGA.K2, A0, S) |  |  |
| PORT 7 | (PIN U1.R95, A1, S) | - (GROUP: GND.U1, | GND, P) |
| PORT 8 | (PIN U2.R95, A1, S) | - (GROUP: GND.U2, | GND, P) |
| PORT 9 | (PIN U3.R95, A1, S) | - (GROUP: GND.U3, | GND, P) |
| PORT 10 | (PIN U4.L95, A1, S) | - (GROUP:GND.U4, | GND, P) |
| PORT 11 | (PIN U5.L95, A1, S) | - (GROUP: GND.U5, | GND, P) |
| PORT 12 | (PIN BGA.J2, A1, S) |  |  |
| PORT 163 | (GROUP:VDD.U1, VDD, P) | - (GROUP: GND.U1, | GND, P) |
| PORT 164 | (GROUP:VDD.U2, VDD, P) | - (GROUP:GND.U2, | GND, P) |
| PORT 165 | (GROUP:VDD.U3, VDD, P) | - (GROUP:GND.U3, | GND, P) |
| PORT 166 | (GROUP:VDD.U4, VDD, P) | - (GROUP:GND.U4, | GND, P) |
| PORT 167 | (GROUP:VDD.U5, VDD, P) | - (GROUP:GND.U5, | GND, P) |
| PORT 168 | (GROUP:VDD.BGA, VDD, P) |  |  |
| PORT 169 | (GROUP:Vtt. BGA, VTt, P) |  |  |


|  | PORT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GROUP | PORT | 2 | NAME:GND.U2 | U2.L2, | U2.L11, | U2.L15 | U2.L2 | U2.L38 | U2.L42, | U2.L43, | U2 | U2.L50, | U2 | U2.L55, | U2.L59 | U2.L60 | U2.L64 | U2.L66, | U2.L69, | , U2.L72, | , U2.L90 | U2 |
| GROUP | PORT | 3 | NAM | U3.L2, | U3.L11, | U3.L15, | U3 | U3.L | U3.L4 | U3 | U3.L47, | U3.L50, | U3.L54 | U3.L55, | U3.L59, | U3.L60, | , U3.L64 | U3.L66, | U3.L69, | , U3.L72, | , U3.L90 | U3.L106 |
| GROUP | PORT | 4 | NAI | U4.L6 | 4.L10, | U4.L18 | 4.L2 | U4.L2 | U4.L2 | L3 | U4.L34 | U4.R2, | 4.R11 | U4.R15, | U4.R23, | U4.R38 | U4.R42 | U4.R43 | U4.R47, | , U4.R50 | U4.R | U4.R55, |
| GROUP | PORT | 5 | NAM | U5.L6 | U5.L10, | U5.L18 | U5.L22 | U5.L27 | U5.L28 | U5.L32 | U5.L34, | U5.R2, | U5.R11 | U5.R15 | U5.R23, | U5.R38 | U5.R42 | U5.R43 | U5.R47, | U5.R50 | U5.R54 | U5 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| GROU | POR |  |  |  |  | U1.L15 | 1. 12 | 1.L3 | . |  |  | 1.L50 | U1.L5 |  | U1.L59, | 1. | U1. | , U1.L66, | 69, |  |  |  |
| GROUP | PO | 8 | NAM | U2.L2 | 2.L11 | U2.L15 | 2.L2 | U2.L38 | U2.L42 | U2.L43, | U2.L47 | U2.L50 | U2.L54, | U2.L55, | U2.L59, | J2.L60 | U2.L64 | U2.L6 | U2.L69, | , U2.L7 | , U2.L90, | U2.L106 |
| GROUP | POR | 9 | NAME: GND.U3 | U3.L2 | U3.L11, | U3.L15, | U3.L23 | U3.L38 | U3.L42 | U3.L43 | U3.L47 | U3.L50 | U3.L54 | U3.L55, | U3.L59, | U3.L60, | , U3.L64 | U3.L66 | U3.L69, | , U3.L72, | U3. | U3.L106 |
| GROUP | PO | 10 | NAME | U4.L6, | U4.L10, | U4.L18, | L22 | U4.L27, | U4.L28, | L32 | U4.L34, | U4.R2, | U4.R11, | U4.R15, | U4.R23, | U4.R38, | , U4.R42 | U4.R43, | , U4.R47, | , U4.R50, | , U4. | J4 |
| GROUP | PORT | 11 | NAME:GND.U5, | U5.L6 | I10 | U5.L18 | U5.L2 | U5.L2 | U5.L28 | , 32 |  |  | R1 | U5 | 5.R23, | U5.R38 | U5.R42 | U5.R43, | , U5.R4 | 5.R50, | , U5. | U5.R55 |
| GROU |  |  | NAME | U1.L4, | U1. |  |  | 20, U1 |  | U1. |  |  |  |  | 57, U1 |  | .L65, | 1.L67, | U1.L68, | .L73, | U1.L92 | U1.L107, |
| GR | POR | 163 | NAME | U1. | 1 |  |  |  |  |  |  |  |  |  | 55 |  | 60, | L64, | U1.L66, | U1.L69, | U1.L72 | U1.L90, |
| GR | POR | 4 | NAME | U2. | U2 |  | U2 | , U2 |  |  |  |  |  |  | 57, |  | 5, | 2.L67, | U2.L68, | U2.L73, | U2.L92 | U2.L107 |
| GR | POR | 164 | NAM | U2. | U2.L11, |  |  |  |  |  |  |  |  |  |  |  | 2.L60, U | 64, | U2 | 69, | U2.L1 |  |
| GROUP | PORT | 165 | NAME | U3.I | U3.L8, | U3 | U3 | , U3 |  | U3 |  |  |  |  | 5, |  | 65, | 67, | U3.L68, | U3.L73, | U3.L92, | U3.L107, |
| GROU | POR | 165 | NAME | U3.1 | U3.L11, |  |  |  |  |  |  | 17, U3 |  |  | 55, | 9, | 3.L60, | U3.L64, | U3.L66 | U3.L69, | U3.L72, | U3.L90, |
| GROUP | PORT | 166 | NAME: | U4.I | U4.L13, |  |  |  |  |  |  |  |  | 20, U4. | R33, | R36, U4 | 4.R40, | U4.R45, | U4.R49, | U4.R52, | U4.R57, | U4.R62, |
| GROUP | PO | 166 | AME | J4.I | J4.L10, |  |  |  |  |  |  | 34, U4 |  |  | R15 | R23, U4 | 4.R38, U | U4.R42 | U4.R43 | U4.R47 | U4.R50 | U4.R54, |
| GROUP | PORT | 167 | NAME:VDD.U5, | U5.L1, | U5.L13, |  | U5.L | 25, U5.L |  |  |  |  | 17, U5 | 20, U5. | R33, U5 | R36, U5 | 5.R40, U | U5.R45, | U5.R49, | U5.R52, | U5.R57, | U5.R62, |
| GROUP | PORT | 167 | 7 NAME:GND.U5 | U5. | U5.L1 |  |  |  |  |  |  | 34, U5 |  |  | R15, | R23, U5 | 5.R38, | U5.R42, | U5.R43, | U5.R47, | U5.R50, | U5.R54, |
| GROUP GROUP |  | 16 | NAME NAME: |  | BGA. | BG | $\begin{aligned} & \text { BGI } \\ & \text { BGI } \end{aligned}$ | $\begin{array}{ll} 5, & B G \\ 4, & B G \end{array}$ | $\begin{array}{ll} 9, & B G \\ 1, & B G \end{array}$ | $\begin{aligned} & \mathrm{BG} \\ & \mathrm{BG} \end{aligned}$ | $\begin{array}{ll} 13, & B C \\ 3, & B C \end{array}$ | $\begin{array}{ll} C 7, & \mathrm{BG} \\ \mathrm{B4}, & \mathrm{BG} \end{array}$ |  |  | $\begin{aligned} & . \mathrm{B9}, \mathrm{~B} \\ & . \mathrm{AC} 4 \end{aligned}$ | B11, BG | BGA.B13, | BGA.C3, | BGA.D1, | BGA. D5, | GA.D12, | A.D14, |

## Example 3 - Missing ground pins on the EMD side with grounded IBIS side (better)



## Example 4 - All ground connections are made through the EMD pins (best)


#### Abstract

|  | POR |  | NAME:GND.U1, | U1.L2, | U1.L11, | U1.L15, | U1.L23, | U1.L38, | U1.L42, | U1.L43, | U1.L47, | U1.L50, | U1.L54, | U1.L55, | U1.L59, |  |  |  | U1.L69, | U1.L72, |  |  |  |  |
| :---: | :---: | :---: | :---: |
| UP | PORT | 8 | NAME:GND.U2, | U2.L2, | U2.L11, | U2.L15, | U2.L23, | U2.L38, | U2.L42, | U2.L43, | U2.147, | U2.L50, |  | U2.L55, | U2.L59, | U2.160, | 4, | U2.L66, | U2.L69, | U2.L72, | U2.L90, | U2.L106, | U2.L110, |  |
| GROUP | PORT | 9 | NAI | U3.L2, | U3.L11, | U3.L15, | U3.L23, | U3.L38, | U3.L42, | U3.L43, | U3.L47, | 0, | U3 | U3.L55, | U3.L59, | U3.L60, | U3.L64, | U3.L66, | U3.L69, | U3.L72, | U3.L90, | U3.L106, | U3.L110, | 6 |
| Roup | PORT | 10 | NAME: | U4.L6 | U4.L10 | U4.L18 | U4.L22 | U4.L27 | U4.L28 | U4.L32 | U4. | U4.R | U4.R1 | U4.R15, | U4.R23, | U4.R38, | U4.R42 | U4.R4 | U4.R47 | 4.R50, | U4.R54, | U4.R55, | U4.R59, | U4.R60, |
| GRoup | PORT | 11 | NAME:GND.U5, | U5 | U5.L10, | U5.L18, | U5.L22, | U5.L27, | U5.L28, | U5.L32, | U5.L34, | U5.R2, | U5.R11, | U5.R15, | U5.R23, | U5.R38, | U5.R42, | U5. | U5 | U5.R50, | U5.R54, | U5.R55, | U5.R59, |  |         ! GROUP PORT 169 NAME:VTT.BGA, BGA.AA1, BGA.AA2, BGA.AA3, BGA.AA4, BGA.AB1, BGA.AB2, BGA.AB3, BGA.AB4, BGA.AC2, BGA.AC3, BGA.AC


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## Example 4 - All ground connections are made through the EMD pins (best)



## Example 5 - Ground connections are made through separate ports in Touchstone (ideal)



## Where is the reference terminal for the S-parameter EMD Model

- During extraction, the reference terminal for the S-parameter ports can be on any conductor that is not part of the nets modeled
- During simulation, the reference terminals for the S-parameter ports may all be connected to one node
- usually A_gnd (node 0 in SPICE)
- The single reference node in EMD models will make the ports electrically connected
- Remember, this doesn't mean "shorted"
- Only the voltages between ports positive terminals are considered
- The voltage at any port positive node by itself (referenced to $A \_g n d$ ) is usually meaningless


## Abstract Reference in 3D field solver

- In this scenario it is important to include "Power" and "Ground" nets in the same S-parameter model
- The reference terminal for ports in the electrical modeling procedure (extraction) can be an external
 conductor not connected to any net in the geometry
- Same for all ports
- One external conductor at module pins and another at die pins
- Separate for every port
- The port length must be short relative to the wavelength of the highest frequency in the extraction



## | Thank you!

