

IBIS Interconnect Task Group: Status and Proposal Overview



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http://www.ibis.org/interconnect_wip/

Agenda

- ❑ History
- ❑ The Need for Improved Interconnect Support
- ❑ Principles of the Interconnect Proposal
 - Structure
 - Terminals, Models and Sets
 - New Keywords
- ❑ An Example Explained
- ❑ Summary
- ❑ Q/A

History

- ❑ Interconnect Task Group resumed meeting in early 2014
 - Received draft BIRD from Walter Katz to support IBIS-ISS packages within IBIS

- ❑ 47 drafts since then
 - Active participation and editing by the Interconnect Task Group Members
 - All available at http://www.ibis.org/interconnect_wip/
 - Review and providing comments are encouraged!

- ❑ Nearly finalized for delivery to the IBIS Open Forum
 - If adopted, intended for inclusion in IBIS 7.0

Why Update Interconnect Modeling in IBIS?

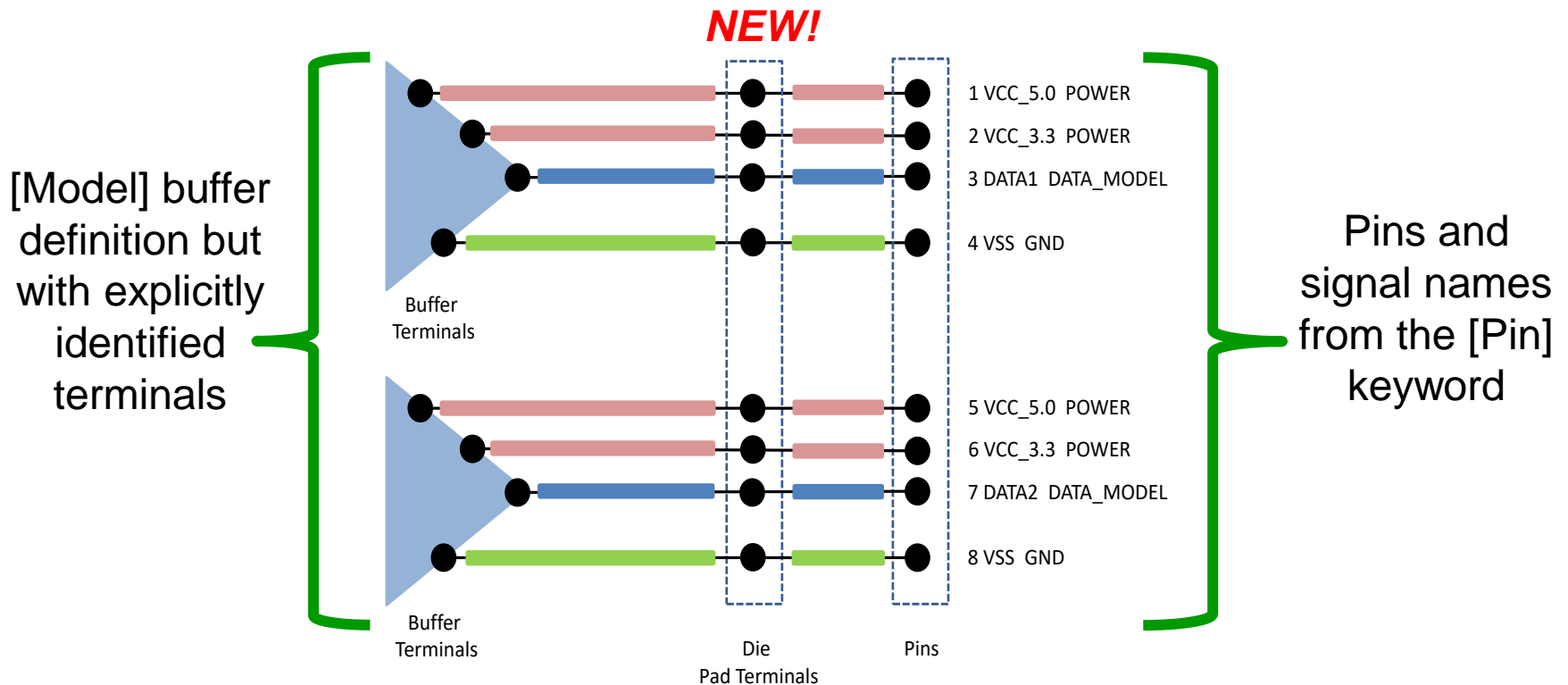
- ❑ The primary focus of these improvements is packaging
- ❑ Package modeling in IBIS has not been seriously revised since 2000
 - IBIS 4.0 – [Alternate Package Models]
 - [Pin], [Package], [Package Model] still the only package modeling methods
 - These are limited in their support of loss, crosstalk and/or partitioning
- ❑ IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
 - These do not directly interact except in a few, very limited, ways... so far
 - ICM has been essentially superseded by IBIS-ISS
 - Package modeling in IBIS still does not support IBIS-ISS or Touchstone
- ❑ EBD exists, but has many of the limitations of IBIS packaging

Principles of the Interconnect Proposal

- ❑ Any useful interconnect improvement proposal must support...
 - Assignment of both I/O and supply (POWER and GND) connections
 - Coupled and uncoupled I/O models
 - POWER and GND models
 - Coupled I/O, POWER, and GND models
 - Clear identification of aggressors and victims in coupled simulations
 - IBIS-ISS and Touchstone models as input
 - Models between pins and buffers, or split into package and on-die interconnect
 - Connections without requiring legacy package keywords
 - Explicit identification of interconnect terminals by pin_name, pad_name, signal_name or even [Pin Mapping] bus_label

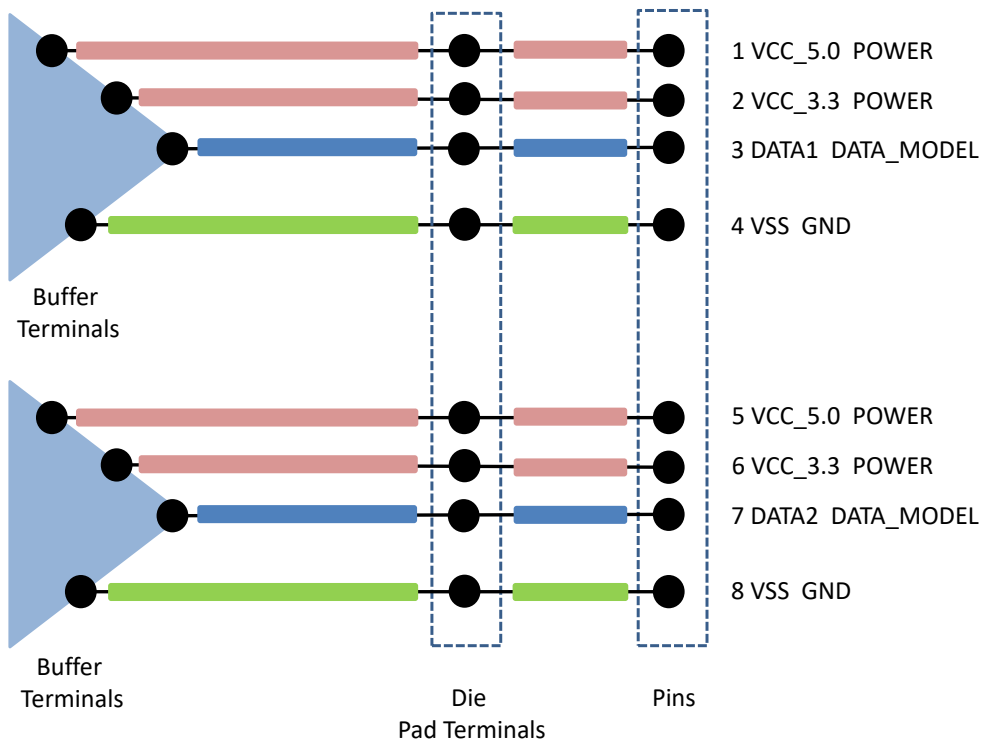
These are expressly stated objectives of the draft Interconnect BIRD, and are supported by it

Structure of the Interconnect Proposal



The proposal introduces “terminals” and makes die pad terminals explicit and separate from buffer terminals

New Concept: Terminals



Original IBIS (4.0 and earlier)

- Pins are explicit
- Buffer terminals implicit in [Model]
- Die pad terminals did not really exist
- Packages defined connections between pins and buffers

Current Proposal

- Die pad terminals are now explicit
- Buffer terminals are now explicit
- [Pin]s are.... still pins
- Separate interconnect definitions can be created from pins to die pad terminals, and from die pad terminals to buffer terminals
- Direct pin-to-buffer connections also (still) supported

Interconnect Models

❑ Interconnect Models

- Describe how terminals connect to other terminals
- Identify terminals as connection points at buffer, die pad, or pin
- Identify terminals as associated with rail or I/O
- Associate the terminals with pin_name, signal_name, pad_name, or bus_label
- Associate the terminals with an IBIS-ISS or Touchstone file
- Identify whether a coupled signal is only an aggressor or also “experiences” coupling from other sources

The format is designed to accommodate the way package and on-die electrical information is generated and delivered today

Interconnect Model Sets

❑ Interconnect Model Sets

- Groups Interconnect Models
- Can be used (and is recommended) to establish a complete path
- Can be grouped with selection controls for individual simulations, similar to [Model] and [Model Selector]

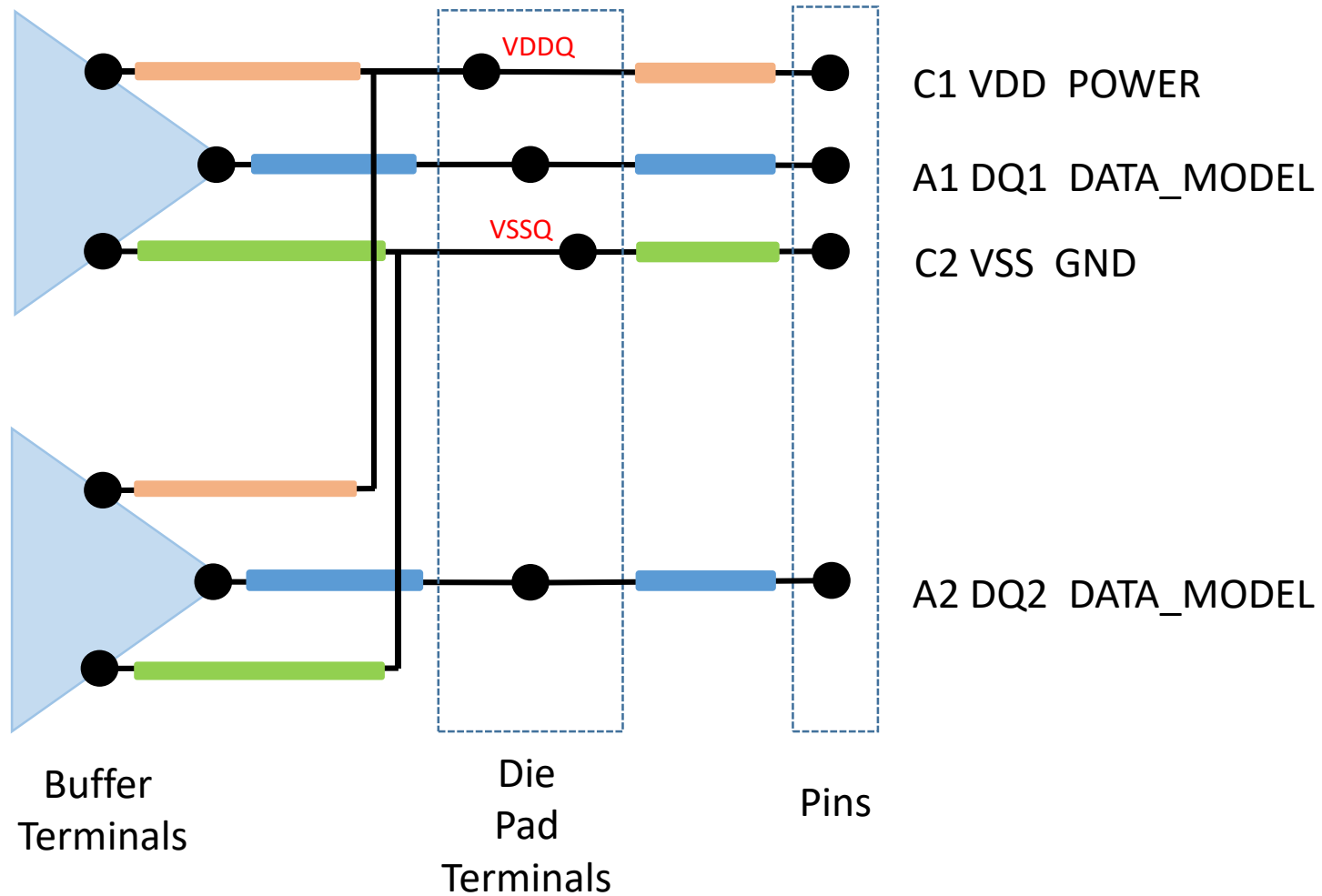
❑ Some Example Groupings and Applications

- Separate sets, one per interface (e.g., memory, network)
- Separate sets for coupled vs. single-line simulations
- Different sets for different power delivery network complexities
 - *POWER connected at single pin, single buffer terminal*
 - *POWER connected through multiple pins, rails to individual buffer terminals*

New Keywords and Subparameters

- ❑ [Bus Labels]
- ❑ [Die Supply Pads]
- ❑ [Interconnect Model]/[End Interconnect Model]
 - Unused_port_termination=<value>
 - Param
 - File_IBIS-ISS
 - File_TS
 - Number_of_terminals=<value>
 - <terminal lines>
- ❑ [Interconnect Model Set] /[End Interconnect Model Set]
- ❑ [Interconnect Model Set Selector]/[End Interconnect Model Set Selector]

An Example Showing Connections



An Example Showing Connections (2)

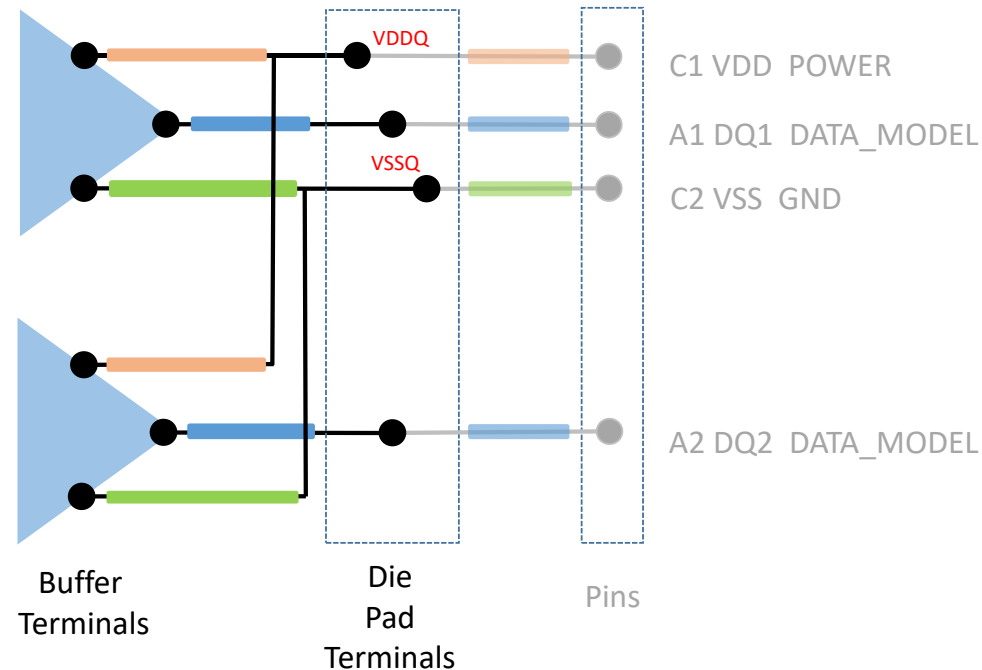
```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
File_IBIS-ISS      buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref   pin_name      A1 | VDD (POWER connection)
4  Pulldown_ref pin_name      A1 | VSS (GND connection)
5  Buf_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pullup_ref   pin_name      A2 | VDD (POWER connection)
7  Pulldown_ref pin_name      A2 | VSS (GND connection)
8  Buf_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail     pad_name      VDDQ | VDD  POWER
10 Pad_Rail     pad_name      VSSQ | VSS  GND
|
[End Interconnect Model]
```

```
[Interconnect Model] Partial_ISS_pad_pin_2
File_IBIS-ISS      pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name    VDD | VDD (POWER connection)
4  Pin_Rail     signal_name    VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ | VDD is signal name
8  Pad_Rail     pad_name      VSSQ | VSS is signal name
[End Interconnect Model]
|
[End Interconnect Model Set]
```

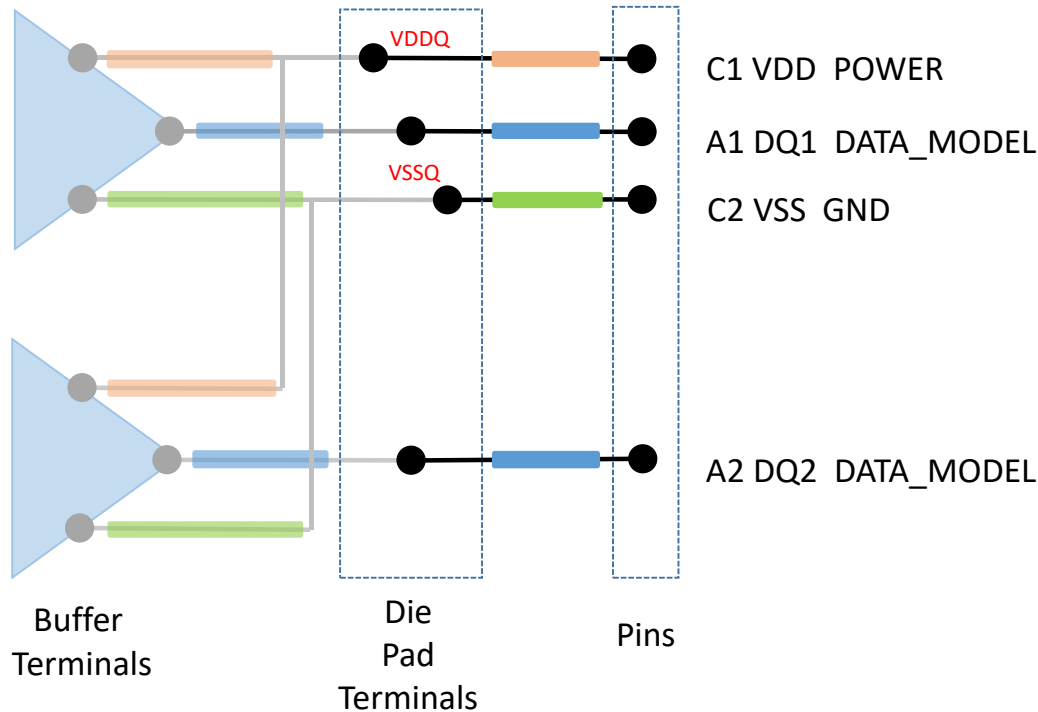
An Example Showing Connections (3)

```
[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
File_IBIS-ISS      buf_pad.iss  buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O      pin_name      A1 |  DQ1 (DQ signal)
2  Pad_I/O      pin_name      A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref   pin_name      A1 |  VDD (POWER connection)
4  Pulldown_ref pin_name      A1 |  VSS (GND connection)
5  Buf_I/O      pin_name      A1 |  DQ1 (DQ signal)
6  Pullup_ref   pin_name      A2 |  VDD (POWER connection)
7  Pulldown_ref pin_name      A2 |  VSS (GND connection)
8  Buf_I/O      pin_name      A2 |  DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail     pad_name      VDDQ |  VDD  POWER
10 Pad_Rail     pad_name      VSSQ |  VSS  GND

[End Interconnect Model]
```



An Example Showing Connections (4)



```
[Interconnect Model] Partial_ISS_pad_pin_2
File_IBIS-ISS          pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name    VDD | VDD (POWER connection)
4  Pin_Rail     signal_name    VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ |
8  Pad_Rail     pad_name      VSSQ |
[End Interconnect Model]
[End Interconnect Model Set]
```

An Example Showing Connections (5)

The [Die Supply Pads] keyword establishes pad_names for rails, and associates them with signal_name and bus_label entries

```
[Die Supply Pads] signal_name bus_label
```

```
VDDQ      VDD
```

```
VSSQ      VSS
```

```
[Interconnect Model] Partial_ISS_pad_pin_2
File_IBIS-ISS      pad_pin.iss  pad_pin_2_typ
Number_of_terminals = 8
|
1  Pin_I/O      pin_name      A1 | DQ1 (DQ signal)
2  Pin_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
3  Pin_Rail     signal_name  VDD | VDD (POWER connection)
4  Pin_Rail     signal_name  VSS | VSS (GND connection)
5  Pad_I/O      pin_name      A1 | DQ1 (DQ signal)
6  Pad_I/O      pin_name      A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names
7  Pad_Rail     pad_name      VDDQ | VDD is signal name
8  Pad_Rail     pad_name      VSSQ | VSS is signal name
[End Interconnect Model]
[End Interconnect Model Set]
```

Additional Improvements

- [Bus Label] and [Die Supply Pads] help clarify meaning of [Pin Mapping]
 - A bus_label defines a single connection (terminal) for multiple rail pins (in [Pin Mapping])
 - A bus_label does the same for multiple buffer rail terminals (also in [Pin Mapping])
 - [Bus Label] supports the above, and together with [Die Supply Pads], extends this to die pads, without requiring [Pin Mapping]

```
[Pin] signal_name model_name
|
1      OUT1      output_buffer1 | Output buffer
3      IO3       io_buffer1     | Input/output buffer
|
11     VSS1      GND             | GND rail connected to pin 11 on signal VSS1, rail GNDBUS1
31     VCC1      POWER          | POWER rail connected to pin 31 on signal VCC1, rail PWRBUS1
51     VSSCLAMP  GND            | GND rail connected to pin 51 on signal VSSCLAMP, rail GNDCLMP
52     VCCCLAMP  POWER          | POWER rail connected to pin 52 on signal VCCCLAMP, rail PWRCLMP
```

```
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
1          GNDBUS1      PWRBUS1                               | Defines supply rails for
|                                                         | these two buffers,
3          GNDBUS1      PWRBUS1      GNDCLMP      PWRCLAMP | including clamp supply connections
|
11         GNDBUS1      NC                               | Associates VSS1 with bus label GNDBUS1
31         NC          PWRBUS1                           | Associates VCC1 with bus label PWRBUS1
51         GNDCLMP     NC                               | Associates VSSCLAMP with GNDCLMP
52         NC          PWRCLMP                           | Associates VCCCLAMP with PWRCLMP
```


Summary

- ❑ The Interconnect Task Group is finalizing a significant improvement to IBIS package modeling through a BIRD
 - Submission to the IBIS Open Forum is expected within weeks
- ❑ This will link IBIS, IBIS-ISS and Touchstone for package models
 - Adds flexible support for package loss, crosstalk and partitioning
- ❑ This also formalizes and separates die pads and buffers

Please review and try out the new advanced Interconnect format!

Q/A