



## IBIS Open Forum Minutes

Meeting Date: **February 3, 2017**

Meeting Location: **DesignCon 2017 IBIS Summit, Santa Clara, CA, USA**

### VOTING MEMBERS AND 2017 PARTICIPANTS

ANSYS	Curtis Clark*, Toru Watanabe*
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Broadcom	Bob Miller
Cadence Design Systems	Brad Brim, Sivaram Chillarige*, Debabrata Das* Ambrish Varma*
Cisco Systems	(Bidyut Sen)
CST	Stefan Paret*, Matthias Troescher*
Ericsson	Zilwan Mahmud*
GLOBALFOUNDRIES	Steve Parker*
Huawei Technologies	(Jinjun Li)
IBM	Luis Armenta, Adge Hawes*, Greg Edlund*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Hsinho Wu*, Eddie Frie* Signorini Gianni*, Barry Grquinovic*
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki, Pegah Alavi*, Fangyi Rao* Stephen Slater*, Jian Yang*
Maxim Integrated	Joe Engert*, Don Greer*, Yan Liang*, Hock Seow*
Mentor Graphics	Arpad Muranyi*, Nitin Bhagwath* Praveen Anmula* Fadi Deek*, Raj Raghuram*, Dmitry Smirnov* Bruce Yuan*
Micron Technology	Randy Wolff*
Qualcomm	Tim Michalka*, Kevin Roselle*
Signal Integrity Software	Mike LaBonte*, Walter Katz*, Todd Westerhoff*
Synopsys	Kevin Li*, Ted Mido*, John Ellis*, Scott Wedge*
Teraspeed Labs	Bob Ross*
Xilinx	(Raymond Anderson)
ZTE Corporation	(Shunlin Zhu)
Zuken	Ralf Bruening*

### OTHER PARTICIPANTS IN 2017

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eASIC	David Banas*
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Independent	Dian Yang*

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Lattice Semiconductor  
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(Logen Johnson)  
Ron Olisar\*  
Wei-hsing Huang\*  
Yasuki Torigoshi\*

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

### **UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 17, 2017	624 999 876	IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/zeulerr>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

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### **OFFICIAL OPENING**

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center, during the week of the 2017 DesignCon conference. About 58 people representing 29 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/feb17/>

Mike LaBonte welcomed everyone to the Summit, opening the meeting at 8:30 a.m. He noted a multitude of mentions of IBIS during the DesignCon conference in papers and presentations. He thanked the sponsors Cadence Design Systems, CST, Keysight Technologies, Mentor Graphics Corporation and Synopsys for offsetting the cost of food and audio-visual equipment.

## **CHAIR'S STATUS REPORT**

Mike LaBonte, Signal Integrity Software (SiSoft)

Mike LaBonte noted there are currently 24 members of IBIS. He introduced the officers and mentioned the officer elections in May 2017. There are weekly teleconferences for several task groups. Summit meetings take place around the world. The Interconnect task group has just released a BIRD related to on-die and package interconnect modeling. The Advanced Technology Modeling task group works on most other technical BIRDs. The IBIS 6.2 specification is in progress and is targeted for release in 2017. He presented a timeline to support this effort. He then showed a tentative schedule for release of IBIS 7.0 in 2018.

Adge Hawes asked if there is a reason for saying that a release will be minor versus major. Mike responded that the original intent of IBIS 6.2 was to make some clarifications of ground referencing. Other technical changes were intended for the next major release. One question is if additional functionality should be accepted for IBIS 6.2 to make it available sooner. This does have an effect on parser costs. Walter Katz commented that he would like to see 6.2 and 7.0 approved before the end of the year with a more aggressive schedule. Bob Ross commented that adding functionality of backchannel support would not be a major parser change. He did not have a concern about backchannel support being in 6.2 as related to the parser. Mike commented that we could look into skipping a 6.2 release and focusing on a 7.0 release.

## **IBIS-ATM TASK GROUP REPORT**

Arpad Muranyi, Mentor Graphics Corporation

Arpad Muranyi showed a list of BIRDs that were discussed in the task group and approved in the Open Forum during 2016. Several BIRDs are expected to be rejected that are related to package modeling, superseded by the new BIRD189. Many BIRDs are in active discussion with some waiting for further discussion once updates are available for review.

## **IBIS INTERCONNECT TASK GROUP: STATUS AND PROPOSAL OVERVIEW**

Michael Mirmak, Intel Corporation

Michael Mirmak reviewed history of the task group formed in 2014. The group was formed to create a solution proposal to improve package and on-die interconnect modeling in IBIS. A proposal has gone through 47 drafts and was introduced one week ago as BIRD189. Package modeling has not been seriously revised since 2000 and still does not support IBIS-ISS or Touchstone. EBD also has many of the limitations of IBIS packaging. Michael showed a list of stated objectives for BIRD189. The proposal introduces "terminals" and makes die pad terminals explicit and separate from buffer terminals. The format is designed to accommodate the way package and on-die electrical information is generated and delivered today. Interconnect Model Sets can be used to group Interconnect Models for various simulation purposes such as coupled or uncoupled options.

Walter Katz commented that this proposal puts wrappers around the types of interconnect models already being created by IC vendors, such as separate models for on-die interconnect

and package interconnect. He also noted that the use of bus\_labels makes it convenient for partitioning of rails to different buffers.

Michael asked people to think about unique cases to make sure the BIRD can describe them. A question was asked about modifications needed to the Touchstone header to support the proposal. Michael noted that no changes are needed to the header. Walter clarified that the terminal number in IBIS is equivalent to the port number in a Touchstone file. A question was asked about the documentation of port ordering in Touchstone files. Michael commented that no assumptions are made about what the port ordering should be. The terminal ordering must be declared correctly in the IBIS file.

## **IBIS-AMI: ASSUMPTIONS, TERMINOLOGY & ANALYTICAL FLOWS**

Walter Katz, Mike Steinberger and Todd Westerhoff, Signal Integrity Software

Todd Westerhoff noted his intention was to establish common terms for discussing IBIS-AMI modeling. Everything unpowered between the TX and RX are called the passive channel and are LTI. The analog channel includes the TX and RX front ends and is assumed to be LTI. The end to end channel includes the algorithmic models as well. Analysis stages include network characterization (circuit simulation) and channel simulation (signal processing). The analysis method for network characterization is not specified by IBIS. He noted that if different tools do not create the same impulse response, the results of channel simulation will be different.

Outputs of statistical and time domain simulation are not specified by IBIS. Three types of algorithmic models exist that allow for statistical simulation, time domain bit-by-bit simulation, or both. This makes for 9 possible simulation cases. One interesting case is a TX with Init-only and an RX with Init-only. A very common case is a TX with Init-only and an RX with GetWave-only. This is common as the TX typically has FIR filters or other equalization which is modeled well with statistical simulation while an RX typically has DFE and adaptability that requires bit-by-bit simulation. A third interesting case is with dual capability models. Todd introduced the language of static equalization and dynamic equalization. Clock recovery modeling is unique to each EDA tool as well as the handling of jitter parameters introduced in IBIS 6.1. Todd asked if the information is complete and correct and if we should incorporate these terms into IBIS.

A question was asked if we have a model that does GetWave and a model that does Init, why do we need a third option that does both? Todd noted it is for simplicity. He noted that for SiSoft they like the ability to draw one schematic that can do both types of analysis with one model. Walter Katz added that when doing statistical you can do simulation with very low BER, and with time domain you are limited to realistic BER simulation of 1E-6 and extrapolation must be done to lower BER.

Michael Mirmak noted that Todd proposed an impulse processing method in 2014 separate from Init and GetWave processing. Todd responded that he would like to see isolation of the impulse response for processing, so that idea is still on the table.

## **THE AMI\_RESOLVE: A CASE STUDY FOR 56G PAM4**

Adge Hawes\*, Steve Parker\*\*, \*IBM Corporation, \*\*GLOBALFOUNDRIES

Adge Hawes noted that AMI parameters are textual and hierarchical, similar to the JSON language. EDA tools send the executable file just parameter value pairs. Corner definitions are difficult to use because it is difficult to define what corners represent. Extreme best and extreme worst corners might be of interest.

AMI\_Resolve introduced a new Usage type into the .ami configuration file. AMI\_Resolve is a housekeeping call that takes care of parameter dependencies before AMI\_Init is called. There are two AMI\_Resolve implementation options with code implemented in the executable DLL or code implemented in the AMI configuration. This requires an interpreter to be built into the DLL code. A major advantage of the second approach is that changes do not require recompilation of the model. The GLOBALFOUNDRIES interpreter solution uses a Forth-like stack-based (RPN) implementation. Adge showed an example of scripting in the AMI\_Resolve input as well as an example of using encryption to obscure the scripting for sensitive dependencies.

Walter Katz asked what the EDA tool should do with a parameter such as baud with a Usage type Dep. Adge commented that the Dep Usage should be replaced by In Usage by the AMI\_Resolve function for the AMI\_Init call.

## **PRACTICAL HSIO LINK DESIGN AND OPTIMIZATION WITH REPEATER AND RETIMER**

Hsinho Wu, Mike Li, Mike Li, Masashi Shimanouchi, Intel Corporation

Hsinho Wu presented the concept of 3R regeneration that reshapes, re-amplifies and retimes signals. Equalizers only solve part of link issues but do not remove effects of random noises, cannot compensate for clock jitter or clock drift, and do not understand data/clock transitions. Repeaters and retimers help solve these problems to boost link margins. Repeaters do not use adaptive equalization, so IBIS-AMI is important for simulating repeaters to determine optimal settings. Retimers are protocol dependent. Placement of retimers in systems is more flexible than repeaters. Experimental results were shown with linear and non-linear repeaters. With linear repeaters, the analysis cannot be used to determine the optimal location for the repeater. Using a retimer requires front end and back end link optimization. Hsinho noted that it is difficult to get good models of repeaters covering corner cases and modeling non-linear behavior more accurately. It is also difficult currently to get models of retimers with accurate jitter sensitivity modeling of the CDR function.

Walter Katz commented that Hsinho's terminology of "linear" and "non-linear" corresponds to usage of Init and GetWave functionality in IBIS-AMI. Hsinho commented that he would like to see more repeater models that use GetWave functions to model non-linear effects. Repeater models are typically just S-parameter models instead of IBIS-AMI models.

Ambrish Varma asked about simulation of repeaters. Hsinho commented that with repeaters, the simulation must be run end-to-end including the repeater. This is not the case for retimers.

## **NECESSITY FOR INTEGRATING FEC FUNCTIONALITY FOR PAM4 IN AMI SIMULATIONS**

Xiaoqing Dong\*, Nick Huang\*\*, \*Huawei Technologies, \*\*Shenzhen Zhongzeling Electronics

Mike LaBonte of Signal Integrity Software presented. Forward Error Correction (FEC) is mandatory in major PAM4 standards to assure basic link BER targets but is not currently supported in IBIS-AMI. Out of a statistical eye simulation you get DFE parameters and a

voltage bathtub. These can be inputs to an error propagation calculation to determine the corrected BER. A case study was shown with symbol error rates for Reed-Solomon signaling that has 10-bit symbols with specific overhead for a given length of transactions. The authors proposed adding FEC functionality to IBIS-AMI.

A question was asked about the need for simulation. Mike responded that the DFE coefficients are needed through simulation as an input to the corrected BER calculation.

Walter Katz commented that he sees IBIS-AMI as a buffer modeling standard and FEC calculations could be done in a simulator outside of the model.

## **USING DATA FILES FOR IBIS-AMI MODELS**

Lance Wang, IO Methodology

Lance Wang noted that creating IBIS-AMI models can require making executables for many platforms and OS's. He presented the concept of creating a single DLL/SO file that references external data files, allowing reuse of code for different transceivers by only modifying the data file. If using data files, the DLL/SO contains AMI standard functions, data processing functions and data file processing functions that might include decryption of the data file. The data file can contain code, data, parameters, and it could be encrypted. With this approach, the DLL/SO file could be developed by professional programmers and used for many different data files. The data file can then be created by designers or modelers and would not require compilation. A test case was shown that pointed to the data file through a Model\_Specific parameter.

Adge Hawes asked if this replaced a proprietary interface for DLL/SO file communication with a standard interface. Ambrish Varma noted that this type of communication already is used by models to store information such as pole/zero information on CTLE circuits in external files. Michael Mirmak commented that he could see a use for paying for some DLL/SO code to do most of the functionality for the AMI file while allowing him to write only a small portion of the code. Walter Katz commented that Lance is showing an example of good programming practice. If additional equalization techniques need to be included, then a new DLL/SO would still need to be rewritten.

## **AMI ANALYSIS USING A PROXY CLASS**

Wei-hsing Huang, SPISim

Wei-hsing Huang presented the concept of using proxy class code for the purpose of development of IBIS-AMI models. The code is called/loaded by the simulator and acts as a man in the middle to intercept/modify data and perform a customized flow. The code can be used for consistency and stress tests, internal backchannel co-optimization to test commutativity, and external backchannel co-optimization using the simulator's post-processing to get performance metrics.

David Banas asked if the second process requires the user to turn off all equalization. Wei-hsing noted that there is no equalization such as when using an RX proxy, the TX is not actually simulated but is bypassed by the proxy.

Walter Katz noted that the backchannel support can be added with BIRD147.5. Wei-hsing commented that the proxy class allows legacy models to implement a backchannel communication.

## **IBIS EXTENSIONS FOR TURN-AROUND CYCLE SIMULATIONS**

Arpad Muranyi\*, Randy Wolff\*\*, Mentor Graphics\*, \*\*Micron Technology

Arpad Muranyi noted there is a need to simulate turn around cycles on memory busses because of SI effects that can negatively affect read/write or write/read transitions. Simulating bus turnaround is desirable with IBIS models. IBIS models are missing the transition information in the waveform tables. This information is needed for transitions from driving to tri-state and tri-state to driving. It is also needed for transitions between on-die termination enabled and tri-state. Additional waveform tables could be added for the new transitions. A simple change to the Bus\_hold Submodel type would allow the Submodel to be triggered by a digital control signal from the EDA tool instead of from a voltage waveform crossing event.

Michael Mirmak asked what would be done with C\_comp modeling. Arpad noted that C\_comp was not changed between states. A question was asked about what signals are used to control the buffers. Nitin Bhagwath commented that control signals for the controller and DRAM included PRBS inputs for data, tri-state and termination control. Another question was asked about use of the B-element for simulation. Arpad responded that the B-element is not accurate because it is missing waveform information related to the transitions.

Michael Mirmak asked about the need to pull in protocol level information to enable this type of simulation. Randy Wolff commented that this is necessary to get correct timing of the various ODT transitions. Timing information from a datasheet would need to be used by the EDA tool to reproduce waveforms that would match measurements and would not violate timing specifications.

Arpad asked if there was interest in seeing a BIRD developed. Walter Katz commented that he would like to see Arpad work with Synopsys on the BIRD.

## **UPDATE ON IBISCHK6.1.3 AND EXECUTABLE MODEL FILE CHECKING**

Bob Ross, Teraspeed Labs

Bob Ross noted that new ibischk6 version 6.1.3 executables are available that resolve BUGs 174-180. The executable names include 32 and 64-bit operating system designations. An enhancement is executable model file checking per BUG179 for [Algorithmic Model] executable lines. Executable files are checked for the existence of required functions based on .ami file Reserved\_Parameters settings including AMI\_Resolve, AMI\_Resolve\_Close, AMI\_Init, AMI\_GetWave and AMI\_Close. The IBIS user guide was also updated.

Ambrish Varma asked if .dll files could be checked on Linux. Bob noted that .so is the recommended file extension for Linux, but if a file is compiled for Linux and named with a .dll extension, it will be checked if possible.

Todd Westerhoff asked how it is determined what version of IBIS-AMI is supported by a .dll. The IBIS file declares a version level and the AMI file declares a version level. Which is looked at? Bob responded that the version in the AMI file is used.

Todd commented that if a .dll contains entry points that do something (such as AMI\_GetWave) but the .ami file says they don't exist, it would be useful to note that the function does exist.

Wei-hsing Huang asked what versions of Linux are supported by ibischk6. Mike LaBonte commented that it is compiled for older versions of Red Hat Enterprise Linux, which should be compatible with newer versions.

## **OPEN DISCUSSION**

Mike LaBonte asked if there were any strong convictions about IBIS 6.2 supporting only the original intent of adding ground reference fixes. One hand went up to express a desire for a cleanup-only 6.2. Walter Katz commented that we need to add local reference language to the specification. He felt that IBIS 6.2 could be released quickly while we separately work on getting the Interconnect BIRD and redriver BIRD finalized for IBIS 7.0. A rewrite of the IBIS-AMI introduction would also be a good thing. Arpad Muranyi commented that if we want to include more technical BIRDs in a 6.2 release, then we should just skip 6.2 and go to a 7.0 release. Bob Ross commented that some BIRDs are very minor parser changes.

Fangyi Rao noted that AMI\_Resolve is needed in order to resolve dependencies on the analog portion of the model before the channel is characterized and AMI\_Init is started.

Mike asked if there were any thoughts on inclusion of more corners in IBIS. Walter noted that with the new Interconnect Model Sets, there are no corners. Corners can be implemented with multiple sets with unique names.

Kevin Roselle asked about support for single-ended signaling from IBIS-AMI. DDR5 will have equalization and will need an ecosystem for support. Walter Katz noted that IBIS-AMI has support now for I/O type AMI models. Ambrish Varma commented that vref levels for single-ended signals are not known. Walter commented that the common-mode voltage is missing when doing impulse response processing. Fangyi commented that AMI cannot address single-ended signaling fundamentally because it ignores the common-mode signal. Part of the common mode is affected by equalization and part of it is not. It may not be an issue for RX but it is for TX models. Todd Westerhoff commented that AMI says nothing about single-ended signaling. Arpad responded that it does specify it is for differential signals. Todd added that it is assumed that the driver, receiver and channel are all linear. With single-ended signaling, power and crosstalk become bigger issues. Michael Mirmak commented that we should look at the JEDEC requirements to see if there are assumptions of linearity baked into the specification. Fangyi commented that the FIR modeling for TX is modeled incorrectly for single-ended buffers with common mode voltage.

## **CONCLUDING ITEMS**

Mike LaBonte again thanked the sponsors Cadence Design Systems, CST, Keysight

Technologies, Mentor Graphics Corporation and Synopsys, the presenters, organizers and attendees.

The meeting concluded at approximately 4:20 PM.

## **NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held February 17, 2017. Votes on BIRD187.2 and BIRD188.1 are scheduled. The following IBIS Open Forum teleconference meeting will tentatively be held March 10, 2017.

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## **NOTES**

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to [info@ibis.org](mailto:info@ibis.org). Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official [ibis@freelists.org](mailto:ibis@freelists.org) and/or [ibis-users@freelists.org](mailto:ibis-users@freelists.org) email lists (formerly [ibis@eda.org](mailto:ibis@eda.org) and [ibis-users@eda.org](mailto:ibis-users@eda.org)).
- To subscribe to one of the task group email lists: [ibis-macro@freelists.org](mailto:ibis-macro@freelists.org), [ibis-interconn@freelists.org](mailto:ibis-interconn@freelists.org), or [ibis-quality@freelists.org](mailto:ibis-quality@freelists.org).
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: `ibischk6`, `tschk2`, `icmchk1`, `s2ibis`, `s2ibis2` and `s2iplt`.

The BUG Report Form for `ibischk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>  
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for `tschk2` resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>  
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for `icmchk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>  
[http://www.ibis.org/bugs/icmchk/icm\\_bugform.txt](http://www.ibis.org/bugs/icmchk/icm_bugform.txt)

To report `s2ibis`, `s2ibis2` and `s2iplt` bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>  
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>  
<http://www.ibis.org/bugs/s2iplt/bugspl.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available

on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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## SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	December 16, 2016	January 6, 2017	January 27, 2017	February 3, 2017
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Active	-	X	X	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	X
Ericsson	Producer	Inactive	-	-	-	X
GLOBALFOUNDRIES	Producer	Inactive	-	X	-	X
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	X	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	X
Keysight Technologies	User	Active	-	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	X
Mentor Graphics	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
Qualcomm	Producer	Inactive	-	-	-	X
Signal Integrity Software	User	Active	X	X	X	X
Synopsys	User	Active	-	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.