

# DDR5 Rx Clock-Forwarding Investigation

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# Why Do We Care About Clock-Forwarding?

- Unlike SerDes channels, DDR transmission lines are not terminated in a matched-impedance (e.g. 50 Ohms)
- Increasing Inter-symbol interference (ISI) at DDR5 speeds requires the inclusion of multiple-tap DFE within both controllers and DRAM for the first time
- In SerDes systems, the DFE is clocked by a CDR...but in DDR5 the DFE is clocked by the external Data Strobe signal (DQS)
- 1 DQS is provided per byte (8x DQ) or per nibble (4x DQ)
- The DFE in the DRAM is not expected to be adaptive, so we expect a list fixed taps selections
- There can be internal delays within the IC that may offer a variation in exact timing instant of the strobe to the DFE block (up to 10ps?)  
*Not Jitter- it is a fixed delay*

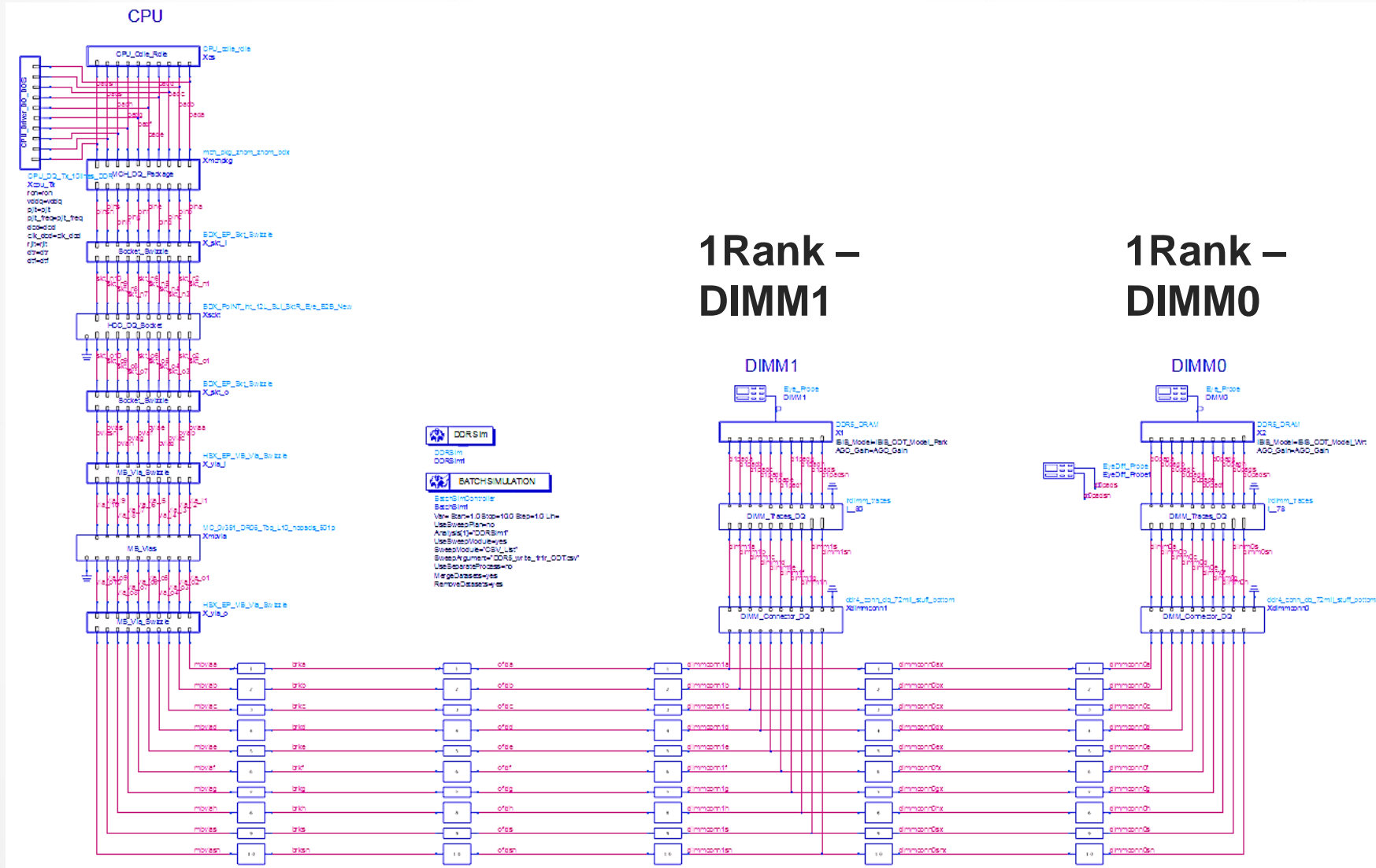
# Why Do We Care About Clock-Forwarding?

- IBIS-ATM has holds on-going discussions regarding the use **Clock times** output from a DQS Rx AMI model & pass those as an Input to a DQ Rx AMI model
- However it ignores internal the internal delays
- In addition, in the Rx architecture on the Controller side, they can make use of an Interpolator on the strobe signal, to fine tune the timing instant that is optimal for all DQ signals

Q: How Does the Timing Instant Impact the Eye?

# First we need a Channel

## A SERVER CASE STUDY EXAMPLE



# Assumptions for Extending the Testbench to DDR5

## TACKLING THE COMPLEXITY OF DDR

DDR5 is not a ratified standard yet. Many specifics will have to be assumed until more is known. Make any assumptions a simulation variable now, so that it is easy to modify and re-run at a later time with new inputs. Assumptions for this investigation:

- **Rise time** and **fall time** for the Memory Controller IP will be **2x faster** than at 2400Mbps.
  - Can this be taken for given?
- **Jitter** will be the same as DDR4 or better than DDR4
- **Rx Mask limits** will not change linearly with Speed Grade. If it's 120mV and 0.22 UI for 2666Mbps
  - Can we be safe with 80mV and 0.25 UI for DDR5 @4800Mbps?

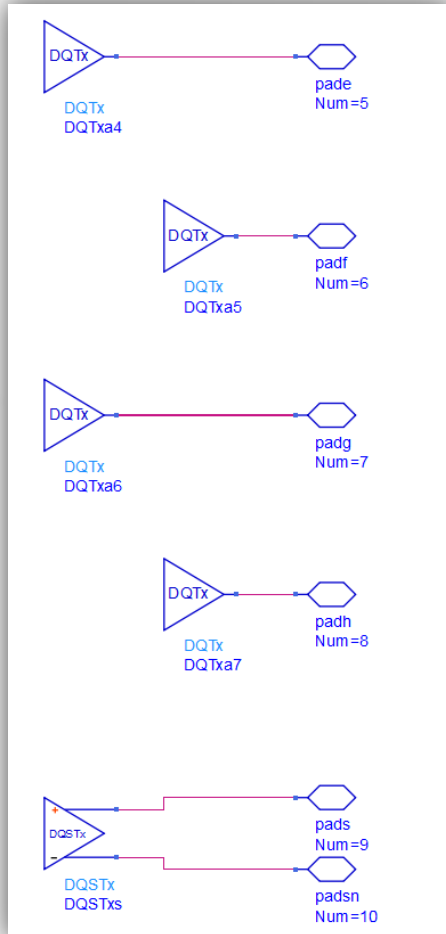
**Table 1: DRAM DQs In Receive Mode; \* UI=tck(avg)min/2**

Symbol	Parameter	1600,1866, 2133		2400		2666	
		Min	Max	Min	Max	Min	Max
VdIVW	Rx Mask voltage pk-pk	-	136	-	130	-	120
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22

Each assumption is author's guess and not based upon knowledge of JEDEC discussions

# Evolving from DDR4 Knowledge

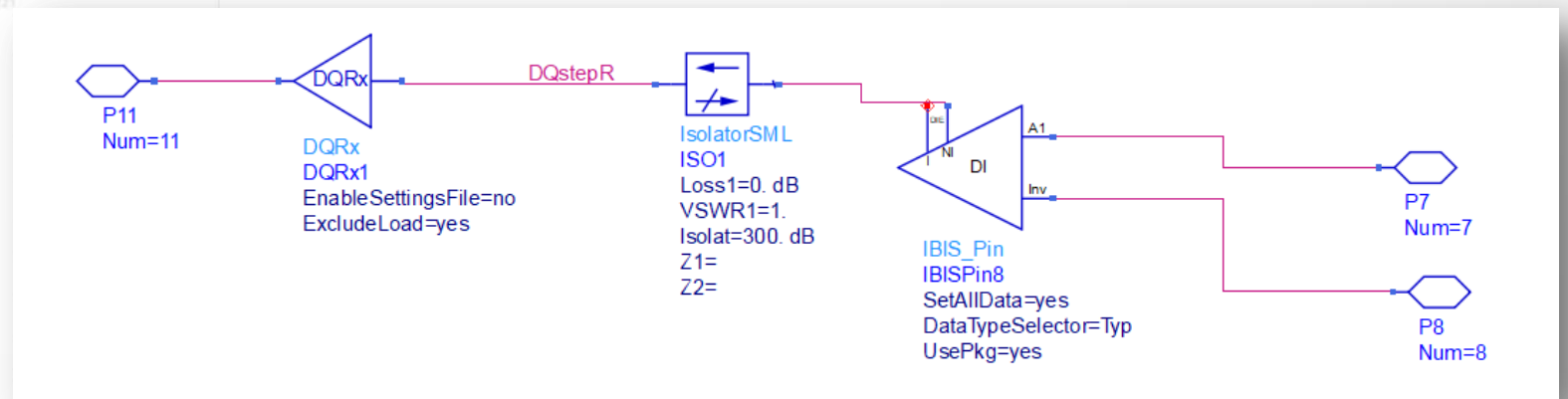
## EXTENDING THE CASE TO DDR5 4800 MBPS



**Memory Controller Model for CPU** – Represented by Tx sources with the following parameters specified:

- Drive Strength (A load in Ohms)
- RJ
- DJ
- Cdie
- ODT value
- RiseTime
- FallTime

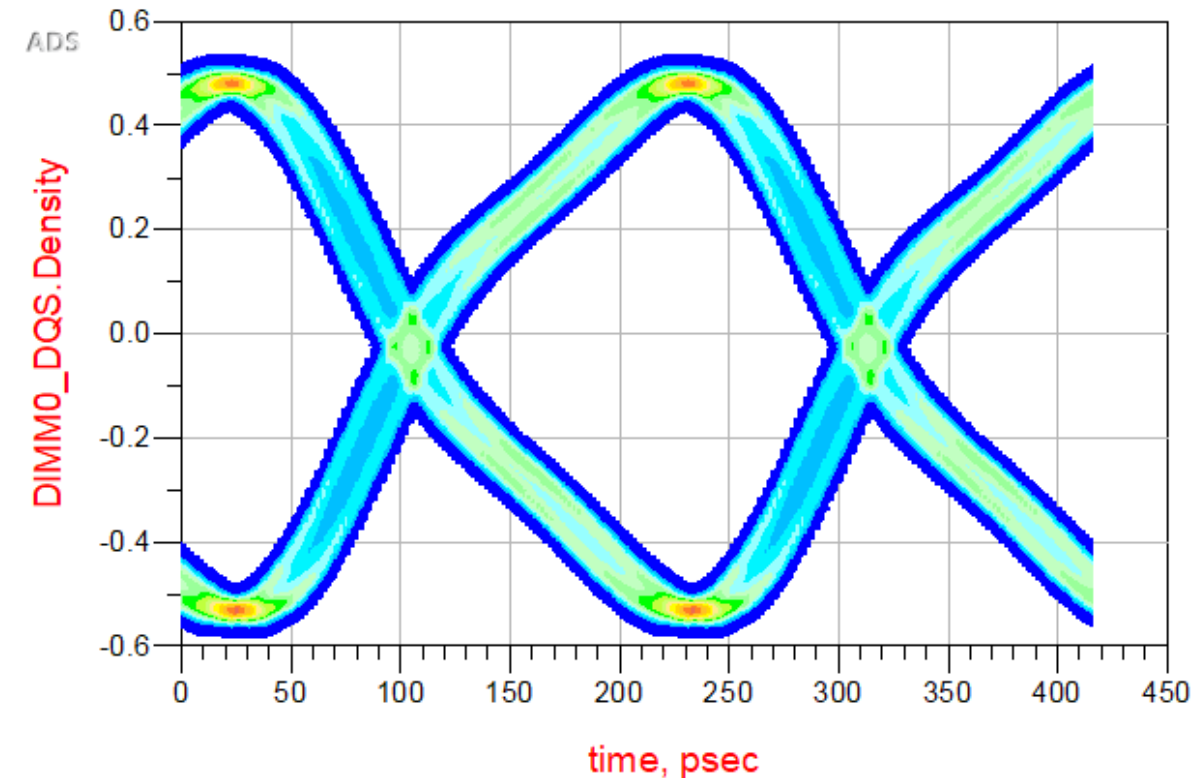
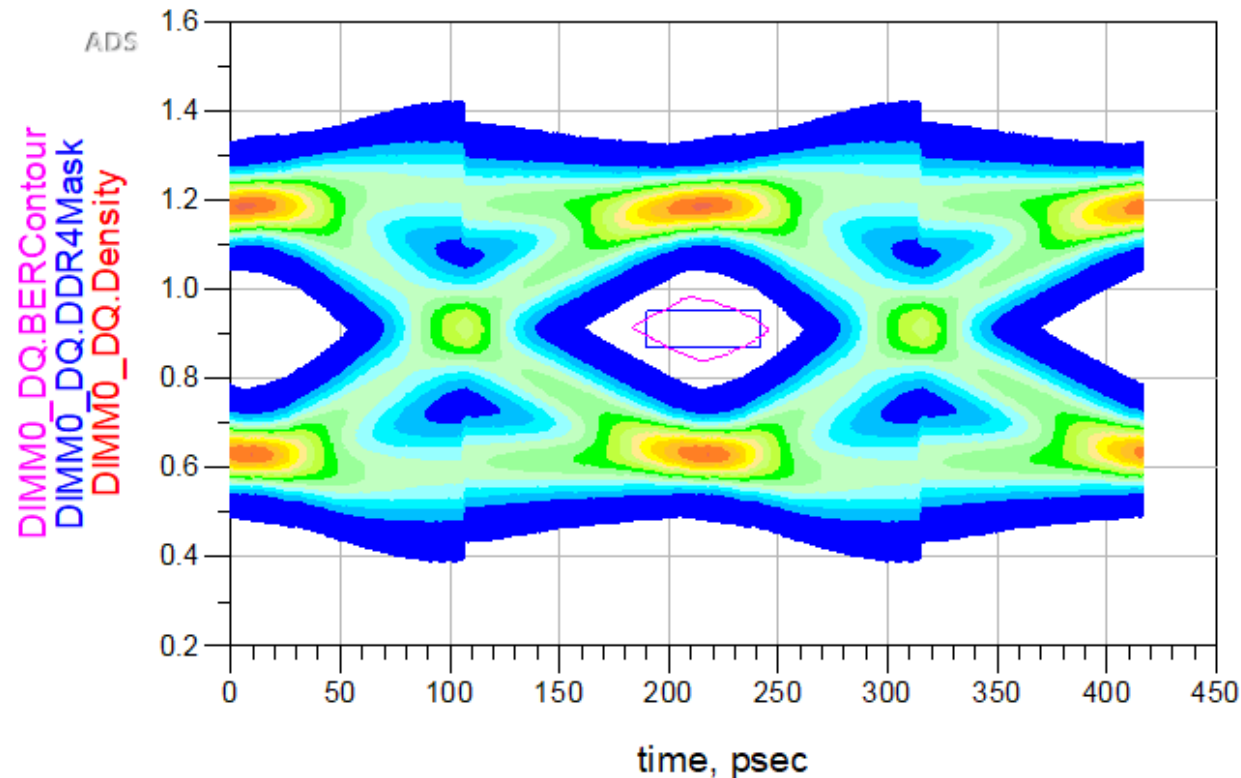
**DRAM Models** – Represented by a DDR5 preliminary IBIS model, and DQ\_Rx block providing 4-tap optimized DFE



# First Simulation Result for 1r1r Configuration

CLOSE BUT FAILS RX MASK @BER OF 1E-16

Simulator returned these Optimized Tap Values:  
-0.0251 -0.0015 0.0021 -0.0076



# Exporting the Channel

- Ideal scenario is to export the step response of the combined channel (including the IBIS models with the correct ODTs selected)
- Step response can be imported to a DSP simulation as a special 'Timed FIR' filter – where the step response is resampled and converted to an impulse response.
- Alternatively export S-parameters – difficulty with this method is that the S-parameter testbenches like to have same port impedances at both sides (not ideal for DDR cases), and effects of the analog part of the IBIS model (their loading on the channel) are discounted.

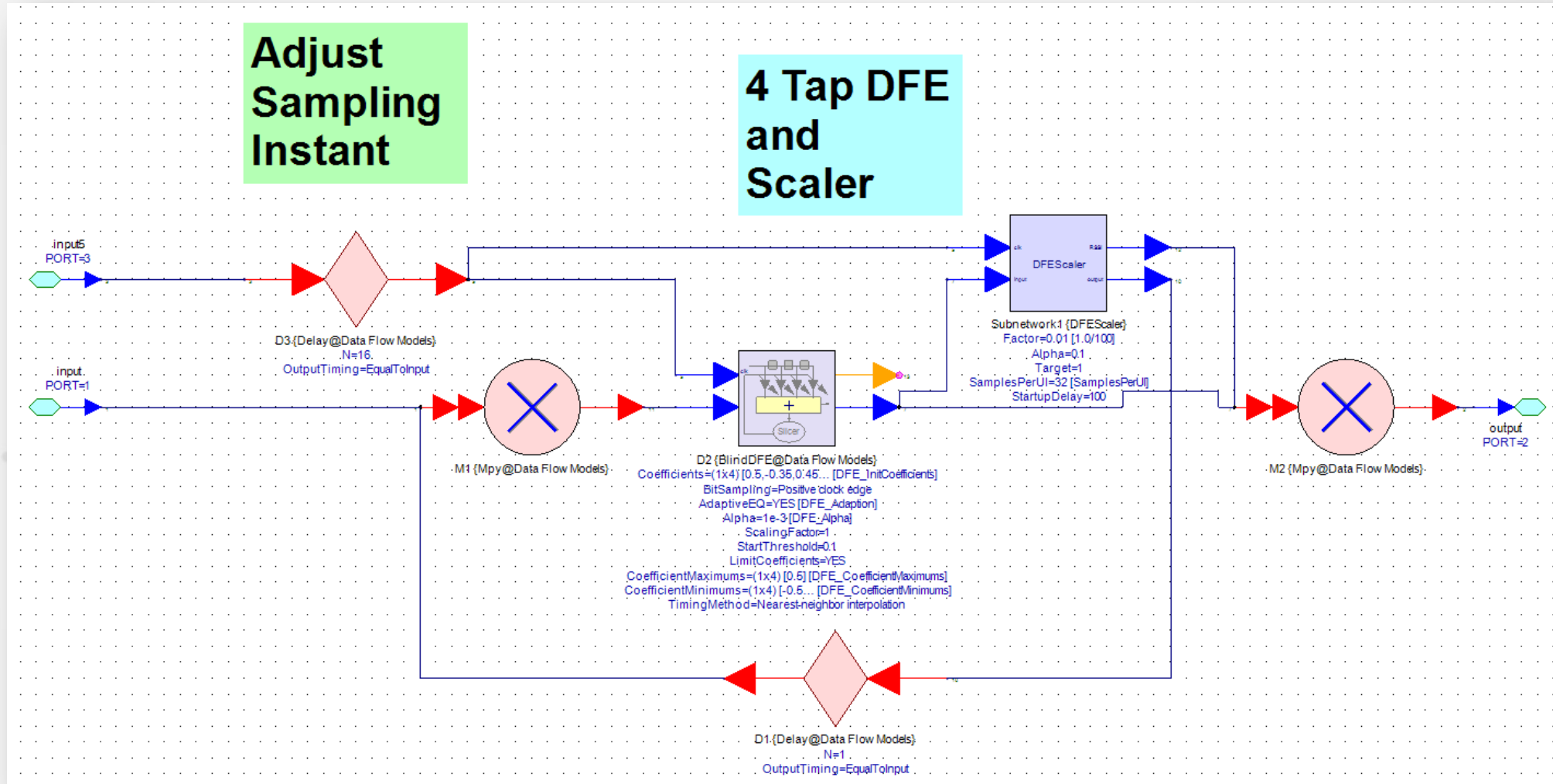




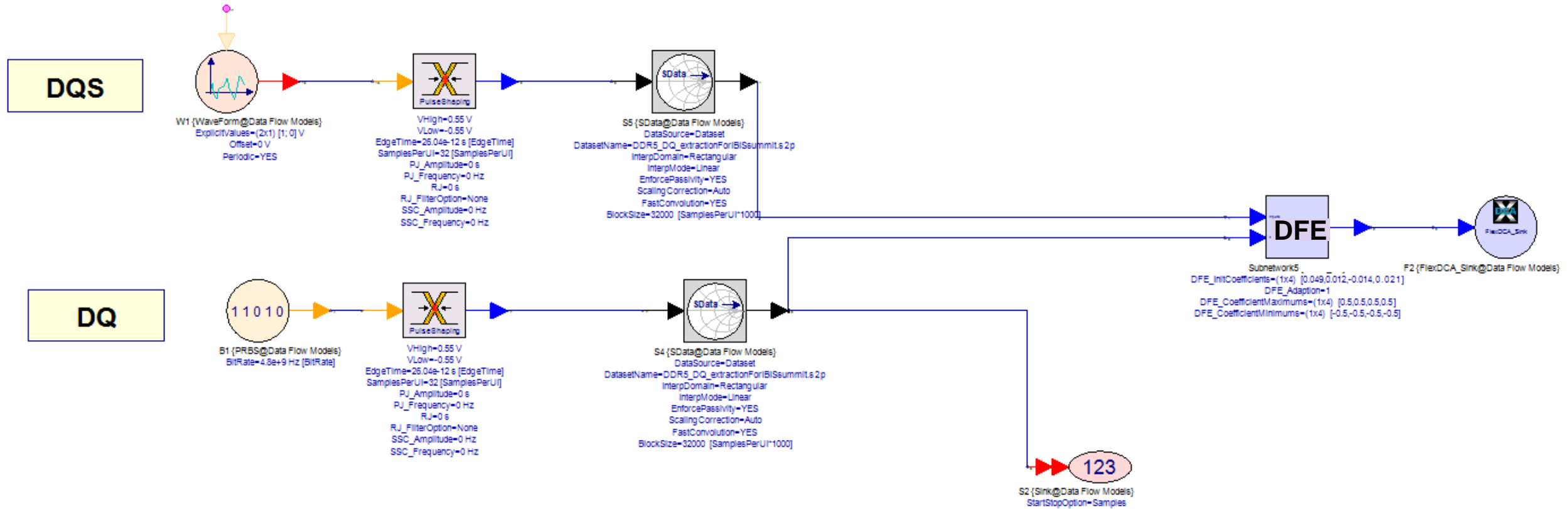
# Move from System Simulation – to DSP domain

TO CONTINUE THE INVESTIGATION

# Decision Feedback Equalizer



# Now in a Data Flow Simulation–

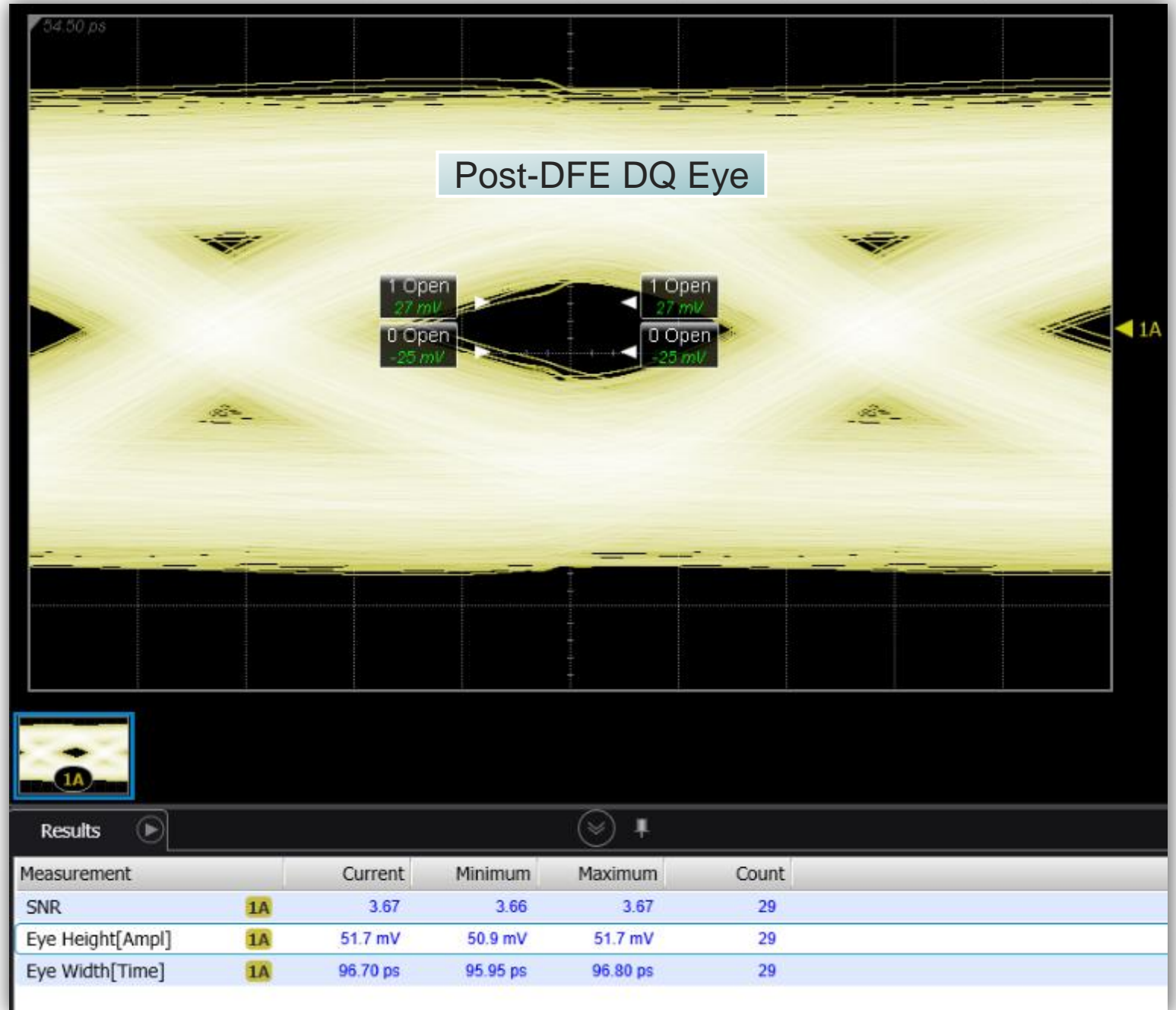


# Output Eye – Nominal

## Nominal Strobe Timing

SNR            3.67  
Eye Height    51.7 mV  
Eye Width     96.7 ps

Allow 4-tap DFE to adapt to find  
base-line EQ taps, then fix the  
values for the next cases.

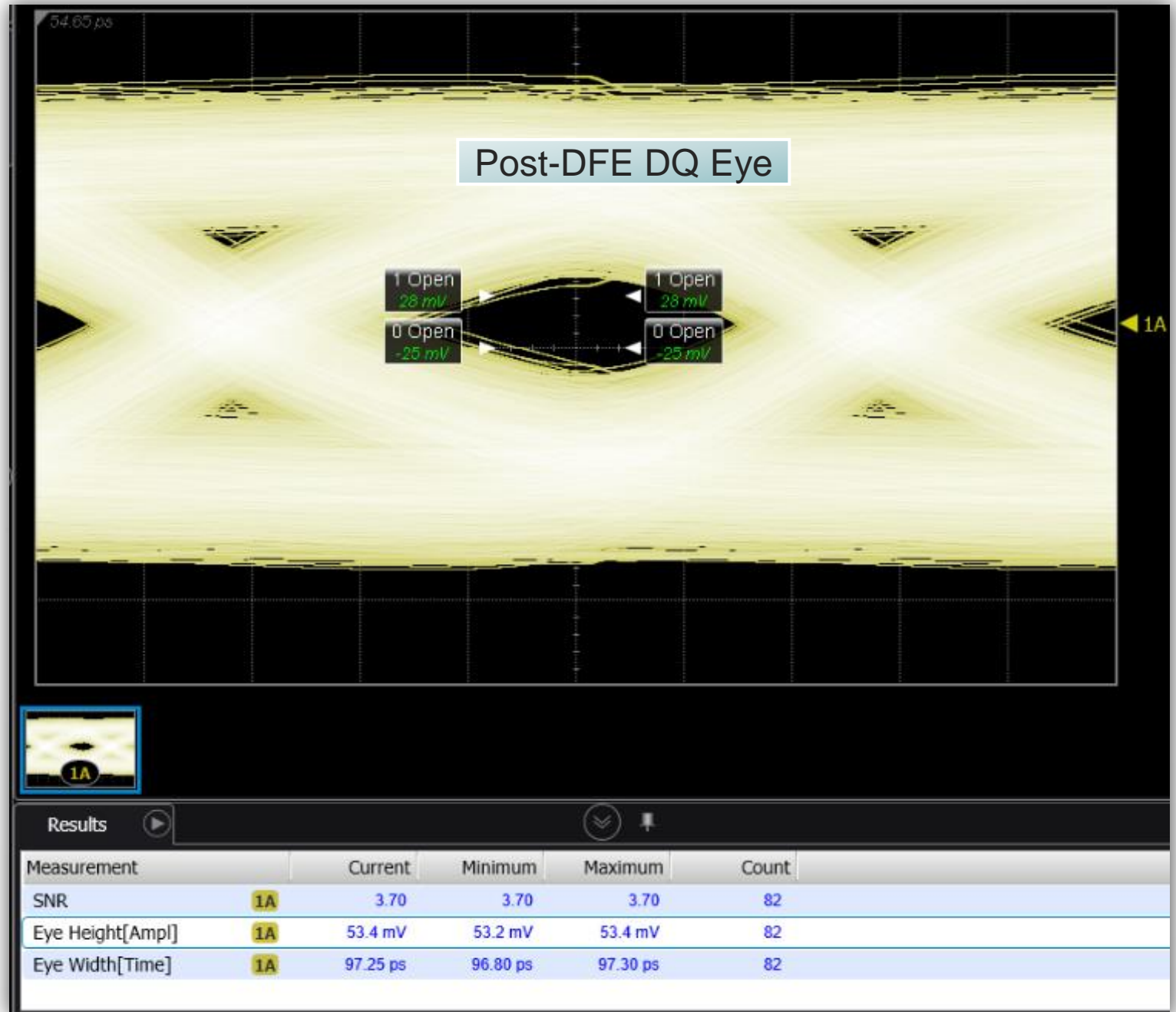


# Late Strobe w/Fixed Taps

Strobe 2 samples **late (+13ps)**

SNR            3.7  
Eye Height    53.4 mV  
Eye Width     97.25 ps

Fixed Taps – result is a little better



# Early Strobe w/Fixed Taps

Strobe 2 samples **early (-13ps)**

SNR            3.64  
Eye Height    49.9 mV  
Eye Width     97.55 ps

Fixed Taps – result is a little  
worse than baseline





**Surprising! I expected much greater deviation**

What if we can optimize both  
tap values and strobe timing?

# Late Strobe w/Adapted Taps

Strobe 4 samples later (+26ps)

SNR 3.89  
Eye Height 64.4 mV  
Eye Width 110.75 ps

Allow adaptive tuning

It's better than the baseline!





# Early Strobe w/Adapted Taps

Strobe 4 samples **early** (-26ps)

SNR 4.18  
Eye Height 79.6 mV  
Eye Width 111.7 ps

Allow **adaptive tuning**

It's looking **MUCH** better!

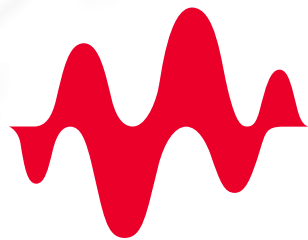
30mV and 20ps more  
margin than baseline



# Summary

- 1. Demonstrated that when taps are fixed the eye opening is not so sensitive to changes to small changes in strobe timing.
- 2. Demonstrated that there is a strong relationship between signal, clock timing and DFE tap values that the **controller** can exploit to optimize the link

Since the clock signal is not We recommend that Clock waveforms be passed to the IBIS-AMI (in bit-by-bit mode) as a new additional input, to allow for such complex behavior to be modeled



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4.50221