IBIS V7 and IEEE 2401 Harmonization

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JEITA Semiconductor Organization

Japan Electronics and Information Technology Industries Association

JEITA-JSIA Semiconductor Industry Association in Japan

Semiconductor Standardization Committee in Japan

LPB Semiconductor & System Design Technical Committee

Chair : Yoshinori Fukuba (SC47A secretary)

International Standard & Steering Working Group

Leader : Genichi Tanaka (TC91WG13 co-convenor)

LPB(LSI Package board) interoperable design sub-committee

Leader: Yoshinori Fukuba

LPB Design Data Exchange Format Working Group

LPB Modeling Working Group

Member: Megumi Ono

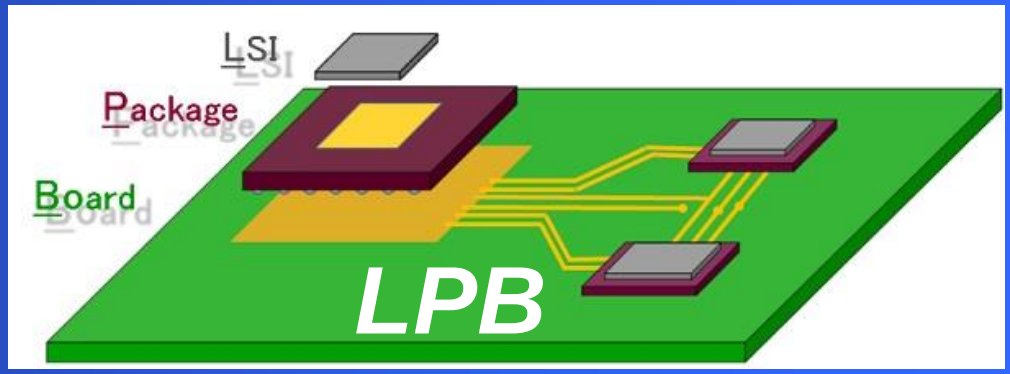
LSI Package Board needs…

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by

LPB ***Standard formats IEC 63055***

IEEE 2401(dual logo)



Contents

- Introduction
- IEC 63055/ IEEE 2401 Concept
- IBIS V7 harmonization & schedule
- Conclusion

Background

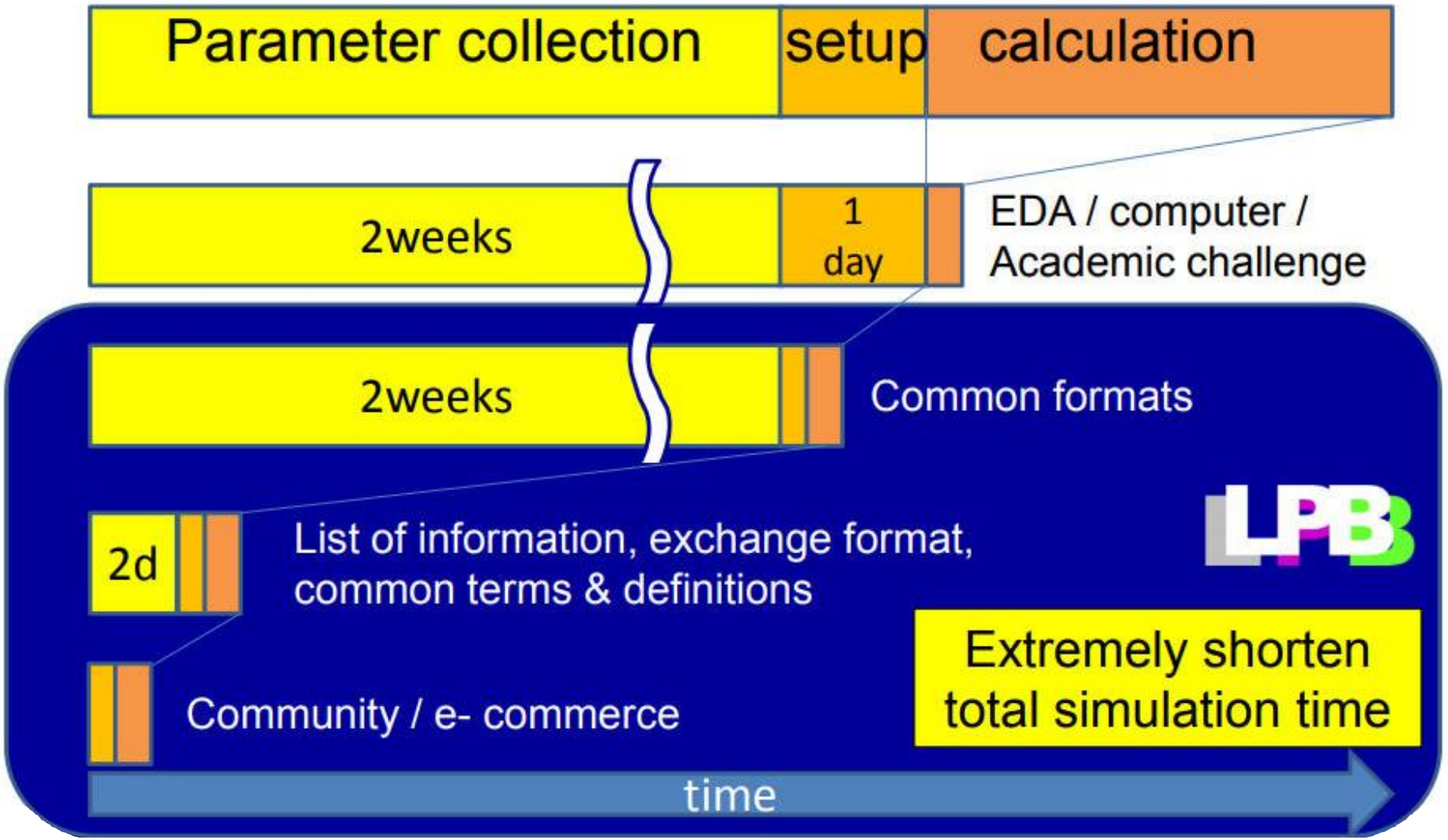
- Need Seamless Data Transformation among LSI (large scale integration), Package and Board
  - Conversion is needed from one to another
  - Mistakes may occur in manual operation
  - Long verification time even for correct setup

- Time is Money!!
  - Engineers need to spend time for innovation
  - Early production gets market share
  - Simpler operation makes better quality

Standardization Strategy

- Make Abstraction Level Higher
- Make Business More Successful
- Make Cost Smaller
- Make Design More Effective
- Make Ecosystem More Attractive

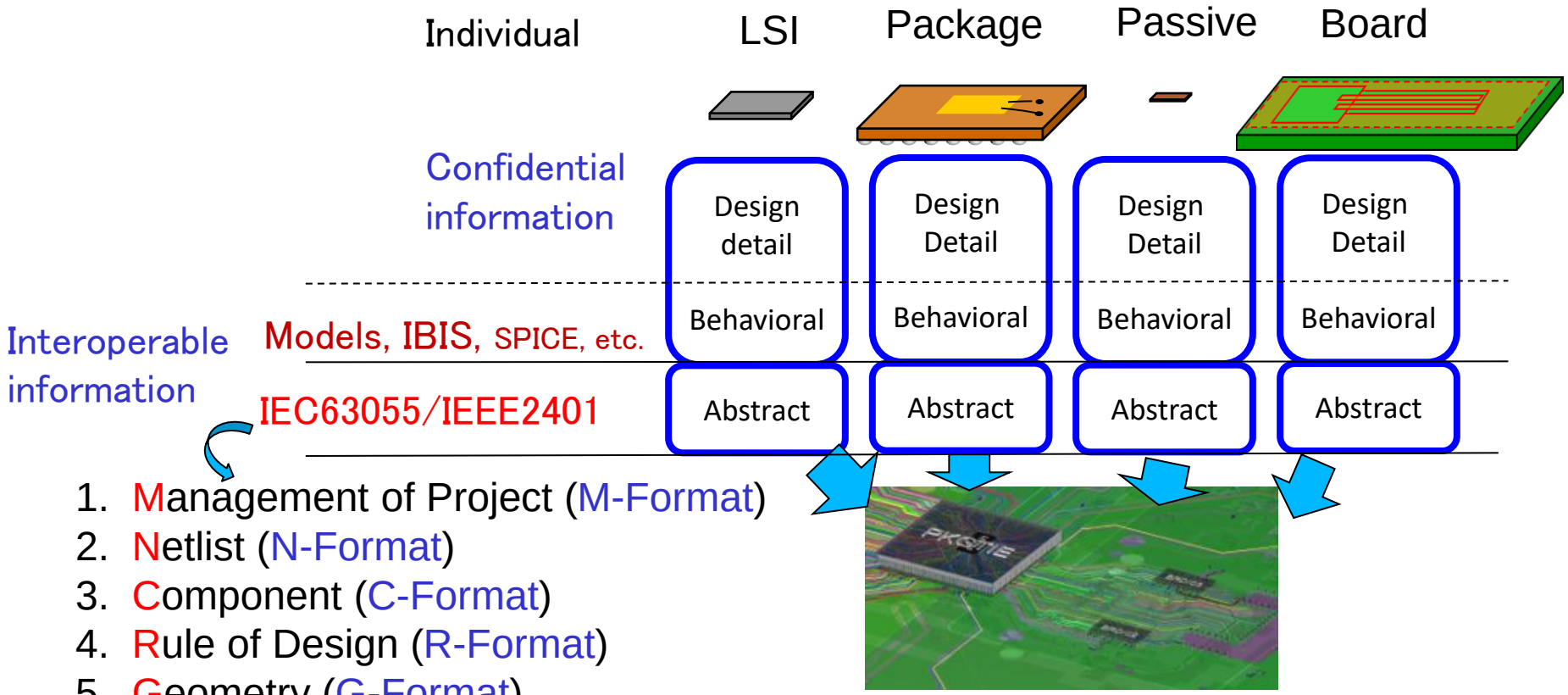
Effect of IEC 63055/IEEE 2401



What is IEC 63055/ IEEE 2401-2015?

Standard Format for LSI Package Board (LPB) Interoperable Design.

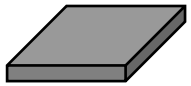
For effective information exchange in supply chain.



1. Management of Project (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Rule of Design (R-Format)
5. Geometry (G-Format)

What is IEC 63055/ IEEE 2401-2015?

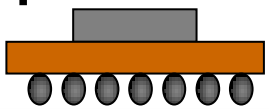
In the deployment of electronic products…



C-Format

Die Size
Pad location
Spice Model
correspondence

Die models
IBIS/SPICE
CPM/LPM



C-Format

Package size
Terminal location
Spice/IBIS/S-param model
correspondence

Package models
IBIS
S-param SPICE

C-Format

Die mount
Coordinate,
Orientation
Flip, etc.

C-Format

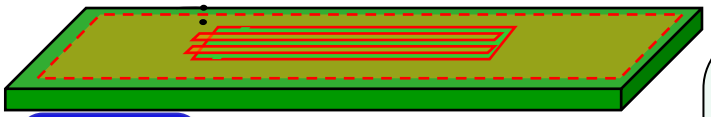
Package mount
Coordinate,
Orientation
Flip, etc.

G-Format **R-Format**

Package Layout
Wire Bonding
Layer stack-up
Via, material

M-Format

Combination of C, G, R, N which constitute the analysis target



R-Format

Line/Space
Via pitch/size/hole
Layer Stack up
Material parameter

G-Format

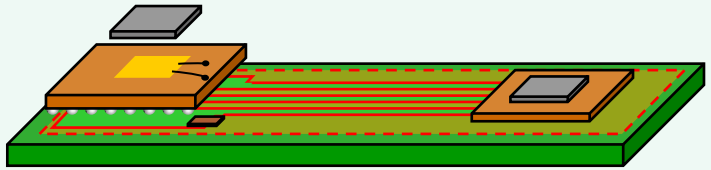
PWB Routing
/Plane

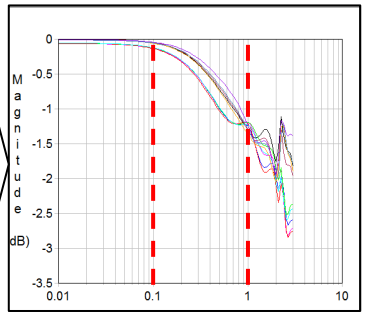
Connectivity

N-Format

Netlist

Simulation Platform

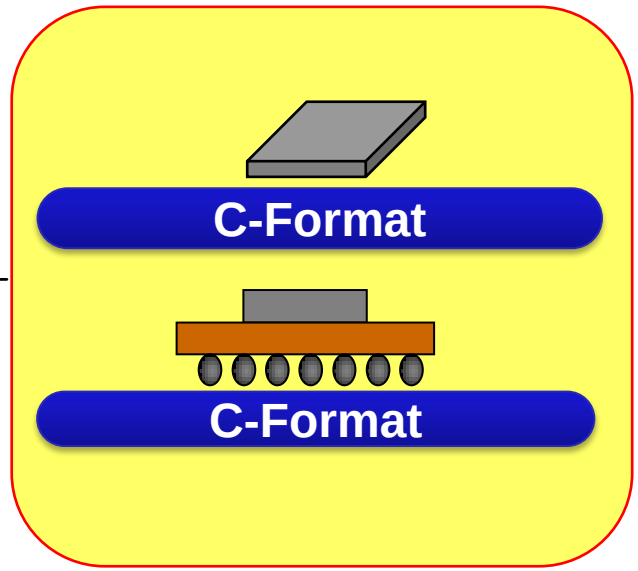




Model “ Wrapper”

■ Function to wrap models to pass models and IPs information to CAD / CAE simultaneously

Geometry
Terminal correspondence
Models
- SPICE
- S parameter
- VHDL (AMS)
- Verilog-HDL
- IEC 62433
- IBIS V4, AMI
- IBIS V7
- SystemC (AMS)
- Thermal models



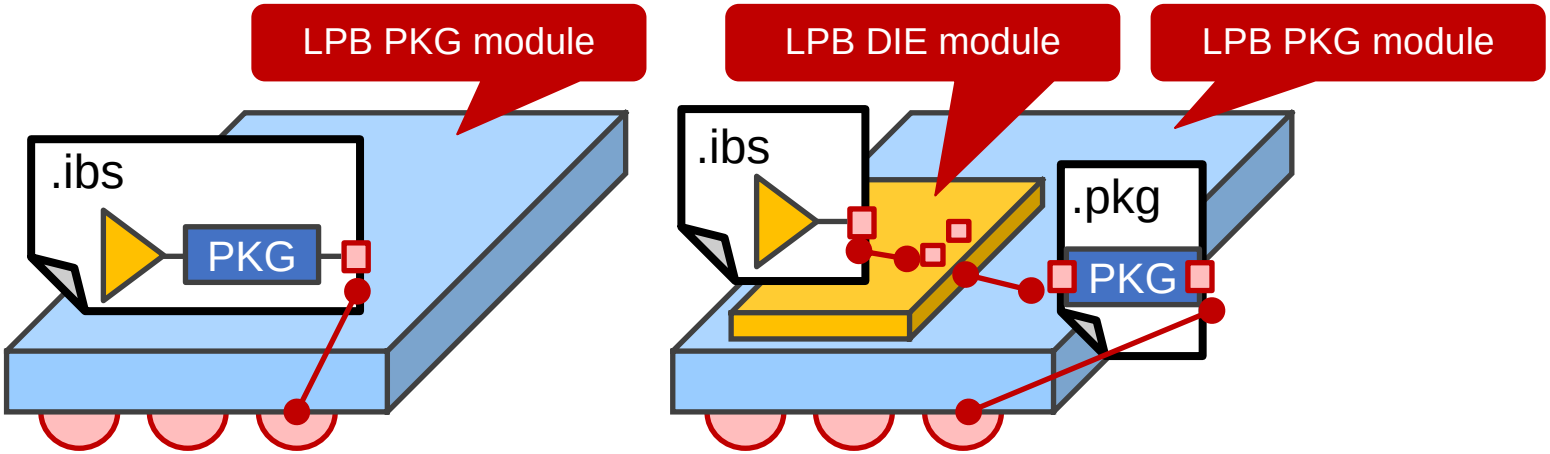
CAE
(SI,PI,EMC, thermal mechanical)

CAD
(Artwork, place, route planning)

Study for IBIS & LPB, Case: IBIS 6.0

In many cases, IBIS6.0 doesn't have die pad information.
Therefore IBIS is linked to LPB PKG module.

If you obtain .pkg file and .ibs file without package model, you can use them for PKG module and DIE module separately.
Then PKG module can be stacked with DIE module.



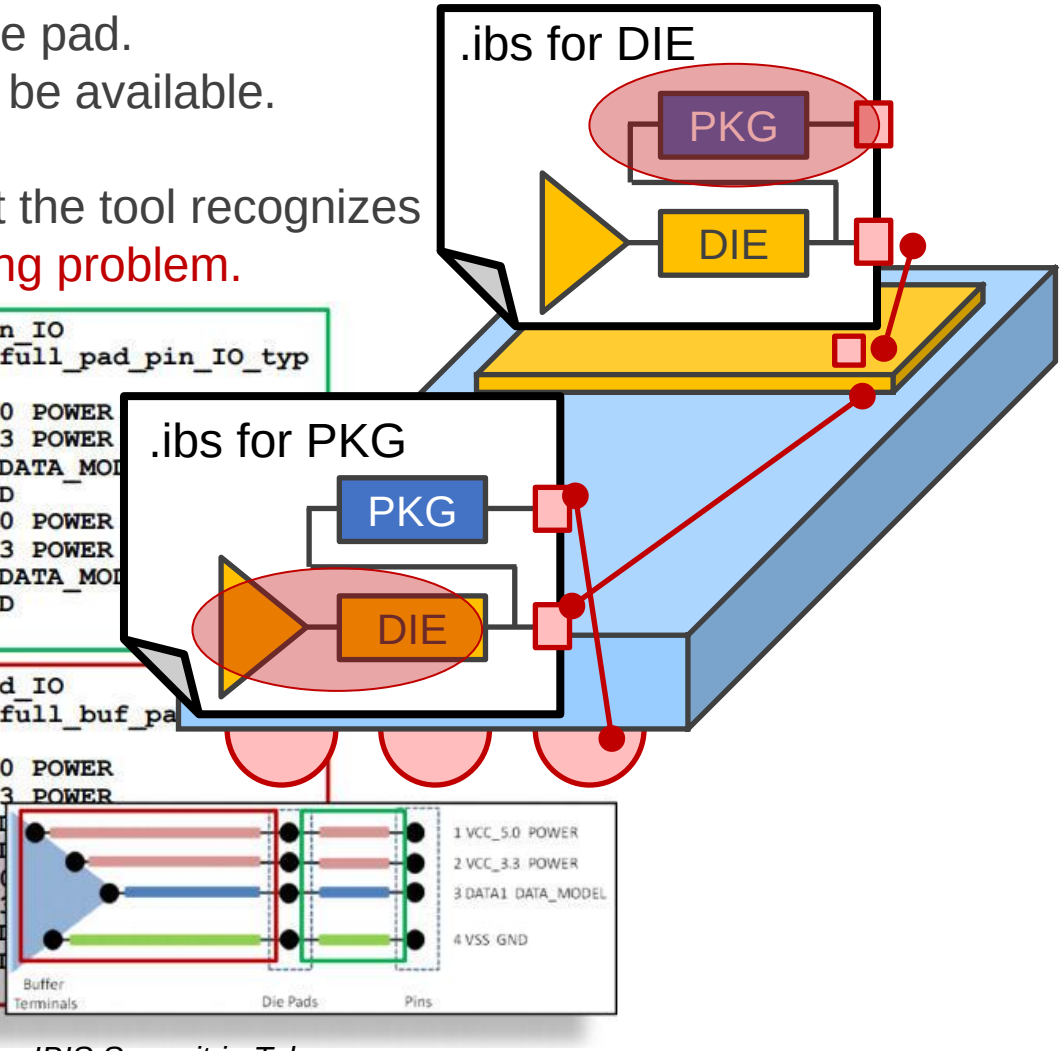
Study for IBIS & LPB, Case: IBIS 7.0

[Interconnect Model] can define die pad.
In this case LPB DIE module may be available.

However, there is a possibility that the tool recognizes each model twice – double counting problem.

```
[Interconnect Model]          Full_ISS_pad_pin_IO
File_IBIS-ISS    full_pad_pin_io.iss          full_pad_pin_IO_typ
Number_of_terminals = 8
1   Pin_Rail      pin_name       1     |  VCC_5.0 POWER
2   Pin_Rail      pin_name       2     |  VCC_3.3 POWER
3   Pin_I/O       pin_name       3     |  DATA1 DATA_MOD
4   Pin_Rail      pin_name       4     |  VSS GND
5   Pad_Rail  →   pad_name     VCC1    |  VCC_5.0 POWER
6   Pad_Rail  →   pad_name     VCC2    |  VCC_3.3 POWER
7   Pad_I/O       pin_name       3     |  DATA1 DATA_MOD
8   Pad_Rail  →   pad_name     VSS1    |  VSS GND
[End Interconnect Model]
```

```
[Interconnect Model]          Full_ISS_buf_pad_IO
File_TS          full_buf_pad_io.s8p |        full_buf_pa
Number_of_terminals = 8
1   Pad_Rail  →   pad_name     VCC1    |  VCC_5.0 POWER
2   Pad_Rail  →   pad_name     VCC2    |  VCC_3.3 POWER
3   Pad_I/O       pin_name       3     |  DATA1 D
4   Pad_Rail  →   pad_name     VSS1    |  VSS GND
5   Buffer_Rail   pin_name       1     |  VCC_5.0
6   Buffer_Rail   pin_name       2     |  VCC_3.3
7   Buffer_I/O    pin_name       3     |  DATA1 D
8   Buffer_Rail   pin_name       4     |  VSS GND
[End Interconnect Model]
```



Concerns and required actions

Concern: double count of die and PKG model in case LPB with IBIS7.0

Action: add the optimal function to LPB ?

✓ active

LPB Example of modification to correspond to IBIS 7.0		[Model]	[Package]	[Pin]	[Package Model]	[Inter-connect]
<ibis:ref_port component=aaa />		✓	(Depends on simulator)			
	<pkg type=short/>	✓				
	<pkg type=package/>	✓	✓			
	<pkg type=pin/>	✓		✓		
	<pkg type=package_model/>	✓			✓	
	<interconnect name=xxx/>	✓				✓
<ibis:ref_port component=aaa without_buf=yes />			(Depends on simulator)			
	<pkg type=short/>					
	<pkg type=package/>		✓			
	<pkg type=pin/>			✓		
	<pkg type=package_model/>				✓	
	<interconnect name=xxx/>					✓

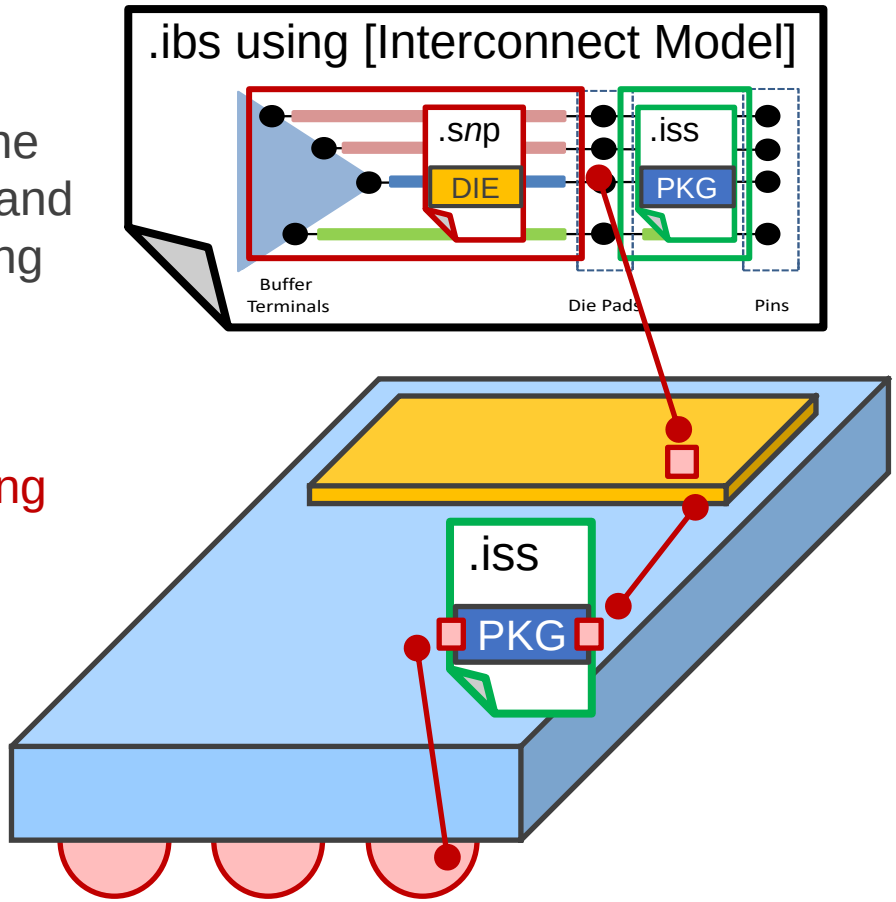
<pkg/> and <interconnect/> can be written together.
More than one <interconnect/> can be written.

Solution

[Interconnect Model] can define die pad.

LPB is going to support directly referring the die pad on IBIS like [Interconnect Model], and to add Touchstone and IBIS-ISS as referring models.

Therefore, DIE and PKG module can be available separately without double counting problem.




```
<reference xmlns:ibis="http://www.jeita.or.jp/LPB/ibis"
  reffile="XXXX.ibs" format="IBIS"
>
  <connection socket_name="socket1" port_id="A1">
    <ibis:ref_port component="ibis_die" signal_name="VCC1"
    terminal_type="Pad_Rail" />
  </connection>
  <connection socket_name="socket1" port_id="A2">
    <ibis:ref_port component="ibis_die" pin_name="3"
    terminal_type="Pad_I/O" />
  </connection>
  ...
</reference>
```

Development of IEEE 2401 revision

Current Ver.: IEEE 2401-2015

https://standards.ieee.org/standard/2401-2015.html

Dual Logo: IEC 63055/ IEEE 2401-2015

Revision work Project profile:
https://standards.ieee.org/project/2401.html

Current status/plan (@ 2019-01-29)

- D2(Draft 2) in circulation, (followed by D3, D4 …)
- Draft with WG approval May, 2019
- Sponsor ballot ; June to October, 2019
- Publish → Target IEEE 2401-2020

Conclusion

- Share IEC63055 / IEEE 2401 Concept
  - Mutual Communication
  - Design Consistency
  - Shorten Development Time

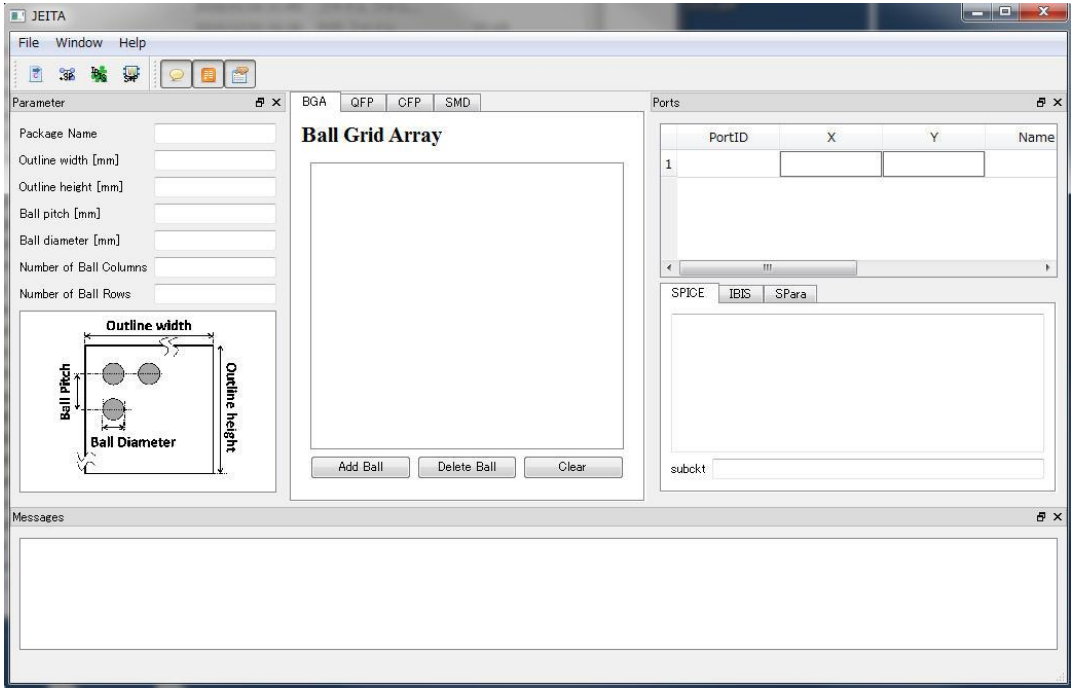
- Modifications of IEEE 2401 for IBIS V7
  - Example
  - Schedule IEEE 2401-2020

Collaboration for making Designers Happy!!

Appendix

Who provides LPB?

For the components, LPB files should be released by component vendors.
Some commodity parts are getting ready!
JEITA has released the sample data and tools for either vendor or user to create LPB files.
In case you have to make LPB by yourself, use ‘LPB design kit’ released by JEITA that can export simple LPB files.



http://www.lpb-forum.com/lpb-open-source-project/download/
Sorry, this web site is Japanese.

System Design

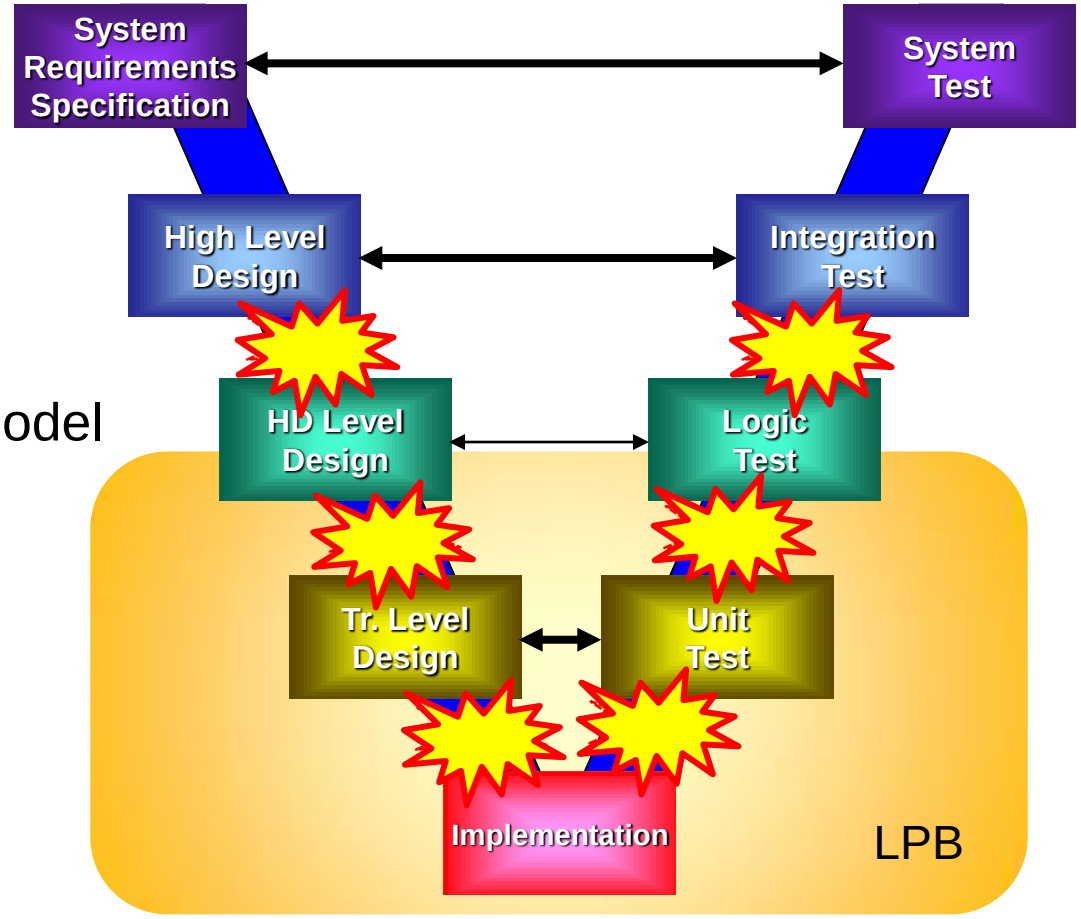
- V-Model
  Ideal: Should work
  Real: Gaps exist

- Design/Verification
  Languages/Tools tackle

  ex.
  High Level Abstraction Model
  High Level Synthesis
  Formal Verification

  LPB format (IEEE 2401)

- Little Digital Issue
  but Analog Ones

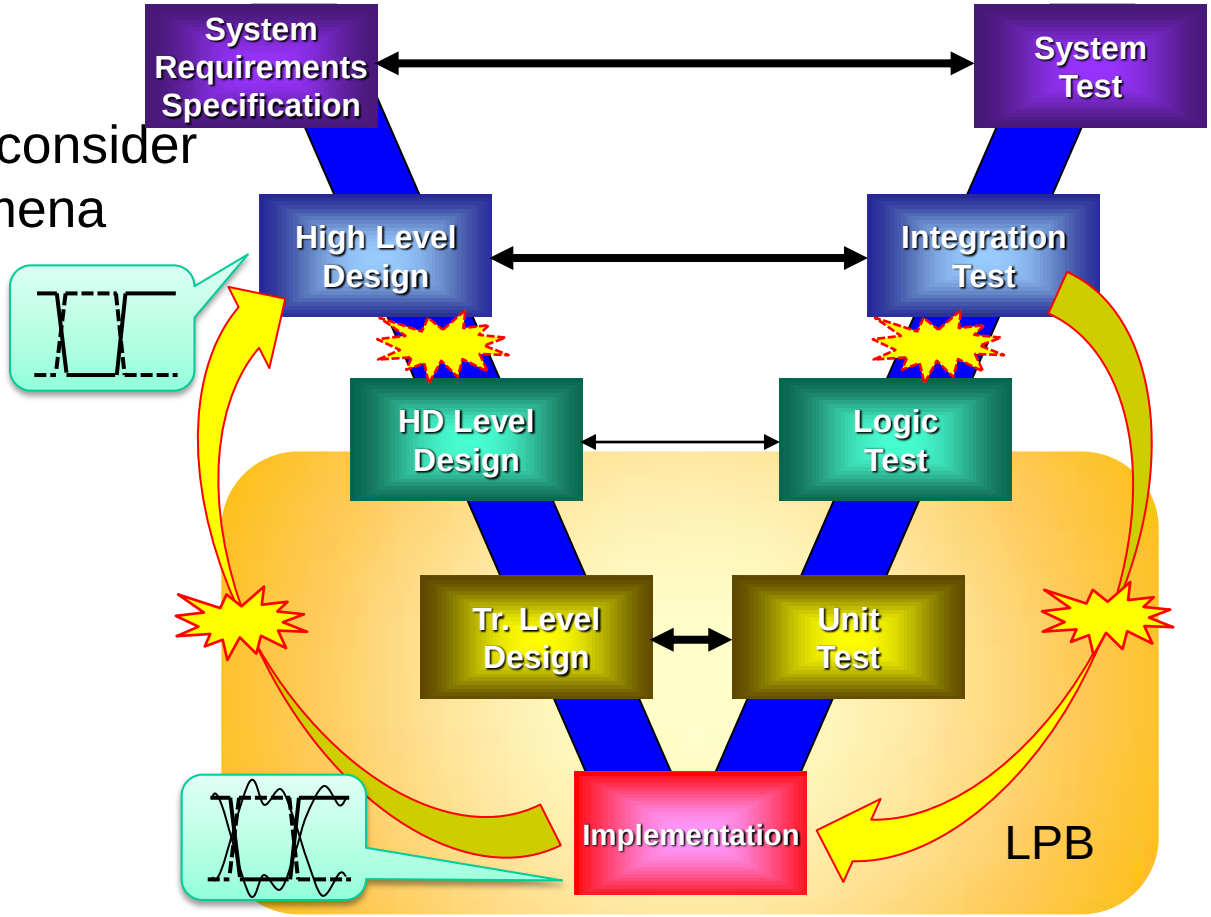


System Design

- Analog Issues

  - Found at final stage

- Because
  Current HLD could consider little analog phenomena
  - Overshoot
  - Undershoot
  - Eye Opening
  - Jitter
  - Vdrop
  - Thermal
  :



System Design

- Potential Solution

- Library/IP w/Analog Info.
  for High Level Design
- Common Language
  which cover different stages

- That enables
  Feed Forward Design
  Short TAT
  Margin Less
  High Accuracy