IBIS-AMI modeling and simulation for PAM3 signaling in USB4 V2/Gen4 Systems

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KEYSIGHT TECHNOLOGIES

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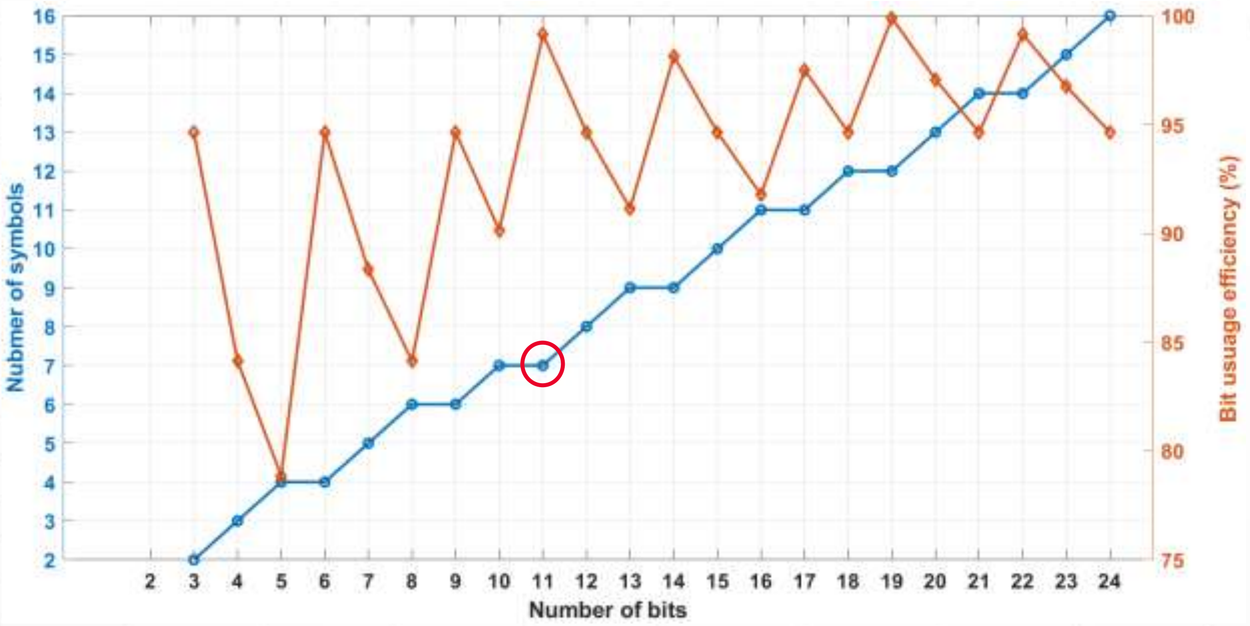
Outline

- Introduction to USB4 V2/Gen4
- PAM3 signaling defined in USB4
- IBIS-AMI modeling and simulation for PAM3 signaling
- PAM3 eye measurements
- Examples of PAM3 simulation
- Summary

Introduction to USB4 V2/Gen4

- Data rate at 40Gbps
- PAM3 signaling with 11 binary bits to 7 ternary symbols (trits) conversion (11B7T)
- Target pre-FEC trit error rate (TER) at 10^{-8}
- 139 ($=3^7-2^{11}$) out of 3^7 (=2187) 7-trit combinations are not used
- 11B7T has high bit usage efficiency with low latency compared to other PAM3 mapping schemes



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11B7T Binary to Ternary Conversion

Step-1

Divide the 11-bit source to 4 groups using *Table 4-51*

Step-2

If A ≠ 11b

a. Convert A to A’ using *Table 4-52*

b. Convert B to B’, C to C’ and D to D’ using *Table 4-53*

c. Construct the ternary symbol using *Table 4-54*

Else

a. Convert C to C’ and D to D’ using *Table 4-53*

b. Depending on the value of B, construct the Ternary Symbol using *Table 4-55*

Note: If the symbol is a Control Symbol, replace trits 6:4 in the ternary symbol from 210t to 111t.

Note: A receiver shall convert from ternary to binary using the same tables. When the receiver detects 111t in trits 6:4 of a symbol, it shall replace trits 6:4 with 210t.

Table 4-51. Binary Symbol Groups

Group	A	B	C	D
Bits	10:9	8:6	5:3	2:0

Table 4-52. Conversion of 2 Bits to 1 Trit

Binary	00	01	10
Ternary	0	1	2

Table 4-53. Conversion of 3 Bits to 2 Trits

Binary	000	001	010	011	100	101	110	111
Ternary	00	01	02	10	12	20	21	22

Table 4-54. Ternary Symbol Groups

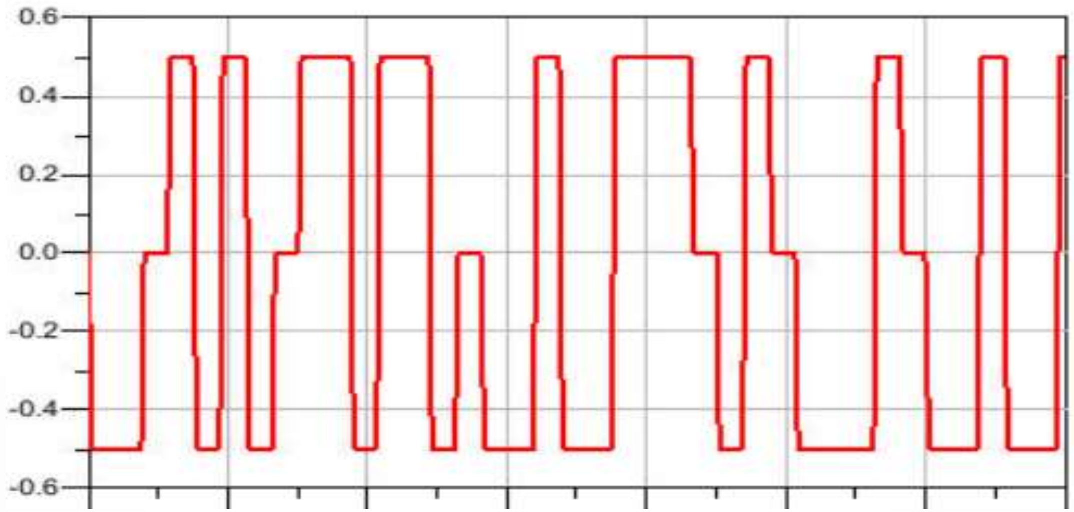
Trits	6	5:4	3:2	1:0
Group	A’	B’	C’	D’

Table 4-55. Constructing Ternary Symbol when A=11b

B	000	001	010	011	100	101	110	111
6	0t	1t	2t	0t	1t	2t	0t	2t
5:4	C’	C’	C’	C’	C’	C’	11t	11t
3:2	D’	D’	D’	11t	11t	11t	C’	C’
1:0	11t	11t	11t	D’	D’	D’	D’	D’

PAM3 AMI Simulation Flow

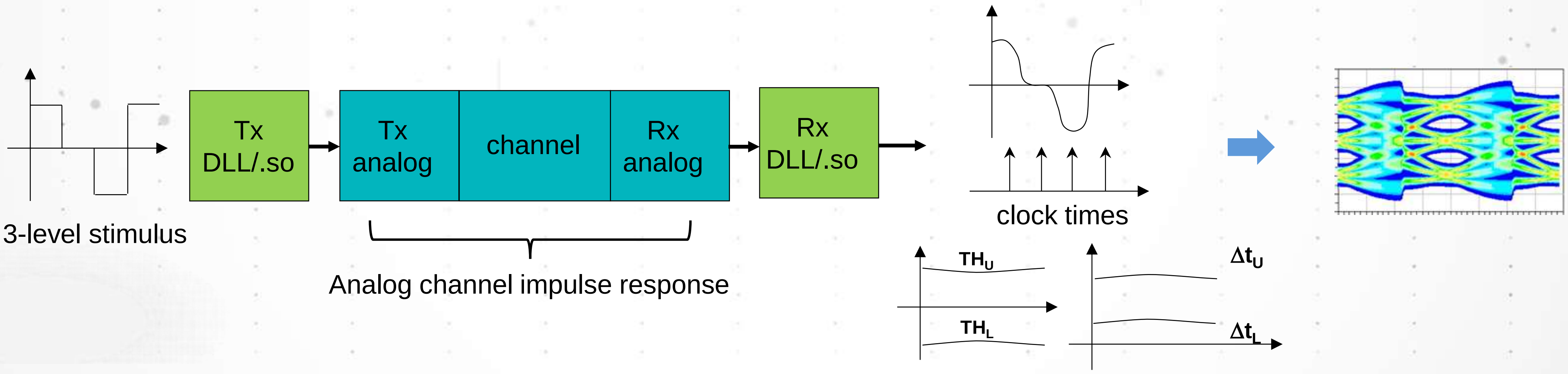
- TX input stimulus is a 3-level square wave. Voltages of the three levels are -0.5V, 0V and 0.5V, representing PAM3 symbols 0, 1 and 2, respectively.
- Simulator converts bit sequence to trit sequence using 11B7T mapping, constructs the corresponding 3-level TX input waveform, and applies TX jitter to transition edges.
- Baud rate = 7/11 of bit rate



PAM3 TX input waveform

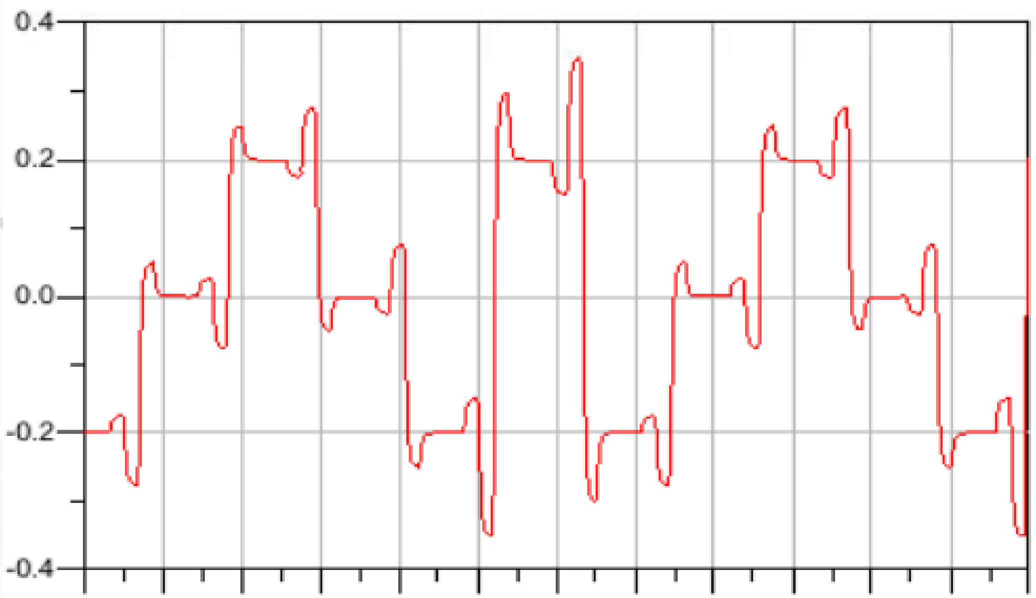
PAM3 AMI Simulation Flow (cont'd)

- TX output is a PAM3 waveform
- RX input is the convolution of TX output and the analog channel impulse response
- RX output is a PAM3 waveform
- RX also returns clock times, upper and lower slicer thresholds and sampling time offsets

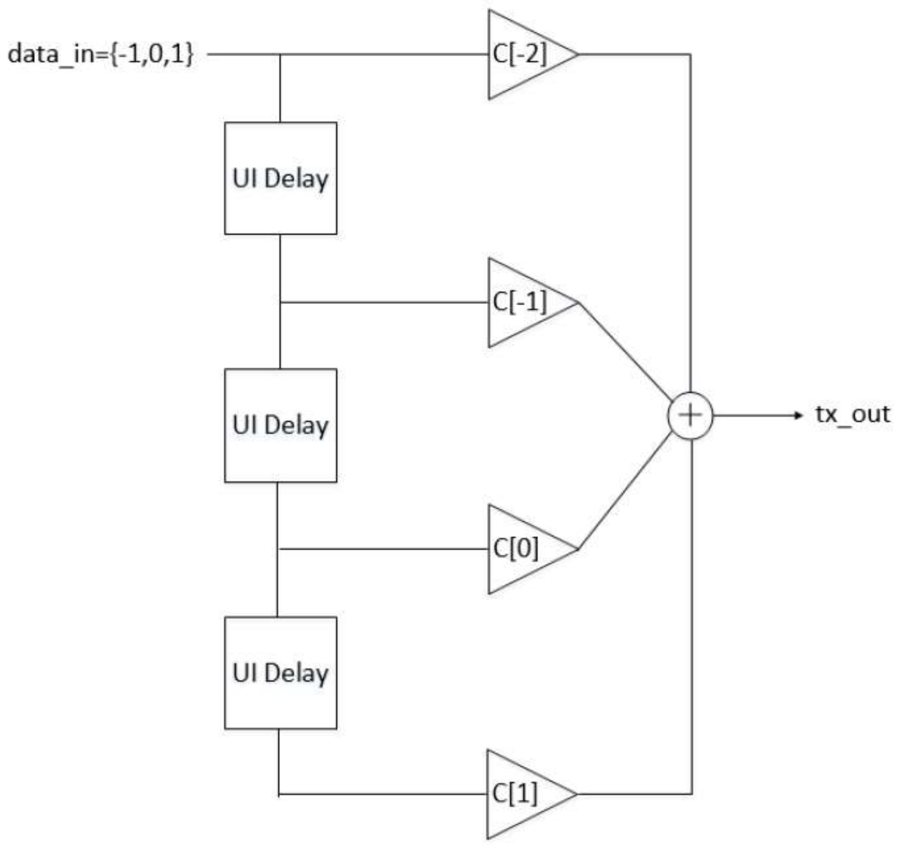


TX Equalization

- USB4 V2 defines a 4-tap UI-spaced finite-impulse-response (FIR) filter
  - 2 pre-cursors, 1 main-cursor and 1 post-cursor
- 42 standard presets are specified
  - An example of waveform with preset 30 is shown



TX output waveform with preset 30



TX Jitter

- USB4 V2 defines a set of TX jitter parameters
  - UJ: peak-to-peak uncorrelated total jitter (at TER = 1e-8)
  - UDJ: peak-to-peak uncorrelated deterministic jitter
  - EVEN_ODD: peak-to-peak even-odd jitter
- Equivalent AMI TX jitter parameters

$$Tx\_Jitter\ mean1_{Dual-Dirac} = -\frac{UDJ}{2}$$

$$Tx\_Jitter\ mean2_{Dual-Dirac} = \frac{UDJ}{2}$$

$$Tx\_Jitter\ sigma_{Dual-Dirac} = \frac{UJ - UDJ}{2}\frac{1}{5.49}$$

$$Tx\_DCD = \frac{EVEN\_ODD}{2}$$

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TX Jitter (cont'd)

- Jitter is applied to switching times of transitions in TX input waveform

$$t(n) = nT + (-1)^n \cdot Tx\_DCD + \mu(n) + A_{SJ} \cdot cos(\omega_{SJ} \cdot nT)$$

- $t(n)$: switching time of the n^{th} symbol

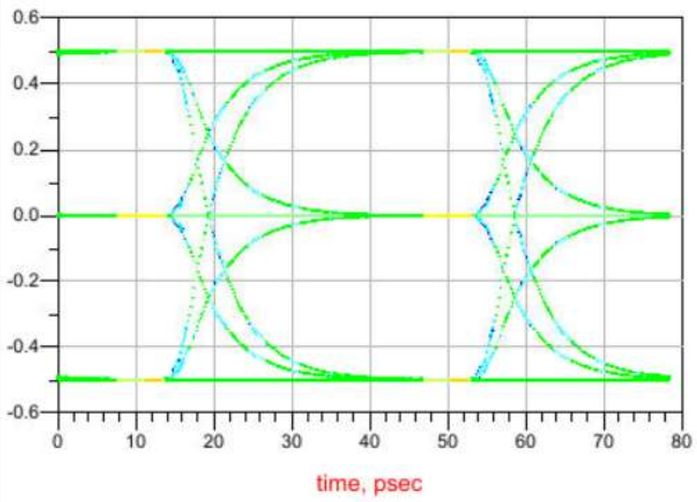
  T: symbol UI

  $\mu(n)$: Dual-Dirac jitter at the n^{th} symbol

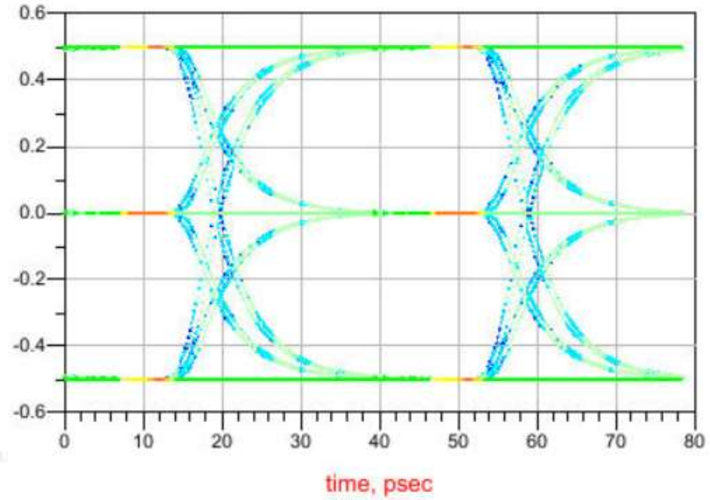
  A_{SJ}: SJ amplitude

  ω_{SJ}: SJ frequency

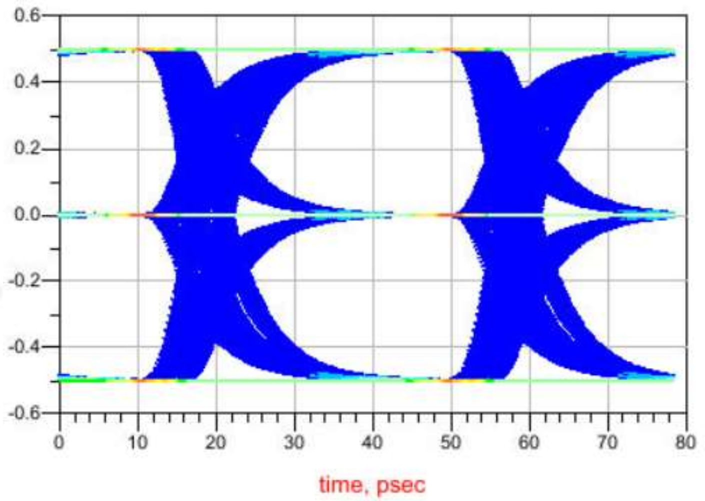
TX Jitter (cont'd)



TX output eye with no TX jitter



TX output eye with 0.02UI EVEN_ODD TX jitter



TX output eye with 0.17UI UJ and 0.075UI UDJ TX jitter

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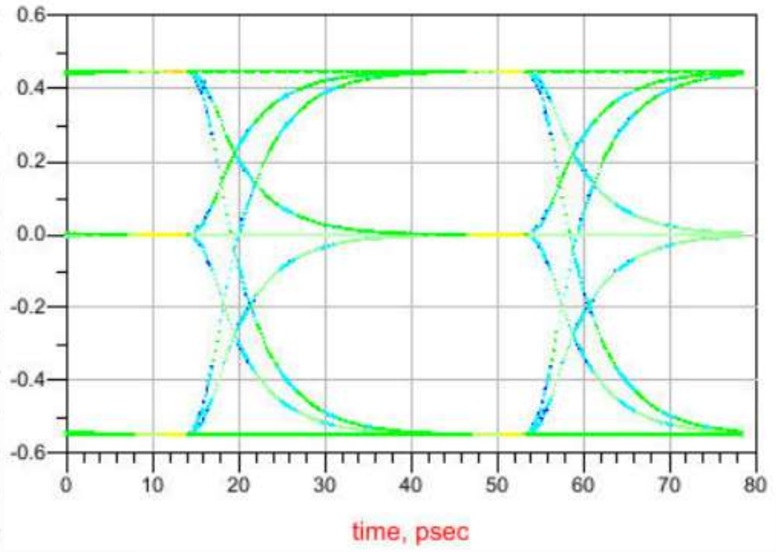
TX Levels Mismatch

- Due to device nonlinearity voltage separations between the three PAM3 levels at the TX output may be nonuniform

$$TX\_LEVELS\_MISMATCH = \min\{\frac{V_2 - V_1}{\Delta}, \frac{V_1 - V_0}{\Delta}\}$$

$V_0, V_{\mathbf{1}}$ and $V_{\mathbf{2}}$: mean voltages of symbols 0, 1 and 2

$$\Delta = \frac{(V_2 - V_0)}{2}$$



- TX output eye with 0.9 TX_LEVELS_MISMATCH
- Lower eye is taller than upper eye due to level mismatch

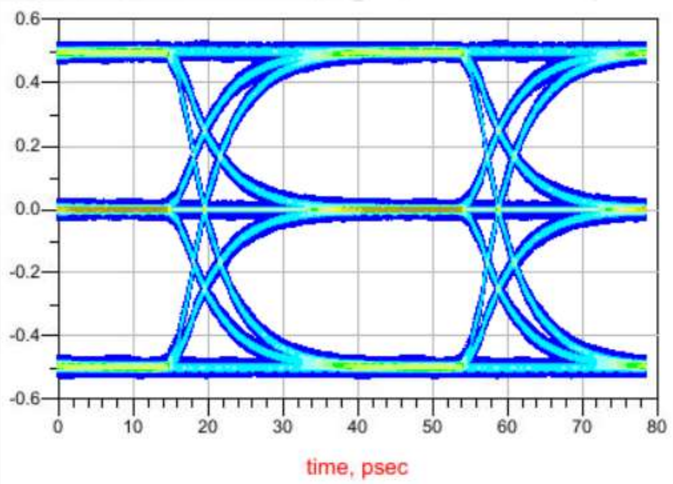
TX Signal-to-noise-and-distortion-ratio

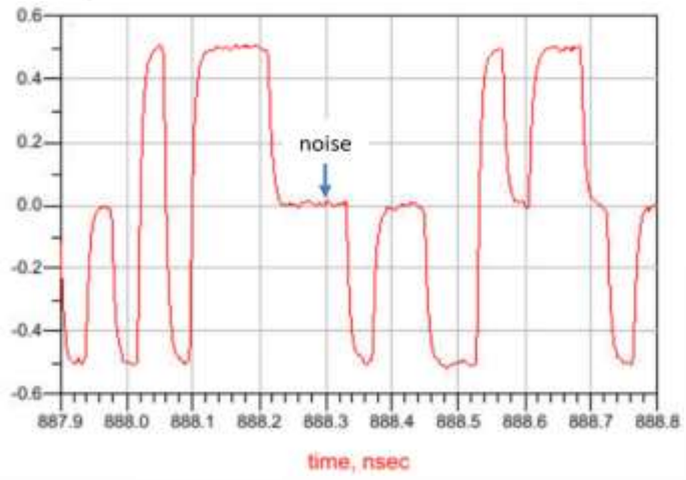
$$TX\_SNDR = 20 \cdot log_{10} \frac{P_{max}}{\sqrt{\sigma_e^2 + \sigma_n^2}}$$

P_{max}: maximum value of the linear fit pulse response

σ_e: RMS of the residual nonlinear distortion in the TX output after excluding the leading order effect of levels mismatch

σ_n: RMS of the additive noise in the TX output

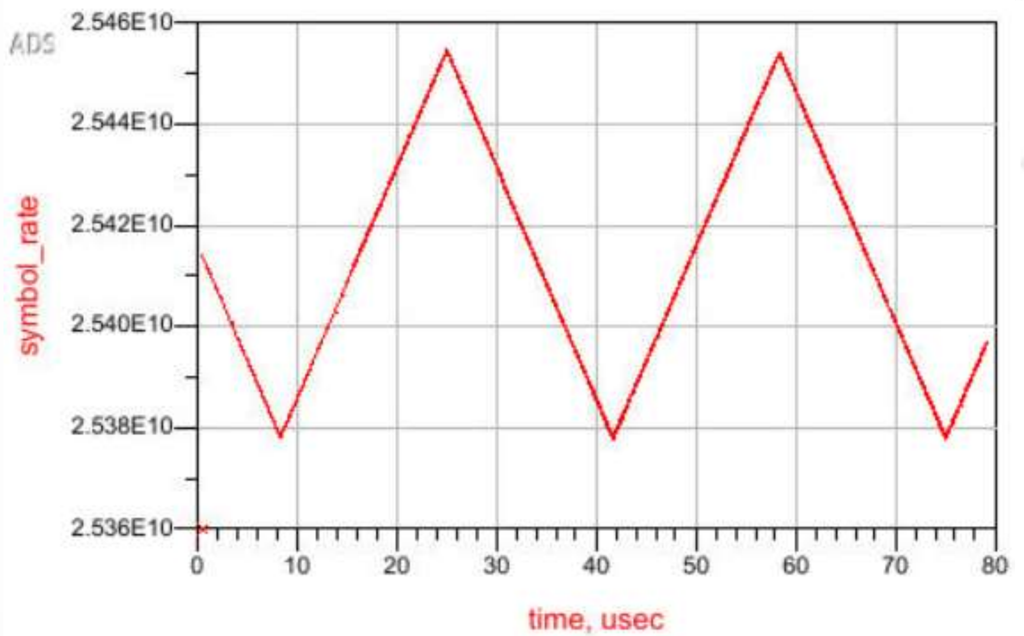




TX output eye and waveform with 25dB TX_SNDR

TX Spread Spectrum Clocking (SSC)

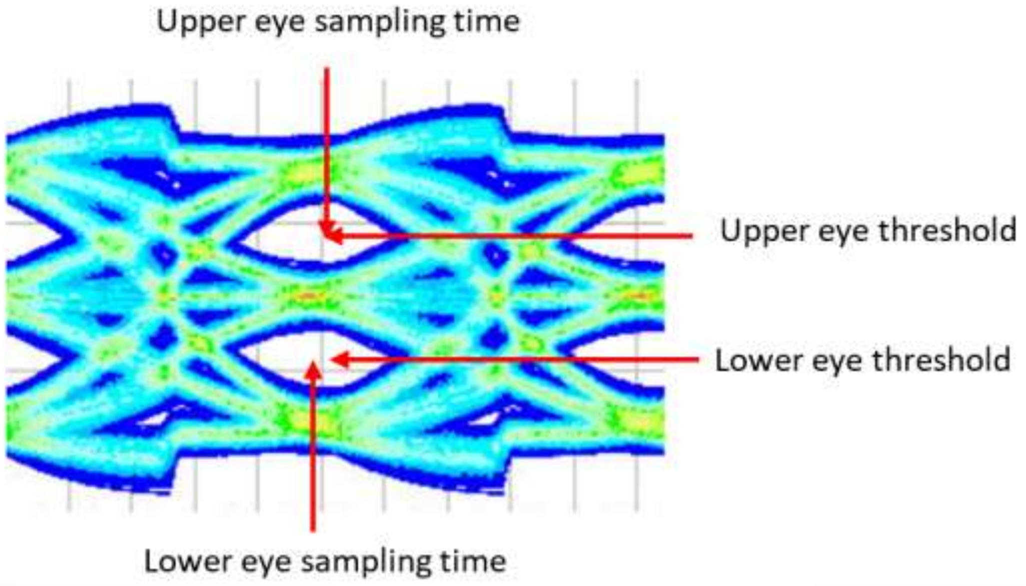
- SSC is applied to reduce EMI
- Frequency of the TX output signal drifts gradually and periodically near the nominal frequency



Instantaneous symbol rate in TX output with 0.3% SSC_DOWN_SPREAD_RANGE and 30kHz SSC_DOWN_SPREAD_RATE

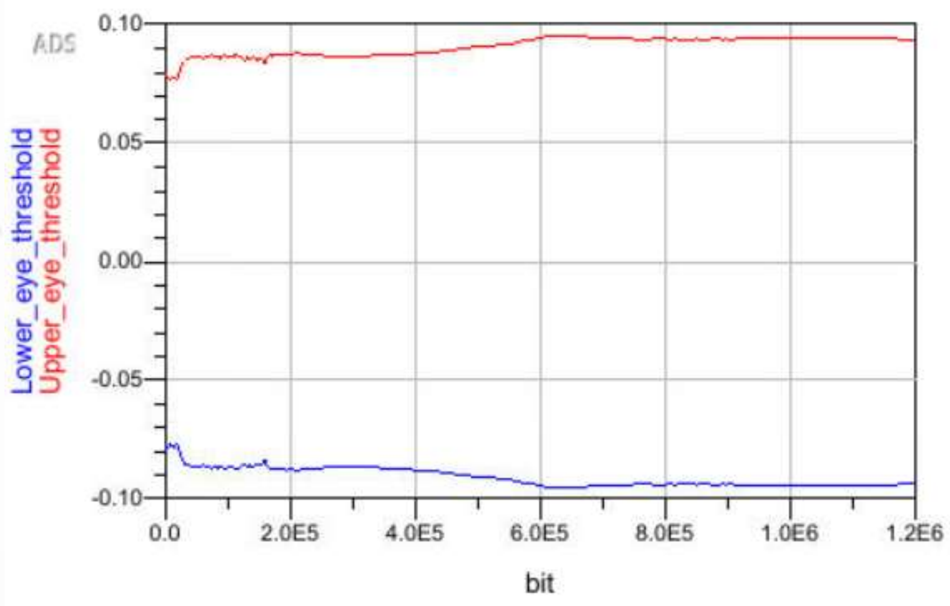
RX Slicer Thresholds and Timing Skew

- RX uses two slicers to detect signal symbol level
- RX model returns a pair of upper and lower slicer thresholds after each GetWave
- Sampling times of upper and lower slicers can be different
- RX model returns a pair of upper and lower slicer sampling time offsets after each GetWave



RX Slicer Thresholds and Timing Skew (cont'd)

- Upper eye sampling times = clock times + upper eye offset
- Lower eye sampling times = clock times + lower eye offset
- Slicer thresholds and offsets can vary from GetWave to GetWave due to adaptation



Slicer threshold waveforms

PAM3 Eye Measurements

- TER and bathtub curves are measured individually for upper and lower eyes

Eye	Traces	Sampling time
Upper	$v_1(t)$-$TH_U(t)$ and $v_2(t)$-$TH_U(t)$	$t_{clk}(n)+\Delta t_U(n)+UI/2$
Lower	$v_0(t)$-$TH_L(t)$ and $v_1(t)$-$TH_L(t)$	$t_{clk}(n)+\Delta t_L(n)+UI/2$

$v_0(t)$, $v_1(t)$ and $v_2(t)$: waveform segments of expected level 0, level 1 and level 2 symbols

$TH_U(t)$ and $TH_L(t)$: instantaneous upper and lower slicer thresholds

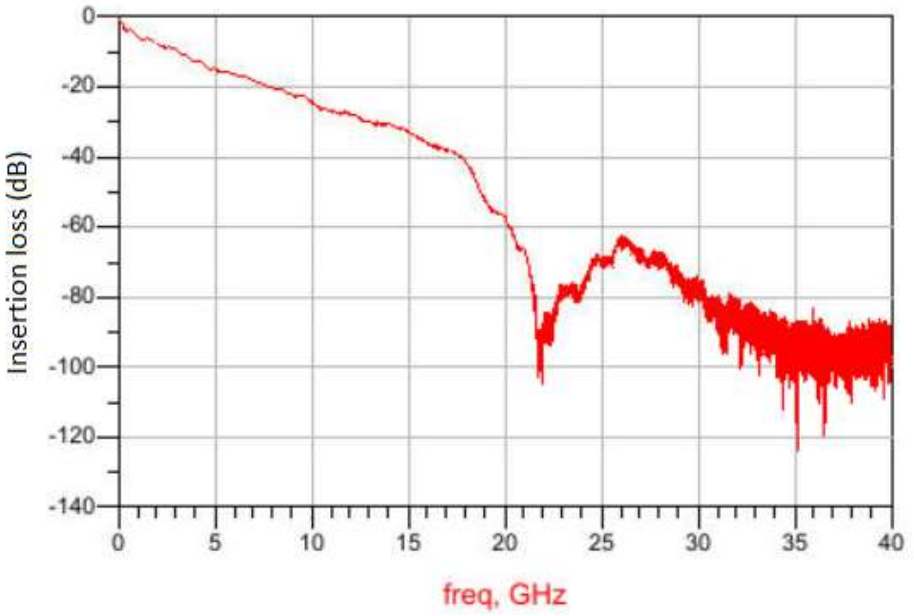
$t_{clk}(n)$: clock time of the n^{th} symbol

$Dt_U(n)$ and $Dt_L(n)$: upper and lower slicer sampling time offsets of the n^{th} symbol

Symbols in the same GetWave block share the same TH_U, TH_L, Dt_U and Dt_L values returned by RX after that GetWave call

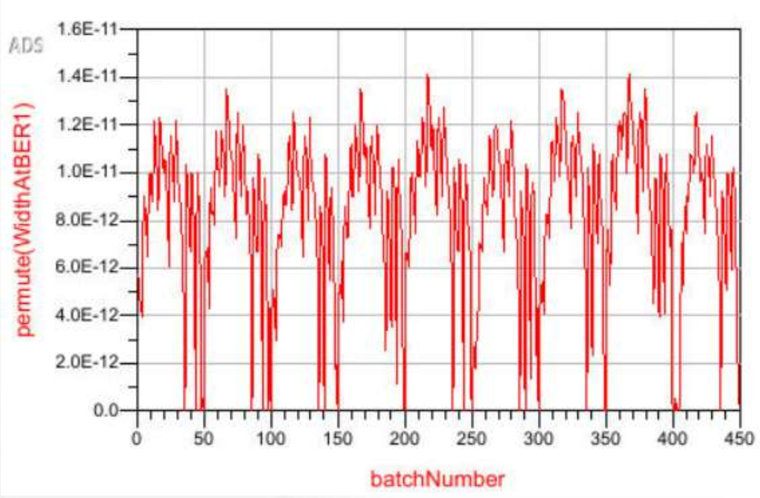
Examples of PAM3 simulation

- 40Gbps data rate (25.45G PAM3 baud rate)
- 29dB channel insertion loss (including host, cable, and device) at 12.8 GHz
- TX: 4-tap FFE with two pre-cursors and one post-cursor and 50 presets (including 42 standard presets)
- RX: 3-pole-2-zero CTLE with 9 presets, 10-tap adaptive DFE, and 2nd order CDR

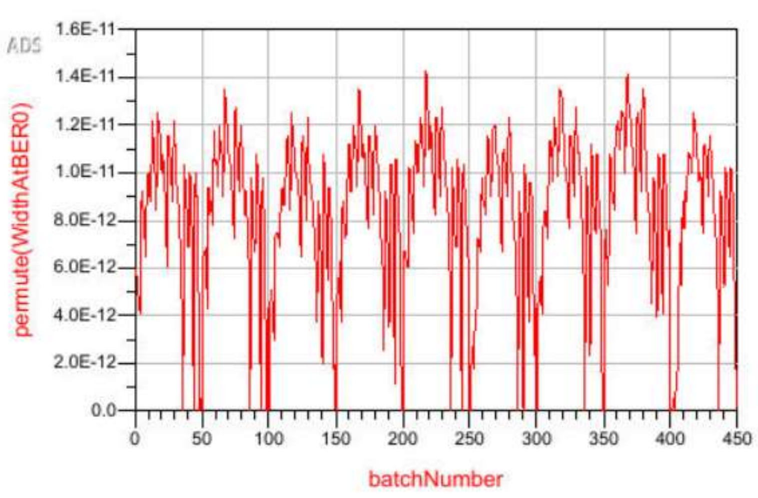


TX FFE and RX CTLE Optimization

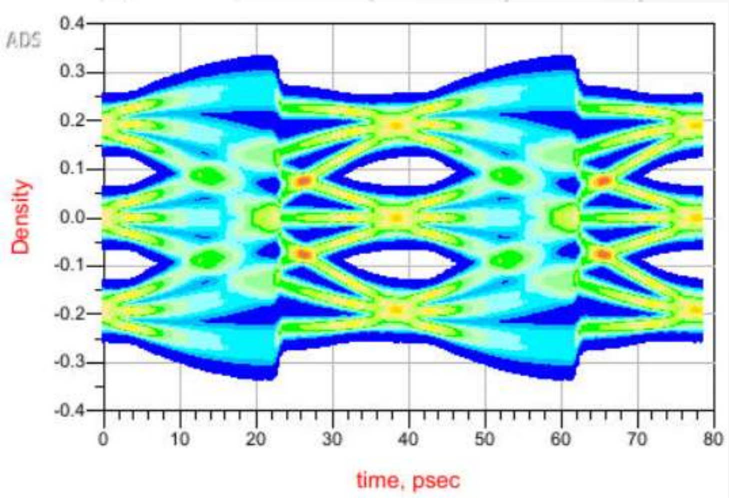
- Sweep 450 combinations of 50 TX FFE presets and 9 RX CTLE presets
- At each sweep point RX model internally optimizes DFE taps
- Run statistical simulation to compute RX output eye widths at 1e-8 TER
- Optimal combination: TX FFE preset 16 and RX CTLE preset 4



RX output upper eye width vs sweep index



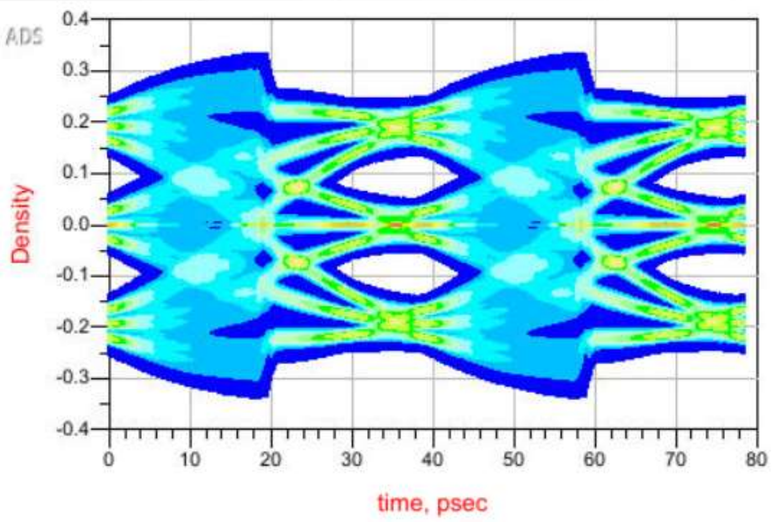
RX output lower eye width vs sweep index



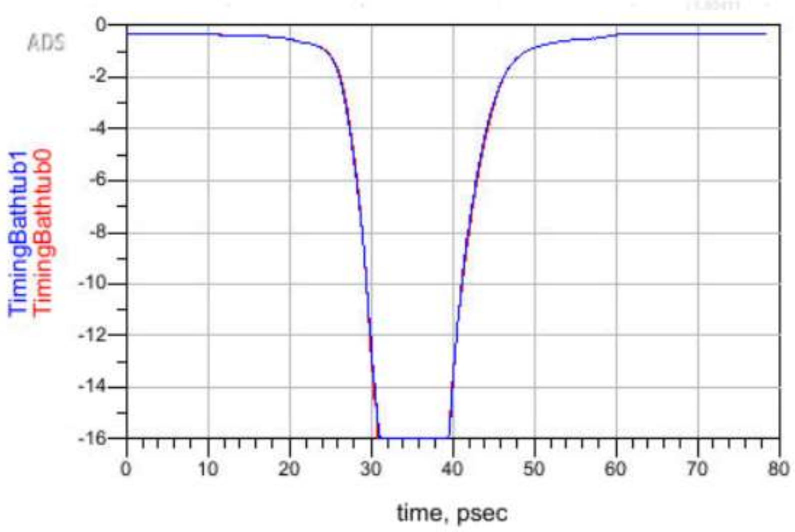
Statistical RX output eye with optimal TX FFE and RX CTLE

RX DFE Adaptation

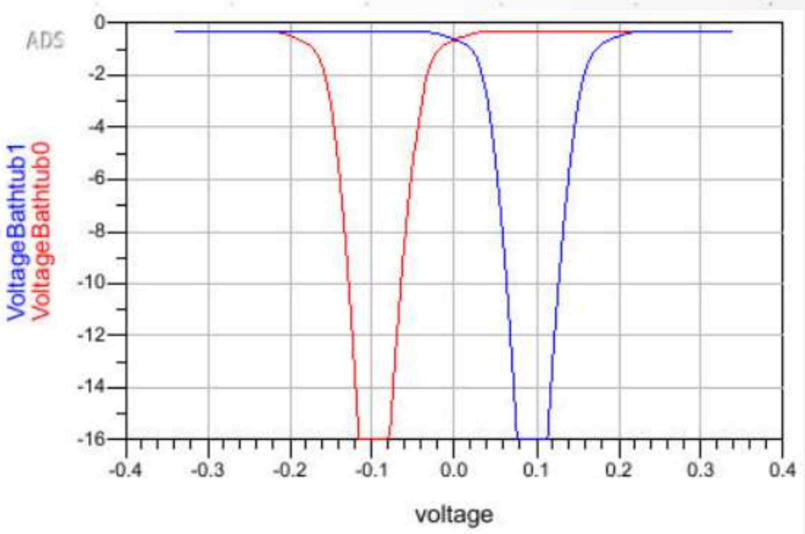
- Bit-by-bit simulation of 2M PAM3 symbols
- Optimal TX FFE and RX CTLE



RX output eye



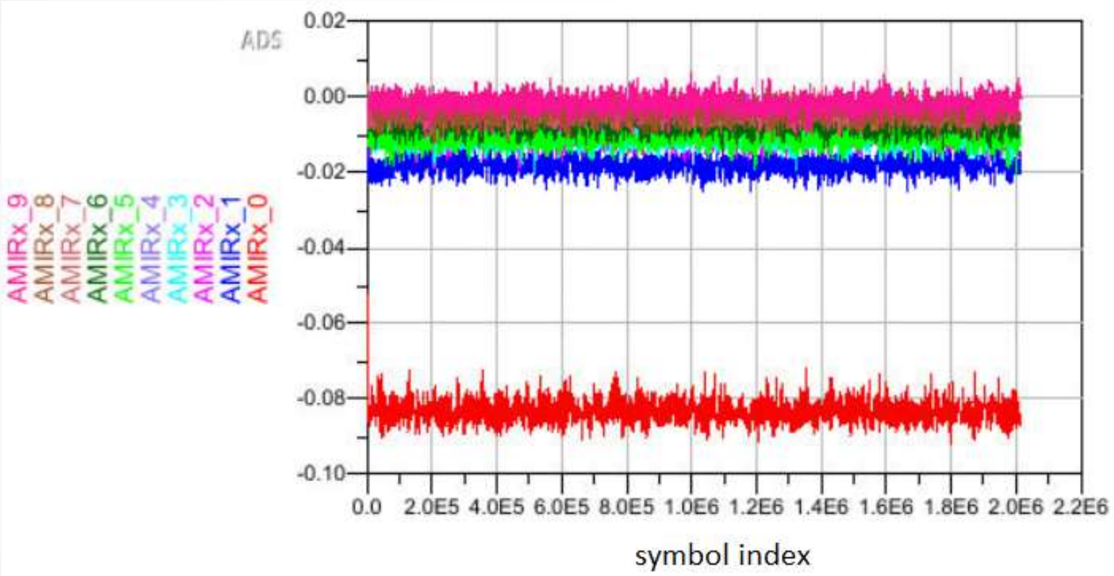
RX output timing bathtub



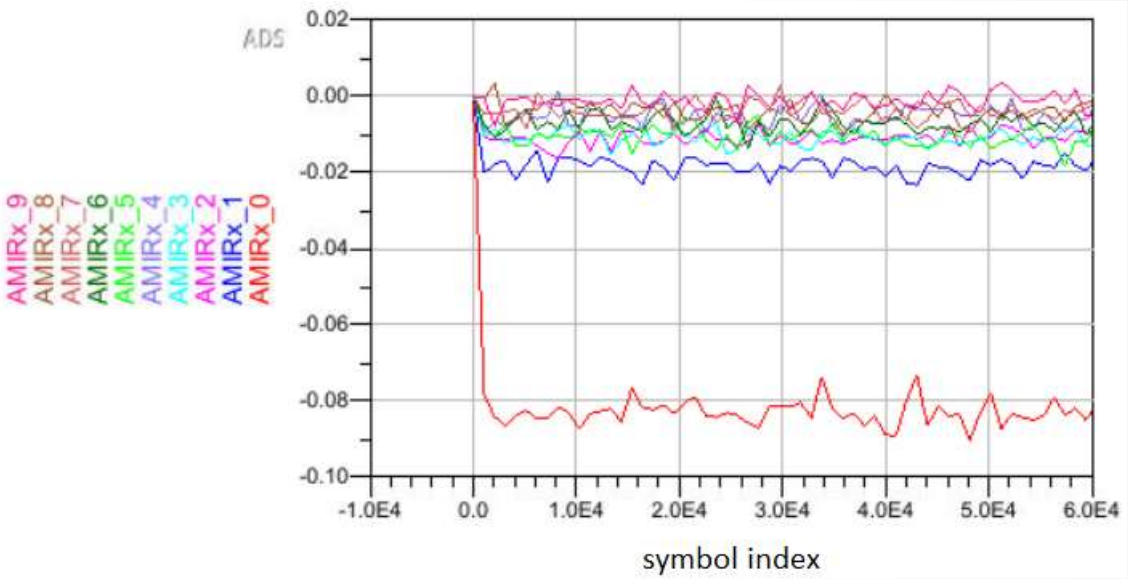
RX output voltage bathtub

- Results are consistent with those of statistical simulation

RX DFE Adaptation (cont'd)



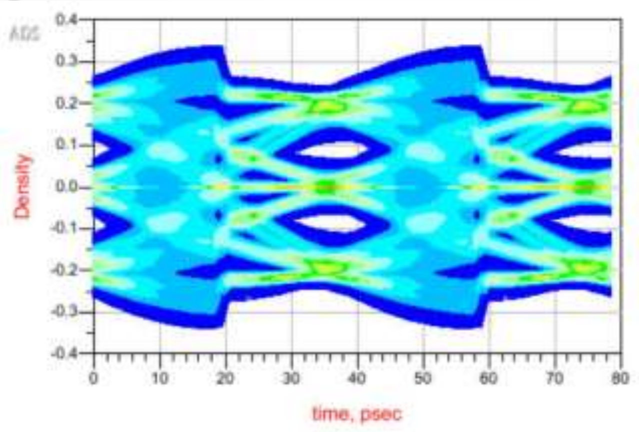
RX DFE tap waveforms



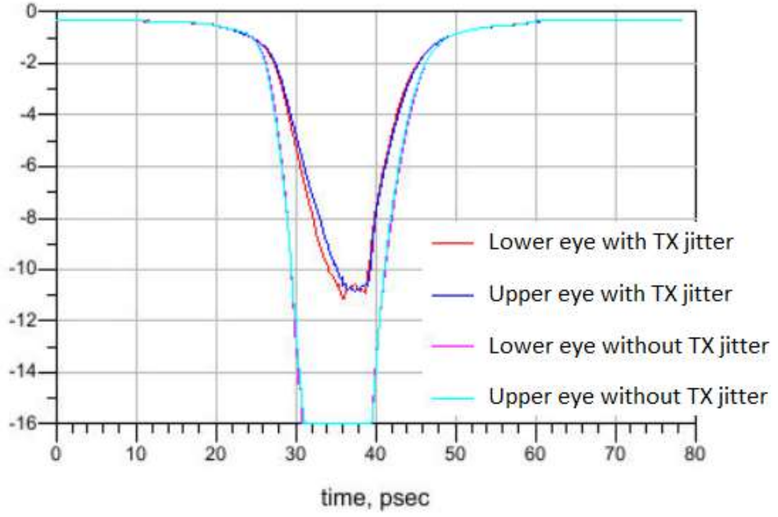
Zoomed-in view of RX DFE tap waveforms

Impact of TX Jitter

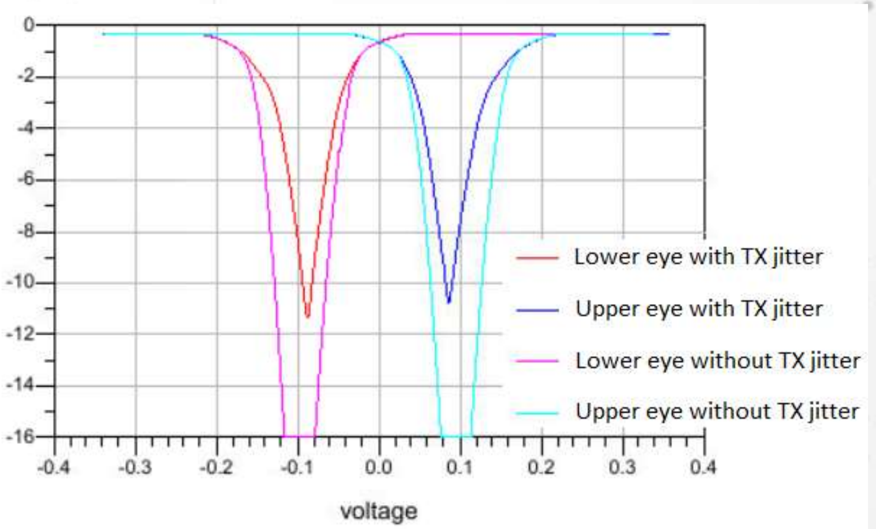
- UJ=0.17UI, UDJ=0.075UI, EVEN_ODD=0.02UI
- 2M symbols
- Optimal TX FFE and RX CTLE
- RX output eye widths and heights are reduced by TX jitter



RX output eye



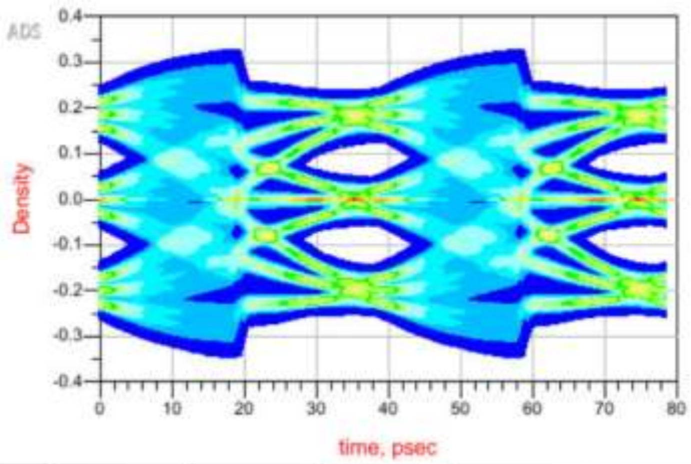
RX output timing bathtub



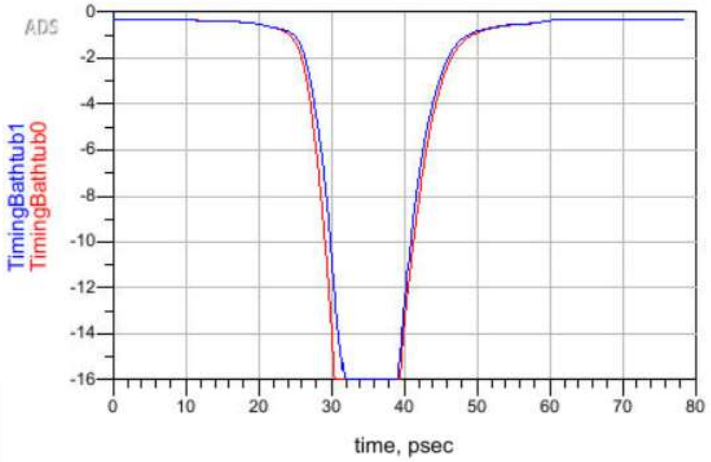
RX output voltage bathtub

Impact of TX Levels Mismatch

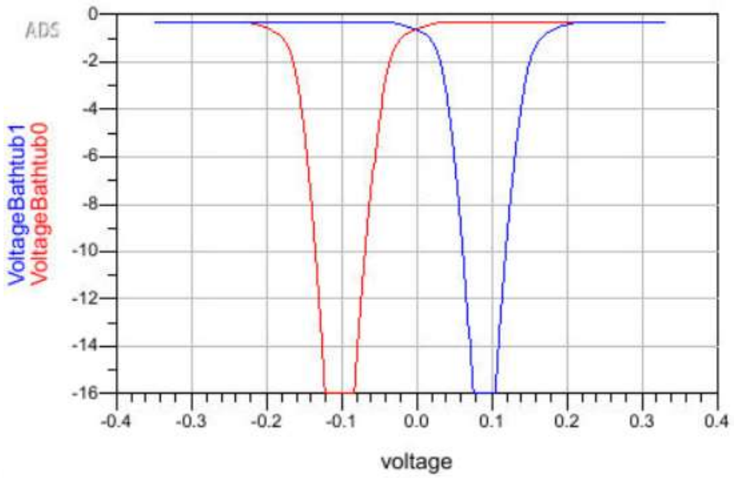
- TX_LEVELS_MISMATCH=0.975
- 2M symbols
- Optimal TX FFE and RX CTLE
- RX output upper eye is slightly smaller than the lower eye both horizontally and vertically due to level mismatch



RX output eye



RX output timing bathtub

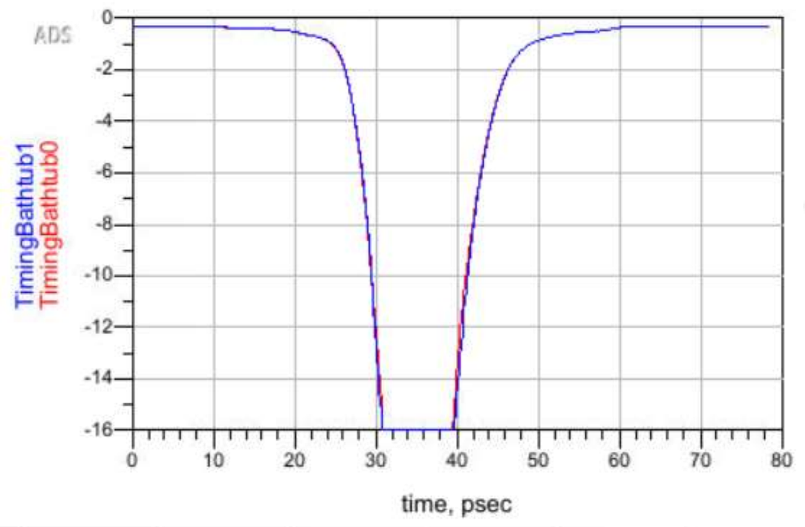


RX output voltage bathtub

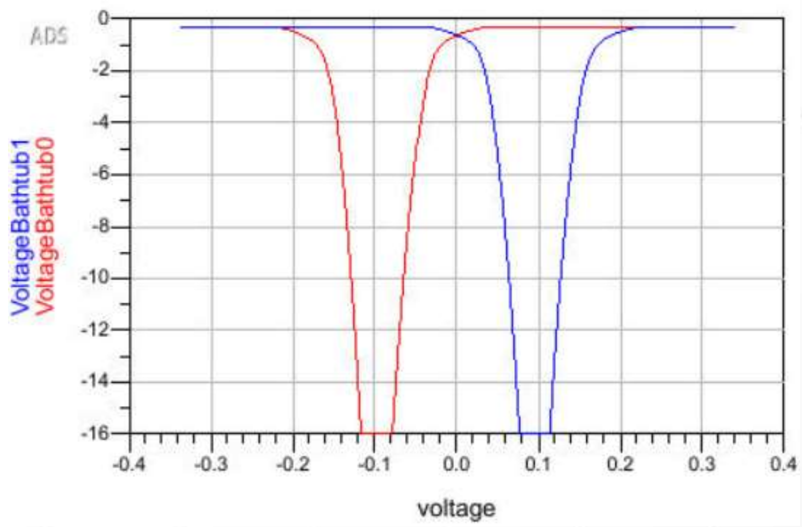
KEYSIGHT TECHNOLOGIES

Impact of TX Noise

- TX_SNDR=32.5dB
- 2M symbols
- Optimal TX FFE and RX CTLE
- RX output results are almost identical to those without TX noise
- TX noise impact on the RX side is limited due to high channel loss



RX output timing bathtub

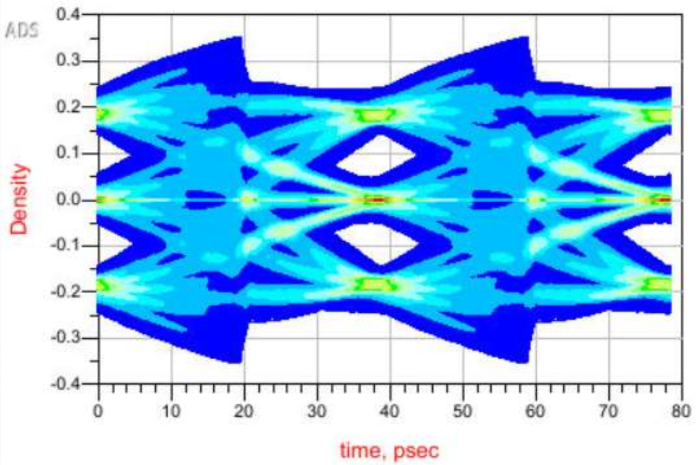


RX output voltage bathtub

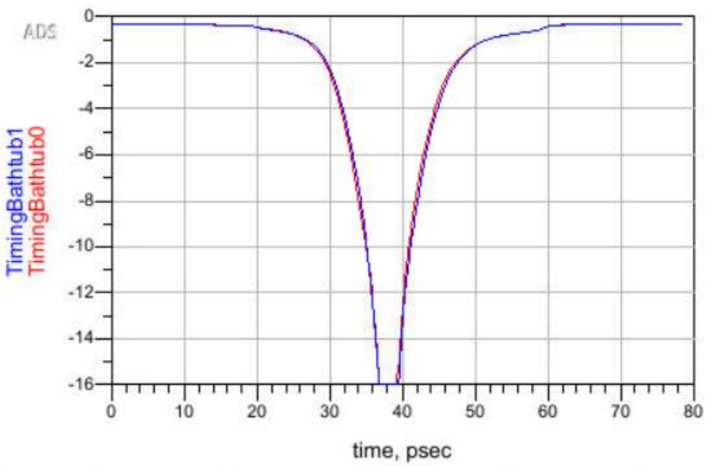
KEYSIGHT TECHNOLOGIES

Impact of TX SSC

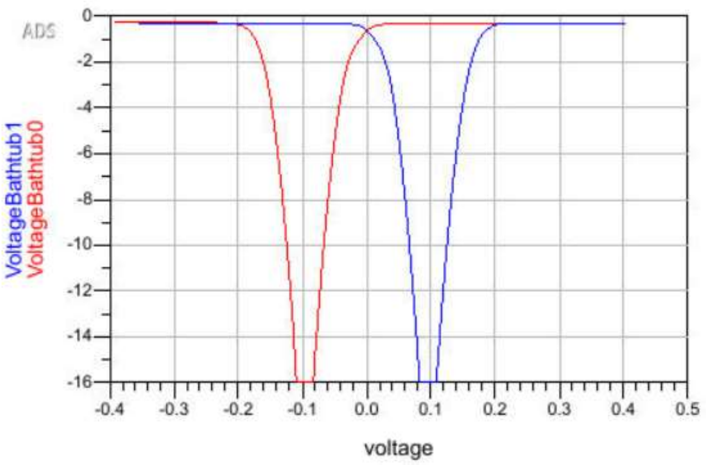
- SSC_DOWN_SPREAD_RANGE=0.3%, SSC_DOWN_SPREAD_RATE=30kHz
- 2M symbols
- Optimal TX FFE and RX CTLE
- SSC degrades the RX CDR performance, leading to reduced timing and voltage margins



RX output eye



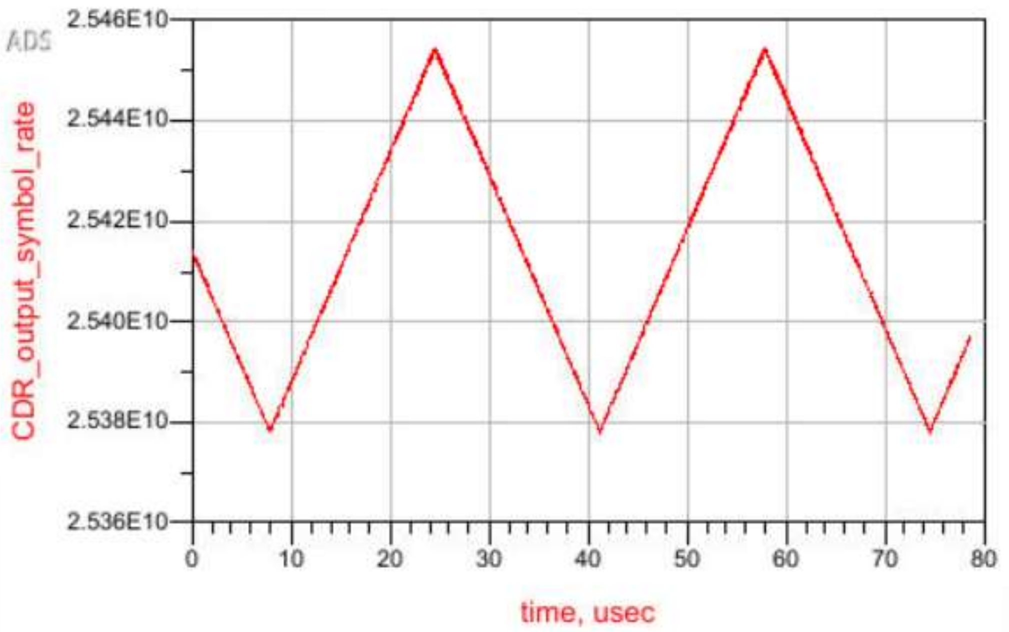
RX output timing bathtub



RX output voltage bathtub

Impact of TX SSC (cont'd)

- Instantaneous symbol rates in RX CDR output is computed using clock_times returned by RX GetWave. High frequency CDR jitter is filtered out by a low-pass filter.
- RX CDR output symbol rate profile matches that of the TX output
- RX CDR tracks the SSC frequency drift in the TX output signal



Instantaneous symbol rate in RX CDR output

Summary

- IBIS-AMI methodology is applied to model and simulate PAM3 signals in USB4 V2 links
- The simulator processes the equalized waveform to provide TER, eye diagrams, and horizonal and vertical bathtub curves
- The approach is verified through simulations of PAM3 signaling of a 29dB channel

Thank you!