Update on BIRD226: PSIJ Sensitivity

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PSIJ = **P**ower **S**upply **I**nduced **J**itter

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intel

Presenter

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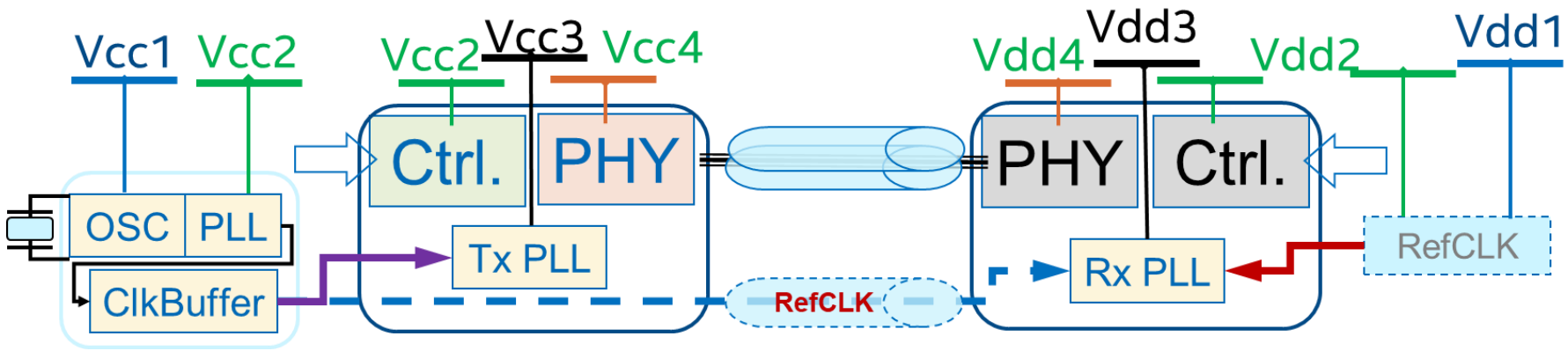
Executive Summary

Summary:

- BIRD226 focuses on including all PSIJ contributions from all PI noises, of each power supply rail, and all power rails, to all involved ckt blocks, for an interface operating in a particular protocol, supporting system level PI and SI co-simulation / design.



BIRD226 for PI & SI Co-sim. Major Steps

1. SI simulation sets up all involved power supplies ideal at Vnom/Vmin/Vmax, (which is equivalent to “disabling” of BIRD220, and/or [ISSO PU] & [ISSO PD], and [Composite Current].).
2. Takes into consideration the total PI noises of each power supply rail, including (1)self-noise, (2)coupling noise and (3)power management relevant noise; while taking care of multiple power supplies to one IO interface simultaneously.
3. Takes into consideration the jitter impact to all relevant ckt blocks from the total PI noise of each power supply rail, which will be calculated with defined/ IEEE published algorithm for PSIJ.
4. All involved power rails’ jitter values to a concerned IO interface, can be super-positioned upon the eye-diagram resulting from SI simulation with ideal power supplies setup, or super-positioned upon Tx_Dj or Rx_Dj in IBIS-AMI.

PSIJ Sensitivity Derivation

- Set up VCC_m, all other powers at their own Vtyp, while sweeping f, get jitter impact
  - *VCC_m= Vtyp + A*sin(2*Pi*f),*
  - *A=(Vmax-Vmin)/2,*
  - *$PSIJ\_VCC\_m\_ckt\_i(f)=Jitter_{PP}(f)/(2*A)$*
- VCC_m power supplies multiple CKT blocks

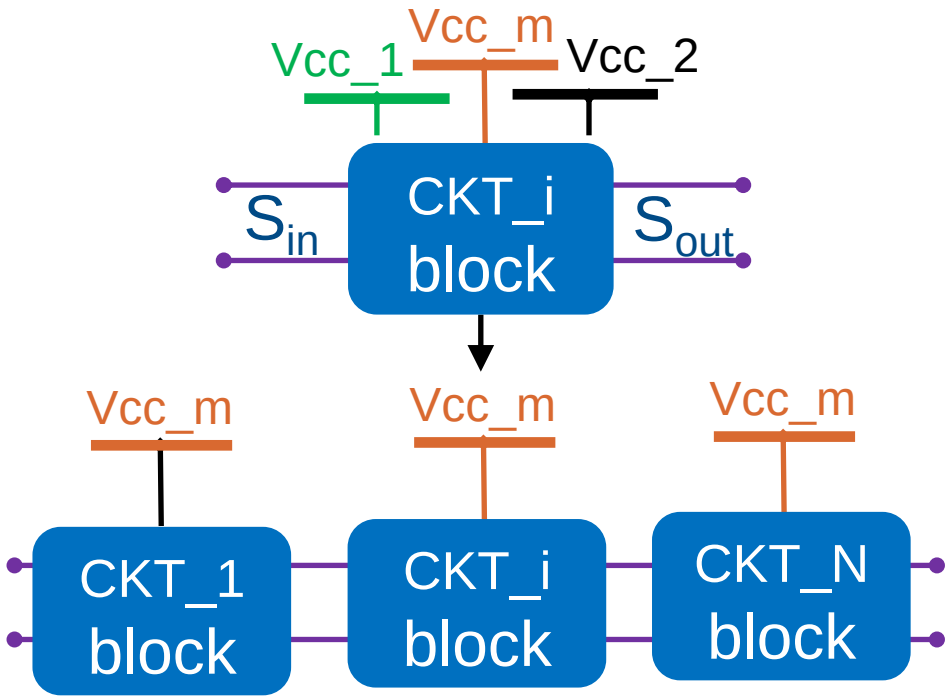
$JTF\_i(f)= Jitter\_of\_S_{out}\_i(f) / Jitter\_of\_S_{in}\_i(f)$

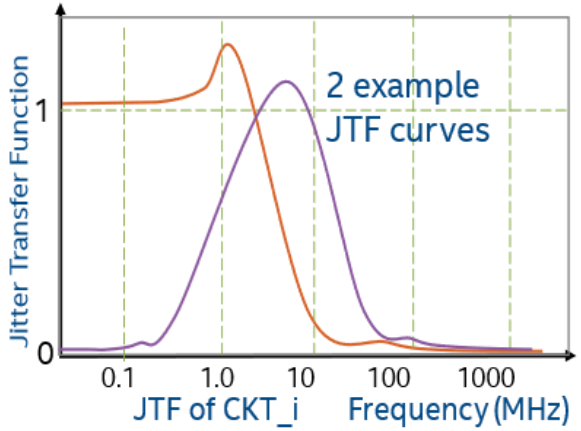
$PSIJ\_Vcc\_m\_i = PSIJ\_Vcc\_m\_(i\text{-}1) * JTF\_i +$

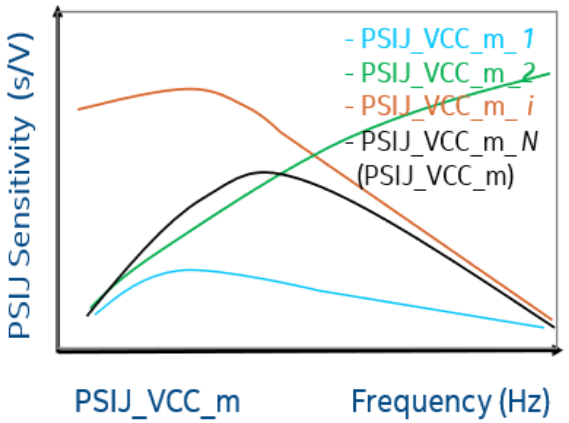
$PSIJ\_Vcc\_m\_CKT\_i, i \in 2, \ldots N$

$PSIJ\_Vcc\_m\_1 = PSIJ\_Vcc\_m\_CKT\_1$

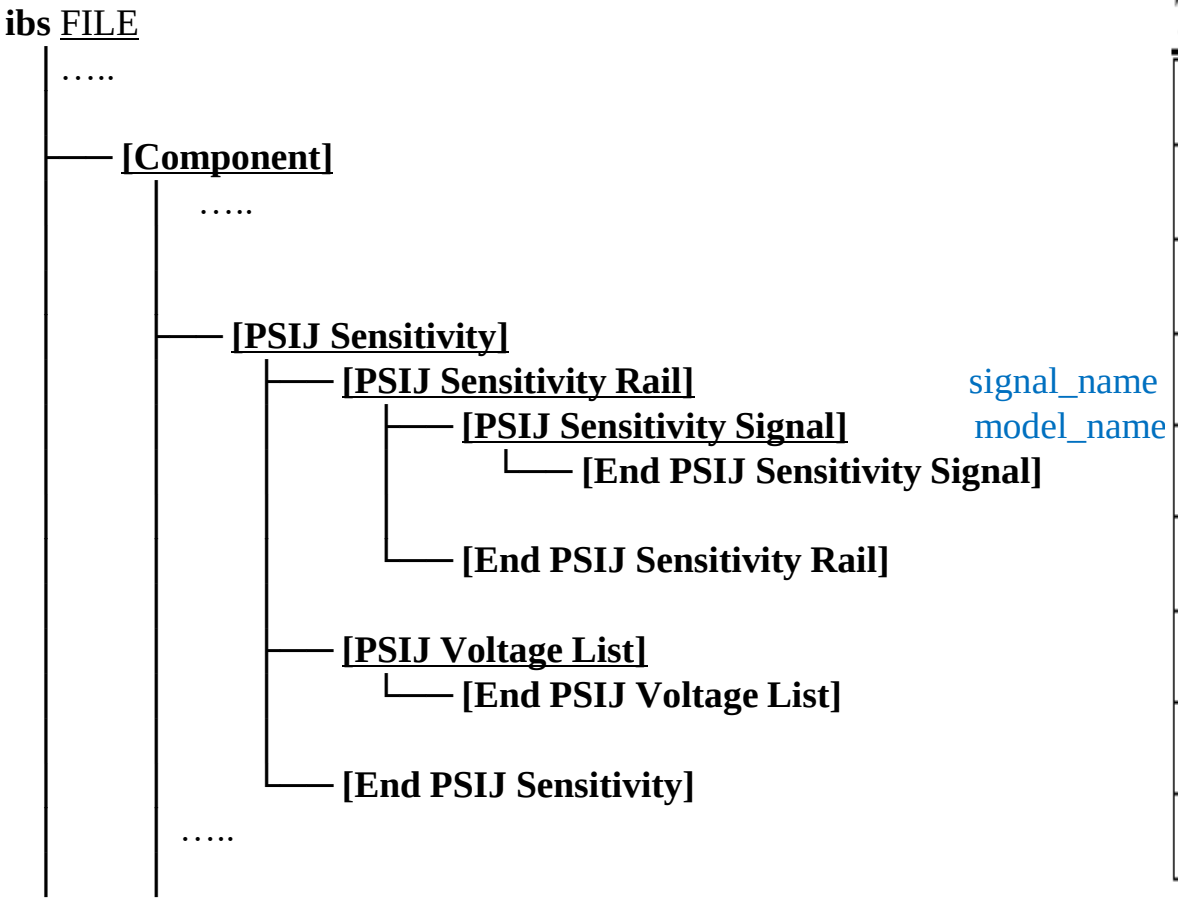
$PSIJ\_Vcc\_m = PSIJ\_Vcc\_m\_N$







[PSIJ Sensitivity] Tree Structure in .ibs



Tale 2- IBIS Keywords and Subparameters

Keywords or subparameter	Notes
[PSIJ Sensitivity]	It is optional in a .ibs file.
[PSIJ Sensitivity Rail]	It is optional in a .ibs file. It is required within [PSIJ Sensitivity].
[PSIJ Sensitivity Signal]	It is optional in a .ibs file. It is required within [PSIJ Sensitivity Rail].
[End PSIJ Sensitivity Signal]	It is optional in a .ibs file. It is required within [PSIJ Sensitivity Signal].
[PSIJ Voltage List]	It is optional in a .ibs file. It is required with [PSIJ Sensitivity Rail].
[End PSIJ Voltage List]	It is optional in a .ibs file. It is required with [PSIJ Voltage List].
[End PSIJ Sensitivity Rail]	It is optional in a .ibs file. It is required with [PSIJ Sensitivity Rail].
[End PSIJ Sensitivity]	It is optional in a .ibs file. It is required with [PSIJ Sensitivity].

[PSIJ Sensitivity] Definition in IBIS

Keyword: **[PSIJ Sensitivity]**

Required: No. Required when [PSIJ Sensitivity Rail] is defined for at least one power supply rail in an I/O interface operating in a particular standard or protocol.

Description: Declares operating protocol of an I/O interface and the beginning of [PSIJ Sensitivity Rail] for the power supply rails.

Usage Rules: The [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair is used to define a list of [PSIJ Sensitivity Rail]s by name that shall be used together for one concerned IO interface operating in a particular standard or protocol in a simulation. A simulation may contain [PSIJ Sensitivity Rail]s of all power rails listed in only one keyword pair of [PSIJ Sensitivity] and [End PSIJ Sensitivity]. The [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair is hierarchically scoped by the [Component] keyword.

… …

Example:

```
[PSIJ Sensitivity] PCIe_Gen4
| …
[End PSIJ Sensitivity]

[PSIJ Sensitivity] PCIe_Gen5
| …
[End PSIJ Sensitivity]

| …

[PSIJ Sensitivity] TypeC
| …
[End PSIJ Sensitivity]
```

[PSIJ Sensitivity Rail] Definition in IBIS

Keyword: **[PSIJ Sensitivity Rail]**

Required: No. Required when [PSIJ Sensitivity Rail] is defined for at least one power supply rail in an I/O interface.

Description: This keyword pair declares the IO POWER supply rail and its unique reference GND, with the next level two keywords of signal_name at pin level. One signal_name is for Power, and the other signal_name for the reference GND.

Sub-Params: signal_name

Usage Rules: The keyword [PSIJ Sensitivity Rail] accepts a string argument, on the same line, which is usually listed as PSR_of_<signal_name> of a POWER supply rail. This string argument shall be no longer than 40 characters and shall not include whitespace.

The keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] may appear multiple times, each with a unique PSR_of_<signal_name> of a POWER supply rail, within a keyword pair of [PSIJ Sensitivity] and [End PSIJ Sensitivity] for the POWER supply rails in one I/O interface operating in one standard or protocol.

… …

Example:

```
[PSIJ Sensitivity] LPDDR4
[PSIJ Sensitivity Rail]  PSR_of_VDD1
signal_name VDD1 | signal_name VDD1 is an
IO power supply rail for LPDDR4 PHY.
signal_name Vss
| …
[End PSIJ Sensitivity Rail]

[PSIJ Sensitivity Rail]  PSR_of_VDD2
signal_name VDD2 | signal_name VDD2 is an
IO power supply rail for LPDDR4 PHY.
signal_name Vss
| …
[End PSIJ Sensitivity Rail]

[PSIJ Sensitivity Rail]  PSR_of_VDDQ
signal_name VDDQ | signal_name VDDQ is an
IO power supply rail for LPDDR4 PHY.
signal_name VSS
| …
[End PSIJ Sensitivity Rail]
[End PSIJ Sensitivity]
```

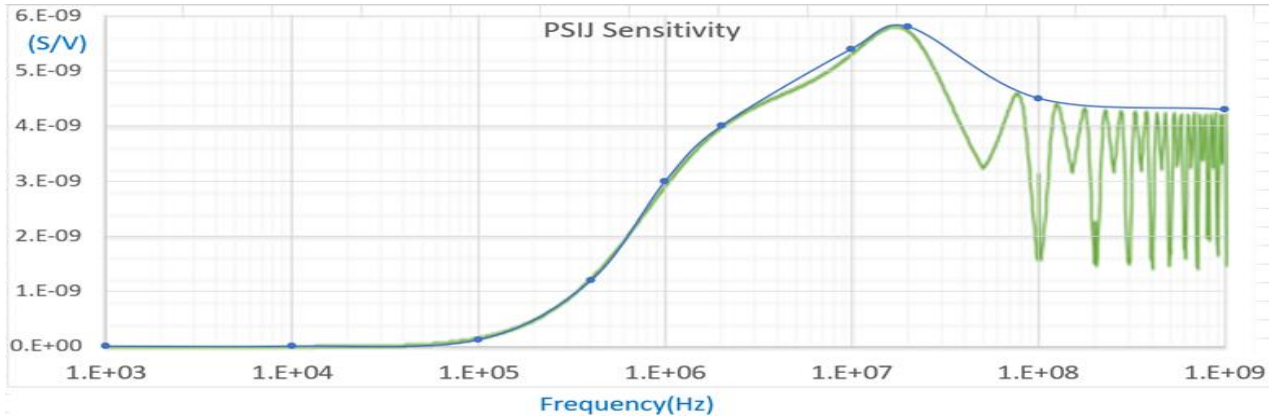
[PSIJ Sensitivity Signal] Definition in IBIS

Keyword: **[PSIJ Sensitivity Signal]**

Required: No. Required when [PSIJ Sensitivity Signal] is defined for at least one type of signals in an I/O interface operating in a particular standard, or protocol.

Description: This keyword pair describes the Power Supply Induced Jitter (PSIJ) sensitivity in PWL (Piece Wise Linear) table format in the frequency domain for a type of signals operating in the particular protocol of [PSIJ Sensitivity], to evaluate the jitter impact to the [PSIJ Sensitivity Signal] through all involved circuit blocks from the total power supply noise of the [PSIJ Sensitivity Rail].

Sub-Params: model_name



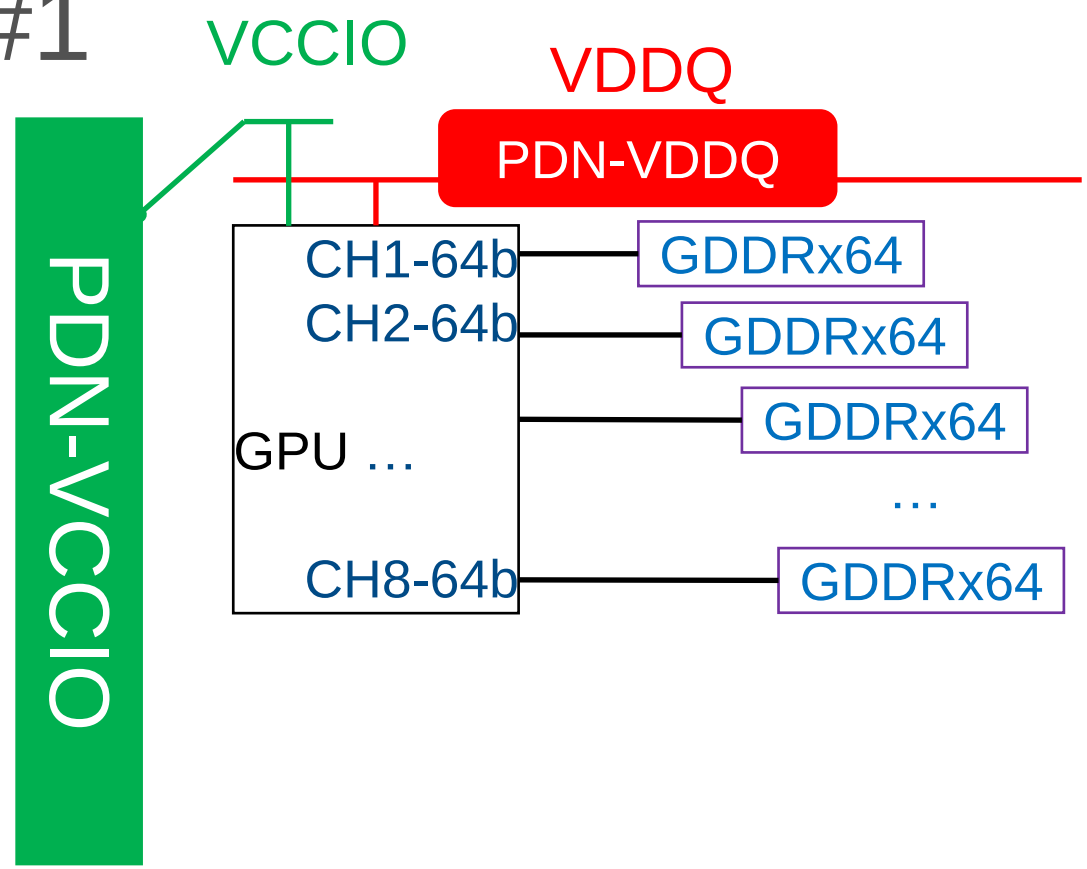
Example:

```
[PSIJ Sensitivity] PCIe_Gen4
[PSIJ Sensitivity Rail]  PSR_of_VCC2
signal_name VCC2
signal_name VSS
[PSIJ Sensitivity Signal] model_name PCIe_Gen4_TX
| model_name defined for same IO signals in the [Pin].
| frequency (Hz)  magnitude(s/V) phase (degree)
0.0             1.00E            0
1.0E+03         1.00E-12         0
1.0E+04         2.00E-12         0
4.0E+05         1.20E-09         0
1.0E+06         3.00E-09         0
1.0E+07         5.40E-09         0
2.0E+07         5.80E-09         0
1.0E+08         4.50E-09         0
1.0E+09         4.30E-09         0
[End PSIJ Sensitivity Signal]
[End PSIJ Sensitivity Rail]

[PSIJ Voltage List]
|V(name)        V(typ)          V(min)          V(max)
VCC2            0.600           0.540           0.660
VSS             0.000           0.000           0.000
[End PSIJ Sensitivity]
```

BIRD226 can well handle #1

1. One power supplier to Multiple Buffers of the same, VCCIO to all 512bits GDDR
2. Multiple power suppliers to one Buffer, VCCIO & VDDQ to 1-bits GDDR
3. Multiple power suppliers to multiple Buffers of the same, VCCIO & VDDQ to all 512bits GDDR

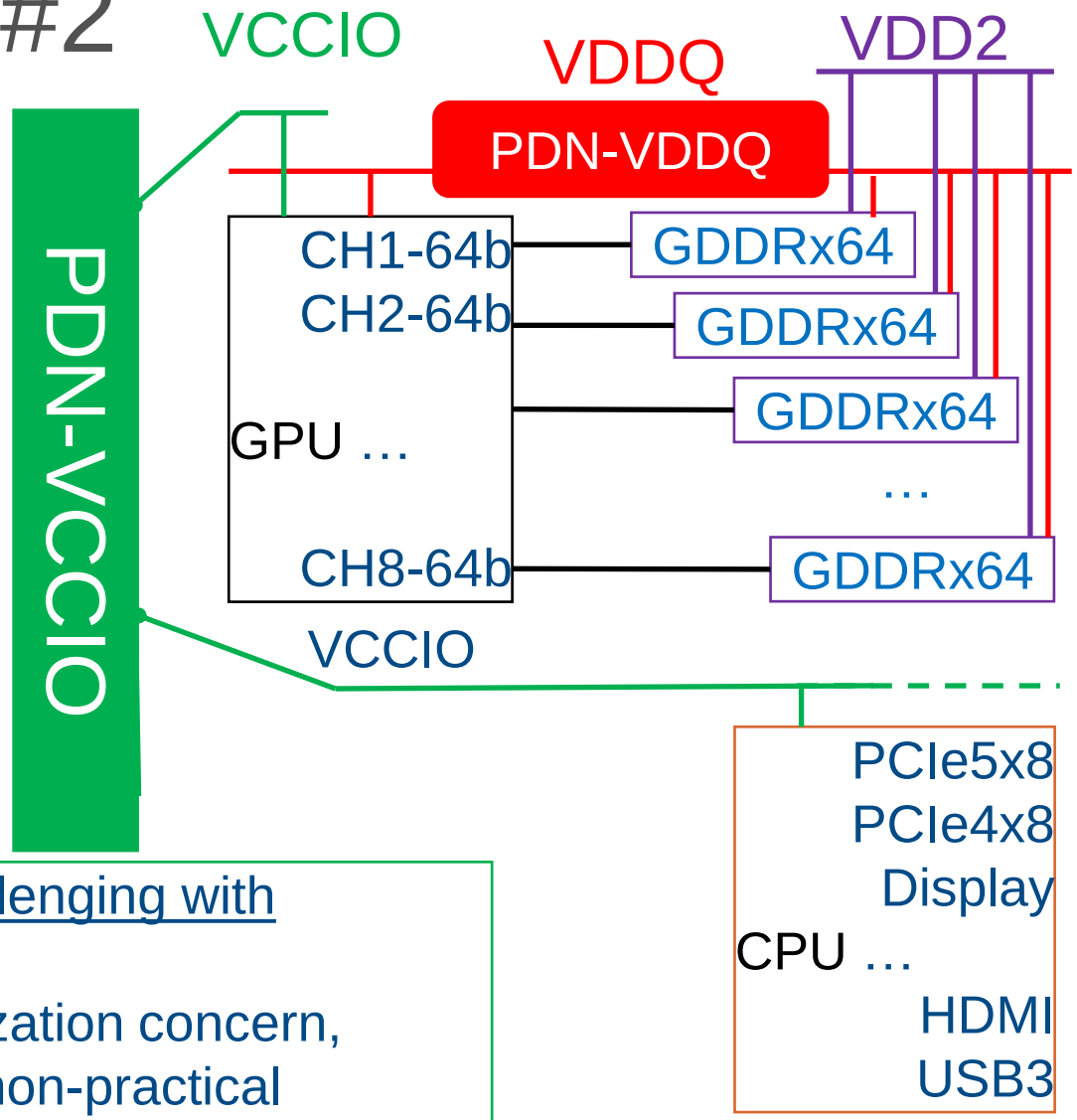


Things need to be considered, might be very challenging with traditional SIPI co-sim algorithm:

1) If a V(t) waveform is directly applied to the SI simulation, there is synchronization concern,
2) Whole PDN need to be included in the sim deck, to reflect the real-time voltage waveform
3) Stimulating bits pattern is tricky for each bit/DQ of all 512 bits, might need to apply PDF

BIRD226 can well handle #2

1. One power supplier to Multiple Buffers of the same, VCCIO to all 512bits GDDR
2. Multiple power suppliers to one Buffer, VCCIO & VDDQ to 1-bits GDDR
3. Multiple power suppliers to multiple Buffers of the same, VCCIO & VDDQ to all 512bits GDDR
4. One/multiple power supplier(s) to multiple interfaces, VCCIO to the interfaces of GDDR PCIe4/5, DP/HDMI/USB3, and etc.



Things need to be considered, might be very challenging with traditional SIPI co-sim algorithm:

1) Directly apply V(t) in SI simulation, synchronization concern,
2) Whole PDN involved of multiple power rails, non-practical
3) Handle **power management events, most critically**

Takeaway

- BIRD226 focused on system level PI & SI co-simulation/design:
  1) SI simulation sets up all involved power supplies ideal at Vnom/Vmin/Vmax, (which is equivalent to disabling of BIRD220, or [ISSO PU] & [ISSO PD], and [Composite Current].)
  2) PI simulation for each involved power rail, includes the contribution from all involved interfaces, and the power management events (multiple stages of sleep/wake-up)
  3) The algorithm of PI contributing jitter from each involved power rails is specified in https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157
  4) All involved power rails' jitter values can be super-positioned upon the eye-diagram from SI simulation as specified in item#1, or upon Tx_Dj or Rx_Dj in IBIS-AMI.
- BIRD226 can handle all listed scenarios:
  - One/multiple power suppliers, to one/multiple Buffer(/bit/lane/interface)s.

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