IBIS Chair's Report

Lance Wang

Zuken USA

Chair, IBIS Open Forum

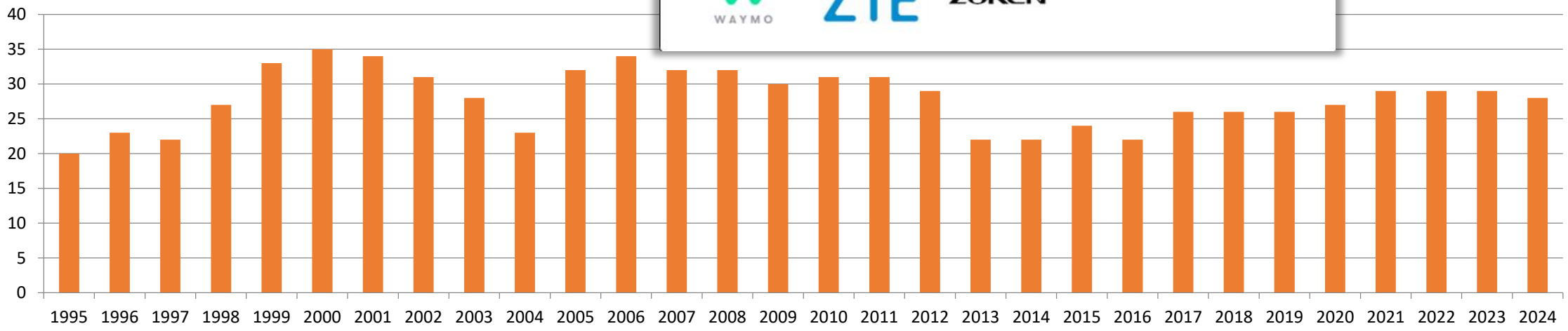
DesignCon 2024 IBIS Summit (Hybrid)

Santa Clara, California, USA

February 2, 2024

28 IBIS Members (Organization-based)

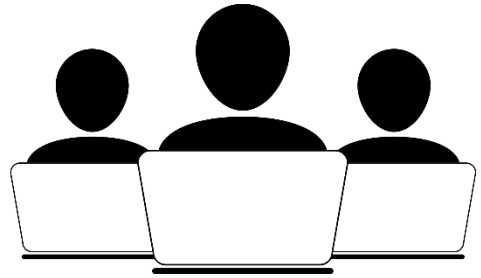
Number of Members by Year



IBIS Officers June 2023- May 2024

Elected

Chair:	*Lance Wang, Zuken USA*
Vice-Chair:	*Randy Wolff, Siemens EDA*
Secretary:	*Graham Kus, MathWorks*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Zhiping Yang, MST*
Postmaster:	*Curtis Clark, ANSYS*
Webmaster:	*Steve Parker, Marvell*

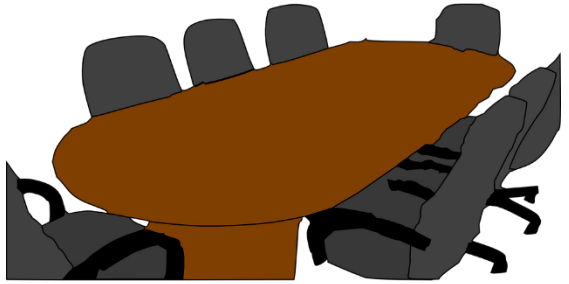


Appointed

- University Relations: *Chulsoon Hwang, MST*
- IEEE DASC IBIS Liaison: *Michael Mirmak, Intel*

IBIS Meetings

- Weekly teleconferences
  - Quality task group (Tuesdays, 09:00 PT)
  - Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
  - Interconnect task group (Wednesdays, 08:00 PT)
  - Editorial task group (Suspended)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
  - DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Tokyo (JEITA-organized)
- Participants: ~290 in 2023 (~280 in 2022)



SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees Tammy Patton (replacing José Godoy), Phyllis Gross, and Michael McNair
- SAE ITC provides financial, legal, and other services
- https://www.sae-itc.com/

SAE ITC®
An SAE International Affiliate

Task Groups

- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Siemens EDA
  - https://ibis.org/atm_wip/
  - Develop non-interconnect technical BIRDs
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/editorial_wip/
  - Produce IBIS specification documents
- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Quality Task Group
  - Chair: Bob Ross, Teraspeed Labs
  - https://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development

BIRD = Buffer Issue Resolution Document

IBIS Milestones

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power-aware model

I/O Buffer Information Specification

- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel time-domain support
  - Interconnect modeling using IBIS-ISS and Touchstone
- 2021 **IBIS 7.1:**
  - DDRx IBIS-AMI support
  - Electrical Module Description (EMD)
  - IBIS-AMI back-channel statistical optimization
- 2023 **IBIS 7.2:**
  - Redriver simulation flow fixes
  - PAMn IBIS-AMI support

Other Work

- 1995: **ANSI/EIA-656 (IBIS 2.1 International standard)**
- 1999: **ANSI/EIA-656-A (IBIS 3.2 International standard)**
- 2001: **IEC 62014-1 (IBIS 3.2 International standard)**
- 2003: **Interconnect Model Specification (ICM 1.0)**
- 2006: **ANSI/EIA-656-B (IBIS 4.2 International standard)**
- 2009: **Touchstone 2.0**
  - Official Touchstone donated from Agilent/Keysight
- 2011: **IBIS-ISS 1.0 (Interconnect SPICE Subcircuit)**
  - Subset of HSPICE
- 2024: **Touchstone 2.1**
  - Clarify S-parameter Definition
  - [End] Keyword Corrections and Other Editorial Changes
  - Per Port Reference Resistance on the Option Line
  - Clarify File Extension Rule for Touchstone 1.0 and 1.1 Files
- **IBISCHK**: IBIS file syntax parser
  - Current version 7.2.1
  - Source code available for purchase
  - Compiled executables available free of charge
- **TSCHK2**: Touchstone 2.0 file syntax parser
  - Current version 2.0.1
  - Source code available for purchase
  - Compiled executables available free of charge

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
229	AMI Test Data Support	Michael Mirmak, Intel Corp.	Dececmber 19, 2023		
228	Pin Name Field Extension	Michael Mirmak, Intel Corporation	December 5, 2023		
227	AMI Ignore Block Feature	Alaeddin A. Aydiner, Sai Zhou, Intel Corp.	November 14, 2023	January 5, 2024	
226	PSIJ Sensitivity	Kinger Cai, Fern Nee Tan, Chi-te Chen, Michael Mirmak, Intel Corp.	August 8, 2023	December 8, 2023	
225	Clarification for bus_label rules	Arpad Muranyi, Weston Beal, Randy Wolff, Siemens EDA	July 11, 2023	September 15, 2023	
224	New AMI Reserved Parameters for Ts4file port order	Liwei Zhao, Intel Corp.; Michael Mirmak, Intel Corp.	April 25, 2023	June 23, 2023	
223.1	Add support for SPIM in IBIS	Kinger Cai, Chi-te Chen, Intel Corp.	March 7, 2023, September 12, 2023	July 14, 2023 (223); November 17, 2023 (223.1)	
222	Clock Times Clarifications	Arpad Muranyi, Siemens EDA	November 8, 2022	December 9, 2022	7.2
221	AMI_parameters_in Clarification	Michael Mirmak, Intel Corp.	October 26, 2022	December 9, 2022	7.2
220	Pre-driver PSIJ Sensitivity Keyword	Yifan Ding, Chulsoon Hwang, Missouri S&T; Zhiping Yang, Waymo; Randy Wolff, Micron Technology	October 20, 2022		
219.1	AMI Parameter Root Name Clarifications	Michael Mirmak, Intel Corp.	March 29, 2022, May 3, 2022	August 12, 2022	7.2

Touchstone Issue Resolution Documents (TSIRD)

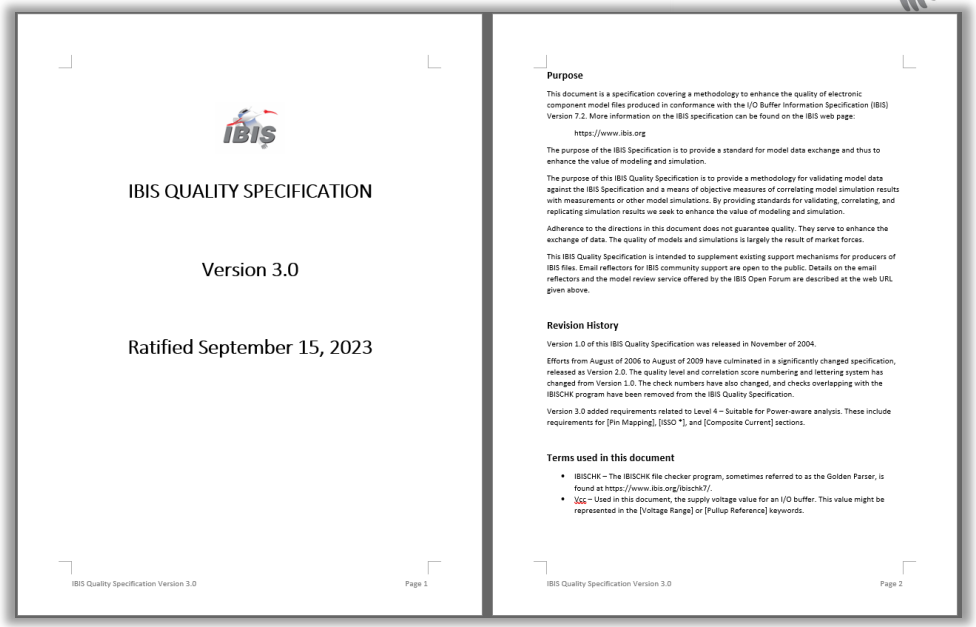
To submit an TSIRD to the IBIS Open Forum, please use the TSIRD Template Rev. 1.0.

ID#	Issue Title	Requestor	Date Submitted	Date Accepted	Supported Version	Formats
6	Clarify File Extension Rule for Touchstone 1.0 and 1.1 Files	Bob Ross, Teraspeed Labs; Arpad Muranyi, Siemens EDA	July 5, 2023	September 15, 2023		(DOC)
5.1	Per Port Reference Resistance on the Option Line	Arpad Muranyi, Randy Wolff, Siemens EDA; Bob Ross, Teraspeed Labs	June 14, 2023; July 5, 2023	September 15, 2023		(DOC)
4.1	[End] Keyword Corrections and Other Editorial Changes	Michael Mirmak, Intel Corp.	March 2, 2022 , July 20, 2022	September 9, 2022		(DOC)
3	Clarify S-parameter Definition	Radek Biernacki, Agilent Technologies; Michael Mirmak, Intel	July 20, 2011 ,	October 7, 2011		(DOC)

IBIS Quality Specification

https://www.ibis.org/quality_ver3.0/

- Quality specification updated to version 3.0 with additions for power-aware models
  - 5 new items for [Component] and [Pin Mapping]
  - 12 new items for [Model]
  - The specification document is approved by the IBIS Open Forum



IBIS QUALITY SPECIFICATION

Version 3.0

Ratified September 15, 2023

Purpose

This document is a specification covering a methodology to enhance the quality of electronic component model files produced in conformance with the I/O Buffer Information Specification (IBIS) Version 7.2. More information on the IBIS specification can be found on the IBIS web page:

https://www.ibis.org

The purpose of the IBIS Specification is to provide a standard for model data exchange and thus to enhance the value of modeling and simulation.

The purpose of this IBIS Quality Specification is to provide a methodology for validating model data against the IBIS Specification and a means of objective measures of correlating model simulation results with measurements or other model simulations. By providing standards for validating, correlating, and replicating simulation results we seek to enhance the value of modeling and simulation.

Adherence to the directions in this document does not guarantee quality. They serve to enhance the exchange of data. The quality of models and simulations is largely the result of market forces.

This IBIS Quality Specification is intended to supplement existing support mechanisms for producers of IBIS files. Email reflectors for IBIS community support are open to the public. Details on the email reflectors and the model review service offered by the IBIS Open Forum are described at the web URL given above.

Revision History

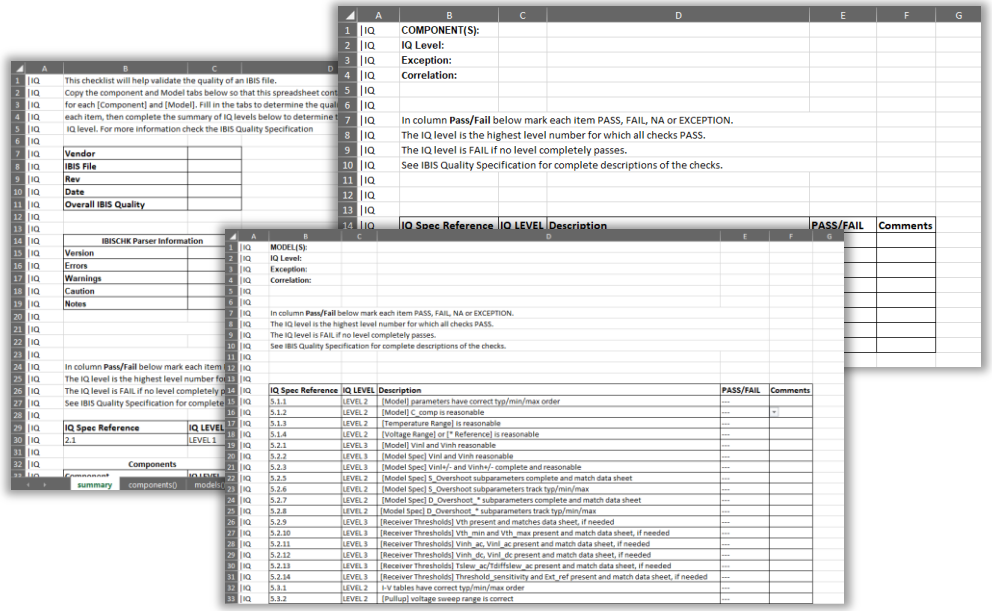
Version 1.0 of this IBIS Quality Specification was released in November of 2004.

Efforts from August of 2006 to August of 2009 have culminated in a significantly changed specification, released as Version 2.0. The quality level and correlation score numbering and lettering system has changed from Version 1.0. The check numbers have also changed, and checks overlapping with the IBISCHK program have been removed from the IBIS Quality Specification.

Version 3.0 added requirements related to Level 4 – Suitable for Power-aware analysis. These include requirements for [Pin Mapping], [ISSO *], and [Composite Current] sections.

Terms used in this document

- IBISCHK – The IBISCHK file checker program, sometimes referred to as the Golden Parser, is found at https://www.ibis.org/ibischk7/.
- Voc – Used in this document, the supply voltage value for an I/O buffer. This value might be represented in the [Voltage Range] or [Pullup Reference] keywords.



1	IQ	COMPONENT(S):					
2	IQ	IQ Level:					
3	IQ	Exception:					
4	IQ	Correlation:					
5	IQ						
6	IQ						
7	IQ	In column **Pass/Fail** below mark each item PASS, FAIL, NA or EXCEPTION.					
8	IQ	The IQ level is the highest level number for which all checks PASS.					
9	IQ	The IQ level is FAIL if no level completely passes.					
10	IQ	See IBIS Quality Specification for complete descriptions of the checks.					
11	IQ						
12	IQ						
13	IQ						
14	IQ	IQ Spec Reference	IQ LEVEL	Description		PASS/FAIL	Comments

1	IQ	This checklist will help validate the quality of an IBIS file.					
2	IQ	Copy the component and Model tabs below so that this spreadsheet cont					
3	IQ	for each [Component] and [Model]. Fill in the tabs to determine the qual					
4	IQ	each item, then complete the summary of IQ levels below to determine t					
5	IQ	IQ level. For more information check the IBIS Quality Specification					
6	IQ						
7	IQ	**Vendor**					
8	IQ	**IBIS File**					
9	IQ	**Rev**					
10	IQ	**Date**					
11	IQ	**Overall IBIS Quality**					
12	IQ						
13	IQ						
14	IQ	**IBISCHK Parser Information**					
15	IQ	**Version**					
16	IQ	**Errors**					
17	IQ	**Warnings**					
18	IQ	**Caution**					
19	IQ	**Notes**					
20	IQ						
21	IQ						
22	IQ						
23	IQ						
24	IQ	In column **Pass/Fail** below mark each item					
25	IQ	The IQ level is the highest level number fo					
26	IQ	The IQ level is FAIL if no level completely p					
27	IQ	See IBIS Quality Specification for complete					
28	IQ						
29	IQ	**IQ Spec Reference**	**IQ LEVEL**				
30	IQ	2.1	LEVEL 1				
31	IQ						
32	IQ	**Components**					

summary | component() | models()

1	IQ	MODEL(S):					
2	IQ	IQ Level:					
3	IQ	Exception:					
4	IQ	Correlation:					
5	IQ						
6	IQ						
7	IQ	In column **Pass/Fail** below mark each item PASS, FAIL, NA or EXCEPTION.					
8	IQ	The IQ level is the highest level number for which all checks PASS.					
9	IQ	The IQ level is FAIL if no level completely passes.					
10	IQ	See IBIS Quality Specification for complete descriptions of the checks.					
11	IQ						
12	IQ						
13	IQ						
14	IQ	**IQ Spec Reference**	**IQ LEVEL**	**Description**		**PASS/FAIL**	**Comments**
15	IQ	5.1.1	LEVEL 2	[Model] parameters have correct typ/min/max order		---	
16	IQ	5.1.2	LEVEL 2	[Model] C_comp is reasonable		---	
17	IQ	5.1.3	LEVEL 2	[Temperature Range] is reasonable		---	
18	IQ	5.1.4	LEVEL 2	[Voltage Range] or [* Reference] is reasonable		---	
19	IQ	5.2.1	LEVEL 3	[Model] Vinl and Vinh reasonable		---	
20	IQ	5.2.2	LEVEL 3	[Model Spec] Vinl and Vinh reasonable		---	
21	IQ	5.2.3	LEVEL 3	[Model Spec] Vinl+/- and Vinh+/- complete and reasonable		---	
22	IQ	5.2.5	LEVEL 2	[Model Spec] S_Overshoot subparameters complete and match data sheet		---	
23	IQ	5.2.6	LEVEL 2	[Model Spec] S_Overshoot subparameters track typ/min/max		---	
24	IQ	5.2.7	LEVEL 2	[Model Spec] D_Overshoot_* subparameters complete and match data sheet		---	
25	IQ	5.2.8	LEVEL 2	[Model Spec] D_Overshoot_* subparameters track typ/min/max		---	
26	IQ	5.2.9	LEVEL 3	[Receiver Thresholds] Vth present and matches data sheet, if needed		---	
27	IQ	5.2.10	LEVEL 3	[Receiver Thresholds] Vth_min and Vth_max present and match data sheet, if needed		---	
28	IQ	5.2.11	LEVEL 3	[Receiver Thresholds] Vinh_ac, Vinl_ac present and match data sheet, if needed		---	
29	IQ	5.2.12	LEVEL 3	[Receiver Thresholds] Vinh_dc, Vinl_dc present and match data sheet, if needed		---	
30	IQ	5.2.13	LEVEL 3	[Receiver Thresholds] Tslew_ac/Tdiffslew_ac present and match data sheet, if needed		---	
31	IQ	5.2.14	LEVEL 3	[Receiver Thresholds] Threshold_sensitivity and Ext_ref present and match data sheet, if needed		---	
32	IQ	5.3.1	LEVEL 2	I-V tables have correct typ/min/max order		---	
33	IQ	5.3.2	LEVEL 2	[Pullup] voltage sweep range is correct		---	

- Quality checklist spreadsheet
  - The checklist spreadsheet is in sync with the specification document
  - The spreadsheet includes some automation to determine IQ level on each component and model sheet
  - The spreadsheet file will be available on the website along with the new version of the specification

IBISCHK 7.2.1 Development

- New parser is delivered on December 21, 2023
- Covers 6 BUG fixes (BUG 239 and BUG 241-245)
  - https://ibis.org/bugs/ibischk/

IBISCHK Parser Issue Reports (BUGs)

To find out how to submit a bug to the IBIS Open Forum, please read the document bugform.txt.

ID#	Title	Requester	Date Submitted	Severity	Priority	Status	Date Closed	Supported Version
245	Has Platform Issue Message in IBIS-AMI Checking Not Clear	Weston Beal, Siemens EDA	June 13, 2023	MODERATE	LOW	CLOSED	December 8, 2023	7.2.1
244	False IBIS Ver Compatibility Error for EMD and IBIS File Checking	Randy Wolff, Arpad Muranyi; Siemens EDA	June 14, 2023	MODERATE	MEDIUM	CLOSED	December 8, 2023	7.2.1
243	Remove Make File Warning Messages During Compilations	Graham Kus, MathWorks; Michael Schaeder, Zuken; Curtis Clark, Ansys; Bob Ross, Teraspeed Labs	May 30, 2023	ANNOYING	LOW	CLOSED	December 8, 2023	7.2.1
242	Change Caution to Error for Illegal NC as signal_type and Change Message	Randy Wolff, Siemens	May 28, 2023	SEVERE	MEDIUM	CLOSED	December 8, 2023	7.2.1
241	Remove or Revise EMD Warning for Legal signal_name, signal_type Combinations	Randy Wolff, Siemens	May 26, 2023	SEVERE	MEDIUM	CLOSED	December 8, 2023	7.2.1
240	Parser Crashes When [Interconnect Model Group] Name is Missing	Arpad Muranyi, Siemens EDA	March 3, 2023	SEVERE	HIGH	CLOSED	April 21, 2023	7.2.0
239	No Message for Unreferenced [Interconnect Model Set]s	Michael Mirmak, Intel Corp.	March 3, 2023	ENHANCEMENT	LOW	CLOSED	December 8, 2023	7.2.1
238	Interconnect Models with Duplicate pin_names Incorrectly Produce Errors	Michael Mirmak, Intel Corp.	October 14, 2022	MODERATE	MEDIUM	CLOSED	November 18, 2022	7.1.1

Recent and Future Developments in IBIS?

- IBIS Open Forum's task groups are discussing these topics:
  - Expanded system-level perspective
    - Clock/data relationships, timing information, equalization training
  - Power Integrity focused modeling
    - Chip-level Standard Power Integrity Model (SPIM, BIRD223 accepted on July 14, 2023)
    - Improved Power Supply Induced Jitter modeling (PSIJ, BIRD226 accepted on Dec. 8, 2023, and BIRD220 is pending approval)
    - Voltage regulator, diode, and inductor models
  - Multi-level analog buffer modeling
  - Interconnect Modeling
    - Touchstone 2.1 expansions, adds per-port reference resistances on the option line
    - Touchstone 3.0 with Pole/Residue and port mapping support
    - IBIS-ISS expansions
  - Quality and Testing
    - AMI Test Data Support (BIRD229)
- What else should we be looking at? Bring your ideas!

Participation in IBIS

- The success of IBIS depends on active participation and volunteering
- Bringing your ideas and talents to IBIS
  - Task groups for technical discussions and document editing
  - IBIS email reflectors
  - Open Forum teleconferences for event planning and voting
  - Summit presentations
  - IBIS Board and task group volunteering
  - Writing BIRDs – Buffer Issue Resolution Documents
    - Official method for submitting a proposed change to the IBIS specification
    - Many developed collaboratively in task groups
    - Discussed and voted on in Open Forum meetings

IBIS Website Resources

IBIS Summits

Task Group Info

Member FAQ

Spec documents

*IRDs

Email support

Syntax Parser Downloads

IBIS.org

[Thank You]

IBIS Open Forum:
Web: https://ibis.org
Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.