

## Addressing the challenges of PAM-3 USB 4.0 - Design and Analysis

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## Agenda

- USB4 Challenges
- USB4 Compliance Kit
- USB4 AMI Model parameters
- Requirements to pass USB4 Gen 4 Compliance
- USB4 Spec
  - This presentation refers to tables and sections defined in the USB4 Specification V2.0
  - o <u>https://www.usb.org/document-library/usb4r-specification-v20</u>
- TX/RX AMI Optimization
- TX/RX AMI and Channel Co-Optimization
- Conclusions

## **USB4 Gen 4 Compliance Challenges**

- USB4 PAM3
- Equalization
  - $\circ$  Tx AMI Model
    - 42 presets
    - 2 precursor taps
    - 1 postcursor tap
  - $\circ$  Rx AMI Model
    - 2 stage CTLE
    - 12 tap DFE

#### - SNDR (Signal to Noise Distortion Ratio)

 $\circ~$  Not a standard serial link measurement

#### **PAM3** Overview

- MLT-3 was included in patent (#5280500) which was filed by Mario, Luca, and Maurilio in 1991
- Multi-Level Transition (MLT-3) was used on 100Base-TX (802.3u) in 1995.
- PAM3 (8b/6t) was adopted into 100BASE-T4 (100 Mbit/s over four-pair UTP cable) in 1995 as well
- USB4 V2.0 adopted PAM3 to support 40Gbps/lane speed for USB4 Gen4
- PAM3 offers larger vertical eye openings compared with PAM4 and less bandwidth requirement than NRZ (PAM2)
- Key technical details
  - 25.6Gtps to support 40Gbps
  - 11b/7t (1.57 bits per symbol) encode/decode scheme
  - **2048/2187** offers better overhead vs USB 3.1/3.2 and USB4 128b/132b and 8b/10b USB3.0 encoding schemes
  - Pre-coding scheme is adopted to reduce the burst errors due to RX DFE (Decision Feedback Equalization)
  - Forward Error Correction (FEC) for PAM-3 is required for USB4 V2.
  - Reed-Solomon (480,504) FEC detects and corrects up to 12 errors per block
  - Combined with precoding, the resulting BER of 1E-19 is significantly better than 1E-12 for USB4 Gen3 20Gbps.



### **USB4 Compliance Kit Setup**

			Ŭ	SB4 Gen 4 Co	ompliance Ki	it				
							D o N ot Delete		o Not Delete	
Tx	TP1	ТХ_РКС	rP2 C	kt Ckt1	Ca	able	TP3	RX_PKG	TP4	Rx
		subckt	ubckt	bokt				subckt	subckt	B
AMI	TX IC Output	TXP ort Conn	ector Output PC I	B Fixture Receptacle Fi:	dure USB-	-C Cable	RX Port C onnecor Input			AMI
Simulation Properties:										
Data Rate (Gbps)	Log BER	Ignore Time (ns)	Minimum # of Bits	Bit Sampling Rate	BER Floor					
38.4	-8	200	100000	32	1e-8					

Figure 3-27. Gen 4 Compliance Test Point Definitions

- 25.6GBaud/S PAM3 Signaling (40 Gbps)
- 42 Preset TX AMI Model
- Dual Stage CTLE with 12 Tap DFE RX AMI Model
- Users can replace all Rx, Tx, PKG, and interconnect models with their own



#### Table 3-21. Electrical Compliance Test Points

Test Point	Description	Comments					
TP1	Transmitter IC output	Not used for Gen 4 electrical testing.					
TP2	Transmitter port connector output	Defined at the output of a compliance plug fixture.					
TP3	Receiver port connector output	Defined at the receptacle side of the connector. All measurements at this point shall be done while applying the reference equalization function.					
TP3'	Receiver port connector input	Defined at the output of a compliance plug fixture.					
TP4	Receiver IC input	Not used for Gen 4 electrical testing.					

## **Compliance Tests**

#### Tx Tests

- Tx Level
- Tx Differential Return Loss (Figure 3-31)
- Tx Signal to Noise Distortion Ration
  (SNDR) (Section 3.2.3.4)

#### • Rx Tests

- End to End Channel Differential Insertion
  Loss @12.8 GHz
- Differential Return Loss Mask (Figure 3-35)
- Receiver Tolerance Test (Section 3.2.4.2)

#### USB 4 - Gen 4 Compliance Kit

#### Choose Compliance Items

No.	Parameter	Values	
1	Tx Level		
2	Tx Differential Return Loss		
3	Tx Signal to Noise Distortion Ratio (SNDR) (Section 3.2.3.4)	32.5 dB	
4	End to End Channel Differential Insertion Loss @ 12.8 GHz	28.5 dB	
5	Rx Differential Return Loss		
6	Receiver Tolerance Test (Section 3.2.4.2)		





## Tx AMI

#### Tx Equalization

- 42 presets defined in USB4 Spec
- Default preset of Tx shall be configured to setting that obtains lowest data dependent jitter





#### USB4 Gen4 TXAMI Model





### **Rx AMI**

- Rx Equalization
- Dual stage CTLE with 12 tap DFE
  - All measurements at TP3 shall be taken while

applying the reference equalization function



			RX EQ Settings
g_DC	[-12:1:0]	dB	CTLE stage1 (high pole) DC attenuation
g_DC_HP	[-6:1:0]		CTLE stage2 (low pole) DC attenuation
f_HP_PZ	0.32	GHz	CTLE stage2 pole location
f_z	10.24	GHz	CTLE stage1 zero location
f_p1	10.24	GHz	CTLE stage1 first pole location
f_p2	25.6	GHz	CTLE stage1 second pole location
N_b	12	UI	Number of DFE taps
b_max(1)	0.75		Dynamic range limitation for the DFE first tap (reference
b_max(2N_b)	0.2		Dynamic range limitation for the DFE taps 2 and above





### **Tx Level**

- Tx levels mismatch ratio is calculated as a function of the mean PAM3 constellation levels
- TX\_LEVELS\_MISMATCH = min{(V2-V1)/ $\Delta$ , (V1-V0)/ $\Delta$ }
- TX\_LEVELS\_MISMATCH >= 0.975





## Tx Differential Return Loss – 3.2.3.7

- Tx Return Loss should only include Tx and PKG
- IBIS File usage
  - $\circ~$  Calculate output impedance and use C\_Comp
  - $_{\circ}\,$  Will use external model if pointed to in IBIS





SDD22(f) = 
$$\begin{cases} -8.5 & 0.05 < f_{GHz} \le 6 \\ -5.84 + 7.2 \cdot \log 10 \left(\frac{f_{GHz}}{14}\right) & 6 < f_{GHz} \le 14 \end{cases}$$

## Tx Signal to Noise and Distortion (SNDR) – 3.2.3.4

- Ratio between linear fit pulse peak and the root square sum of linear fit error and additive noise
  - SNDR is the variation between the ideal signal and the measured signal
  - Same as IEEE Ethernet standards
- TX\_SNDR >= 32.5dB

The TX\_SNDR is defined as follows:

$$TX \_SNDR = 20 \cdot log_{10}(\frac{P_{max}}{\sqrt{\sigma_e^2 + \sigma_n^2}})$$

where, Pmax is the maximum value of the linear fit pulse response p(k).

#### End to End Channel Diff Insertion Loss – 3.2.4.2

- Single point test at 12.8GHz
  - $\circ~IL < \text{-}28.5~dB$ @ 12.8GHz
  - $\circ$  Die to Die





#### **Rx Differential Return Loss – 3.2.4.1.2**

- Rx Return Loss should only include Rx and PKG
- IBIS File usage
  - $\circ\,$  Calculate input impedance and use C\_Comp
  - $\circ\,$  Will use external model if pointed to in IBIS





#### **Receiver Tolerance Testing – 3.2.4.2**

- Receiver tested by injecting different sinusoidal jitter (SJ) one at a time.
  - $_{\odot}$  Jitter frequencies 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz
- Tx parameters configured to Table 3-27
- Operate at BER of 1E-8 or lower

Table 3-27. Stressed Signal for Gen 4 Receiver Compliance Testing

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]	
1	1 1000		0.975	100	0.085	0.0085	
2a+2b	800	32.5	0.975	100	0.075	0.0085	



#### **USB4 Compliance Report**



#### **General Information**

- Project File: usb4\_compliance.topx
- Circuit Simulator: SPDSIM

Summary of Results

#### Transmitter Tests (Table 3-22)

Item	Value	Simulation Results	Pass/Fail
Tx Level	800 mV	800.009	
Tx Differential Return Loss			
Tx Signal to Noise Distortion Ratio (SNDR) (Section 3.2.3.4)	32.5 dB	83.692	
Receiver Tests			
Item	Value	Simulation Results	Pass/Fail
End to End Channel Differential Insertion Loss @ 12.8 GHz			
Rx Differential Return Loss			

## **USB4 Simulation Results**



Eye Contours

Noise Bathtub

## **TX/RX AMI Optimization**

#### Setup parameters for optimization

- $\circ$  FFE Tap
- $\circ$  CTE\_1 select
- $\circ$  CTE\_2 select
- Objective function
  - $\circ~$  Optimize to maximize SNR
  - Sweeps required: 3276 (42x6x13)

🖓 Optimality	
Analysis Types Optimization Parameters Optimization Configuration Optimization Results	General Configuration Iteration Count 50 Parallel Count 2 Maximum Time(Hour) 100 Advanced Options _ Use Ref value as initial _ Local Optimization _ Resume _ Decimal Places 8 CPU for optimization engine 16

	1	1	1	1								2		
Index	Optimize	Name	Туре	Expression	<pre></pre>	Unit	undTy	wBoui	∃hBou	Step		List		
1	$\checkmark$	FFE Tap	List								P0,P1,P2,P3,P4,P5,	P6,P7,P8,P9,P10	,P11,P12,F	13,P14,P15
2		CTE_1_sel	List								0,1,2,3,4,5,6,7,8,9,	10,11,12		
3		CTE_2_sel	List								0,1,2,3,4,5			
inction ta	able													
inction ta	able		Expre	ssion		Cust	om Fun	ction			Туре	Quantity		
nction ta Ni COM	ame		Expres	ssion		Cust	om Fun	ction	Measu	uremen	Type t	Quantity		
INCTION TA NA COM SNR	able		Expres	ssion		Cust	om Fun	ction	Measu	uremen	Type t	Quantity		
INCTION TA NA COM SNR BER_Eyel	able ame		Expres	ssion		Cust	om Fun	ction	Measu Measu Measu	uremen uremen uremen	Type t t t	Quantity		
COM SNR BER_Eyel BER_Eyel	able ame		Expres	ssion		Cust	om Fun	ction	Measu Measu Measu Measu	uremen uremen uremen uremen	Type t t t	Quantity		
UNCTION TA N COM SNR BER_Eye BER_Eye <sup>4</sup> obj	ame Height .	1 / SNR	Expre	ssion		Cust	om Fun	ction	Measu Measu Measu Measu Objec	uremen uremen uremen uremen	Type t t t t t t t	Quantity		

## **TX/RX AMI Optimization Results**

- Convergence history and Results Table. View waveforms directly from Results Table

40

FFE Tap

P16

P16

P16

P16

P12

P12

P18

P9

Save

SNR

189.29

182.96

164.3

164.25

155.76

150.93

123.48

Generate HTML Report

EyeContourHeight

55

45

45

48

53

45

62

53

- Sweeps required: 3276 (42x6x13)

Convergence History

0.001

obj

0.0052829 35

0.00381098 44

0.00546568 35

0.00608643 37

0.00608828 43

0.00642013 36

0.00662559 49

0.00809848 44

BER\_EyeHeight

BER\_EyeWidth

0.33

0.3

0.29

0.3

0.3

0.29

0.31

0.32

COM

10.13

8.31

8.54

8.07

8.97

8.16

8.19

10.66

Result Table

Index

20

16

48

18

17

13

15

- AI-empowered optimization with less than 100 iterations

Iteration number

CTE\_1\_sel

8

0

8

CTE\_2\_sel

0

3

0

0

0

0



Least Optimized

#### **Cable Modeling Tool**



妃 Cable Editor				×					
Stackup Editor	T-Line Results		Gene	rate W-Element Model					
Iteration: 1 🔻									
Wire Name	Imp_SE (Ohm)	Delay (ps/m)	Velocity (cm/ns)	Alpha (nepers/m)					
a	181.714	8887.47	11.2518	0.190059					
b	181.714	8887.47	11.2518	0.190059					
Pair Name	Imp_Diff (Ohm)	Imp_Comm (Ohm)	Delay_Diff (ps/m)	Alpha_Diff (nepers/rr					
a-b	100.666	423.609	8887.47	0.190059-0.190059					

## **TX/RX AMI and Channel Co-Optimization**

#### - Optimize around Cable Diameter and Tx, Rx AMI

#### parameters

- Simulate +/-20% manufacturing tolerances
  - Lowbound 0.8
  - Highbound 1.2
- Ability to optimize any cable parameter that you wish
- Discrete and continuous parameters
- Sweep Iterations Required (1 mil steps):>4.7M

General Configuration
Iteration Count 50 A V
Parallel Count 4 🔺 🔻
Maximum Time(Hour) 100 🔺 🔻
Advanced Options
Use Ref value as initial
Local Optimization
Resume
Decimal Places 4 🔺 🔻
CPU for optimization engine 16

Paramet	er table										
Filter											Manage Parameters Check Parameters
Index	Optimize	Name	Туре	Expression	Ref Value	Unit	BoundType	LowBound	HighBound	Step	List
1	$\checkmark$	FFE Tap	List								P0,P1,P2,P3,P4,P5,P6,P7,P8,P9,P10,P11,P12,P13,P14,P15,P16,P17,P18,P19,P20,P21,P
2	$\checkmark$	CTE_1_sel	List								0,1,2,3,4,5,6,7,8,9,10,11,12
3	$\checkmark$	CTE_2_sel	List								0,1,2,3,4,5
4	$\checkmark$	cable_diameter	Float	200 mil	200	mil	relative	0.8	1.2		
5	$\checkmark$	conductor_diameter	Float	42.5 mil	42.5	mil	relative	0.8	1.2		
- Functior	table										
	Name		Expression		C	ustom Fur	nction		Туре		Quantity
EyeCo	ntourHeight	·					M	easurement			
СОМ							M	easurement			
SNR							M	easurement			
BER_E	yeHeight						M	easurement			
BER_E	yeWidth						M	easurement			
obj		1 / SNR					Ob	jective Functi	on(goal)		
Targ	et relative path										Set up Mask Select Measurements Add Delete

## **TX/RX AMI and Channel Co-Optimization Results**

Convergence history and Results Table. View waveforms directly

#### from Results Table.

Optimize taps, and +/-20% at the same time (>4.7M sweeps)



AI-empowered optimization with less than 50 iterations

## Conclusion

#### - USB4 Challenges simulating next-gen interfaces

- Unique measurements
- Higher speeds and PAM-3 encoding

#### USB4 Compliance Kit

- Tx & Rx Checks
- Interconnect, Channels Checks
- IBIS, AMI Models

#### - USB4 optimization functions

- TX/RX AMI parameter optimization
- Channel design optimization & manufacturing tolerance simulations
- TX/RX and Channel co-optimization

# THANK YOU! & QUESTIONS?

Please contact me at <u>yangzhip@mst.edu</u> or <u>zhipingyang@JAY-Plus.com</u>