



## IBIS Open Forum Minutes

Meeting Date: **January 31, 2020**

Meeting Location: **DesignCon 2020 IBIS Summit, Santa Clara, CA, USA**

### VOTING MEMBERS AND 2020 PARTICIPANTS

ANSYS	Curtis Clark, Marko Marin*, Shai Sayfan-Altman* Zilwan Mahmood*
Applied Simulation Technology	(Fred Balistreri)
Broadcom	James Church*
Cadence Design Systems	Zhen Mu, Ambrish Varma*, Jared James* Kumar Keshavan*, Ken Willis*
Cisco Systems	Stephen Searce*, Hong Wu*
Dassault Systemes (CST)	Stefan Paret*
Ericsson	Anders Ekholm*, Sungjoo Yu*, Thomas Ahlstrom*
Google	Zhiping Yang*, Shuai Jin*, Zhenxue Xu*
Huawei Technologies	(Hang (Paul) Yan)
IBM	Michael Cohen
Infineon Technologies AG	(Christian Sporrer)
Instituto de Telecomunicações	(Abdelgader Abdalla)
Intel Corporation	Hsinho Wu*, Michael Mirmak*, Adrien Auge* Fernando Mendoza*, Taeyoung Kim*, Wendem Beyene* Oleg Mikulchenko*, Nhan Phan*, Ifiok Umoh* Subas Bastola*
Keysight Technologies	Radek Biernacki, Hee-Soo Lee*, Todd Bermensolo* Graham Riley*, Pegah Alavi*, Fangyi Rao* Stephen Slater*
Marvell	Steve Parker*, Johann Nittmann*
Maxim Integrated	Joe Engert*, Charles Ganal*, Dzung Tran*
Mentor, A Siemens Business	Arpad Muranyi*, Raj Raghuram*, Todd Westerhoff* Weston Beal*
Micron Technology	Randy Wolff*, Justin Butterfield*
NXP	John Burnett*
SerDesDesign.com	John Baprawski*
SiSoft (MathWorks)	Mike LaBonte, Walter Katz*, Graham Kus*
SPISim	Wei-hsing Huang*
Synopsys	Ted Mido*, Andy Tai*
Teraspeed Labs	Bob Ross*
Xilinx	Ravindra Gali*
ZTE Corporation	(Shunlin Zhu)
Zuken	Michael Schäder*, Kazunari Koga*
Zuken USA	Lance Wang*

## OTHER PARTICIPANTS IN 2020

Accton	Tariq Abou-Jeyab*
Achronix Semiconductor	Hansel Dsilva*
Apollo Giken Co.	Satoshi Endo*
Kandou Bus	Sherman Chen*
KEI Systems	Shinichi Maeda*
Kioxia Corporation	Yasuo Otsuka*
OmniVision	Sirius Tsang*
Qualcomm	Kevin Roselle*, Sunil Gupta*
Renesas	Genichi Tanaka*
RITA Electronics	Takahide Nozaki*
SAE ITC	Jose Godoy
Samsung	Wonsuk Choi*
San Jose State University	Vincent Tam*
Seagate	Preetesh Rathod*, Alex Tain*, Karthik Chandrasekar* Emmanuel Atta*
Signal Metrics	Ron Olisar*
Silvaco Japan Co.	Yoshiharu Furui*
SK Hynix Memory Solutions	Jongchul Shin*, Alex Lee*, James Yu*
Socionext	Matsumura Motoaki*, Shinichiro Ikeda* Takafumi Shimada*
Teradyne	Dongmei Han*, Edward Pulscher*, Sheri Zhuang* Tomoo Tashiro*, Paul Carlin*, Tao Wang*

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

## UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 21, 2020	627 261 744	Friday1

For teleconference dial-in information, use the password at the following website:

<https://tinyurl.com/IBISfriday-new>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

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## **OFFICIAL OPENING**

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center, during the week of the 2020 DesignCon conference. About 87 people representing 39 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<https://www.ibis.org/summits/jan20/>

Randy Wolff welcomed everyone to the Summit, opening the meeting at 8:30 a.m. He thanked the sponsors Cadence Design Systems, Keysight Technologies, and Synopsys for offsetting the cost of food and audio-visual equipment.

Randy asked participants to introduce themselves. He noted the Summit presentations are up on the IBIS website.

## **IBIS CHAIR'S REPORT**

Randy Wolff (Micron Technology, USA)

Randy Wolff reported on the current state of the IBIS Open Forum. He noted we now have 27 members including SerdesDesign.com who was added last week. Randy encouraged anyone who is not currently a member to join IBIS, noting members have voting rights. Randy thanked the IBIS officers for their involvement in IBIS. Randy reviewed the task group meeting schedules and the schedule for the IBIS Open Forum meetings and likely IBIS Summit meetings. He also noted, in addition to DesignCon, they plan to have summits including IEEE SPI, Shanghai, Taipei, and Tokyo. Randy reviewed how SAE is the parent organization for IBIS providing financial, legal, and other services. He thanked the task group chairs for leading these groups and weekly meetings.

Randy announced an IBIS China Regional Forum as a way for people in China to support each other and talk about technical IBIS topics and BIRD development. He noted the meetings will be conducted in Mandarin, but the minutes will be provided in English for everyone to review. Randy noted IBIS 1.0 was issued in 1993, and in 2019, we released IBIS 7.0. Randy showed the number of meetings for each new IBIS version including 7.0, and he would like everyone to be thinking about the timeline for IBIS 7.1. He discussed the planning of BIRDs to include in IBIS 7.1. These include DC\_Offset, C\_comp Model, EMD, and Back-channel Statistical Optimization, among others. He would like to start planning when to cut off new technical content for IBIS 7.1.

## **IBIS-ATM TASK GROUP REPORT**

Arpad Muranyi (Mentor, a Siemens Business, USA)

Arpad Muranyi reviewed the charter of the IBIS ATM task group, which is to look at advanced modeling topics. The group is currently discussing DDR5 IBIS-AMI topics. Arpad noted IBIS

7.0 was released in March 2019 and included 17 BIRDS. He noted two BIRDS have been approved since DesignCon 2019 including BIRD199 and BIRD200. He reviewed the pending BIRDS including enhancements to the Redriver Flow, DC\_Offset, I-V Table Clarifications, On-die PDN modeling, EMD, and Back-channel Statistical Optimization. Arpad noted there might be a need for a new redriver flow. He has asked for feedback from the SI engineering community, but he has not received any feedback yet. He noted the PDN model proposed from JEITA in BIRD198 is a simplified approach to include on-die PDN models. The task group is also discussing DDR5 IBIS-AMI topics including the clock input for an IBIS-AMI function.

Michael Mirmak asked about other BIRDS that may be coming not related to DDR5, and if there are any other discussion topics. Arpad stated he is not aware of any. Bob Ross noted the discussion about the null character and how to handle the passing of double quotes into the IBIS-AMI executable model. Walter Katz noted there are a few presentations today, which may raise some additional topics.

## **IEEE 2401-2019 PUBLICATION WITH SUPPORTING IBIS VERSION 7.0**

Kazunari Koga (Zuken (for JEITA), Japan)

Kazunari Koga from the Zuken core design group introduced himself as a member of JEITA. He has worked on the IEEE 2401 LPB specification, which can link to IBIS models. He gave an overview of the LSI, package, and board PCB co-design. The co-design methodology can be challenging from the EDA standpoint, since the CAD database formats can be very different between these design types. The current approach is to use a spreadsheet, which is prone to human error and does not have a standard format.

The LPB format was proposed by JEITA and describes the shared information for the design. The format is divided into project management, netlist, component, design rules, geometry, and glossary. The merit of the LPB format is to allow the LSI package and board design companies to have a consistent format. The LPB format can help to reduce the design time by standardizing the information across these companies. The new IEEE2401-2019 LPB format includes electrical models (such as IBIS), thermal models, and 3D structures. The format links to IBIS 7.0, which can define the interconnect model, including the on-die interconnect from die pad to buffer. Koga-san showed an example of the LPB format linking to that IBIS model that describes both the die and the package.

Koga-san noted feedback from early developers is that it would be nice to have a textbook with a specific scope for user purpose. Users would also like to check if the format is correct. He noted with the LPB format users can have different use cases. They plan to have an educational course to cover the fundamentals of the 2401 format. He gave an example of the textbook, which details the format of a capacitor including the dimensions and linking a SPICE circuit model.

Walter Katz noted it is good to see the LPB format link to IBIS. He added we now have broadband models for on-die interconnect and packages, but we lack sufficient connector model support. He would like to have better support for connector models in IBIS.

Michael Mirmak asked if the format is based on XML, and if there is any plan for a syntax checker. Koga-san noted it depends on the format if it is based on XML, and they do plan to

create a checker for two of the formats. Many EDA tools can check the format as well.

Ken Willis asked if interposers can be included in LPB. Koga-san replied that silicon interposers can be included in the format.

A question was asked about where to find more information about the courses. Koga-san noted they are planning the courses now and will release the schedule. Randy Wolff asked if this information will be on the JEITA website. Koga-san responded he thinks so, but he will have to check.

Randy asked if each company is expected to create these files for customers. Koga stated, ideally, the EDA tool can generate the LPB format files automatically.

Walter asked about more complicated package models in EMD and how these will be supported in LPB. He asked if the board layout should be in the package model format or the physical format. Koga-san noted very few EDA vendors support the LPB format, and he hopes more EDA vendors will support the format in the future. Randy asked if you need to be an IEEE or JEITA member to access the specification. Koga-san noted you can access the LPB specification from IEEE for a fee.

## **DDR SIMULATION WITH IBIS-AMI**

Randy Wolff, Justin Butterfield (Micron Technology, USA)  
[Presented by Randy Wolff (Micron Technology, USA)]

Randy Wolff noted DDR with IBIS-AMI has been a hot topic in the last few years. He described how several tools have adopted IBIS-AMI channel simulation for DDR to include equalization. The traditional IBIS-AMI flow was designed for SerDes differential signaling. The issues using IBIS-AMI for single-ended DDR systems include the common mode voltage, the non-linearities (which can have intentional differences in rise and fall impedances and slew rate), and non-linear IV curves due to the nature of DRAM transistors. He noted the forwarded clock is also an issue, although he does not plan to cover this.

Randy compared differences between some of the simulators. He gave an anonymous comparison of some of the EDA simulator tool features. One of these features is a multi-edge time domain technique to improve the modeling of the non-linearities. This has not been standardized, as IBIS decided to not change the specification and allow tools to come up with their own solution. He noted the common mode issue can vary between tools and BIRD197 should help to standardize this, but currently tools can pass the waveforms into GetWave with the common mode voltage or centered around 0V. In Micron's models, they provide a VREF parameter to account for this, but he would like to avoid this in the future. He noted the clocking is still a work in progress, and there is some responsibility of the model makers to show how big an issue this is.

Randy noted he used an example LPDDR5 system with an IBIS-AMI simulation. Only an IBIS-AMI model for the DRAM Rx was required in this test case. For tool A, he only had a rising edge step response. He noted the correlation with the rising edge is good, but the falling edge has significant difference in the tool A case. Arpad Muranyi asked if this was due to the difference between pulldown and pullup impedances. Randy replied, this is correct. Randy

noted tool B can include a rising edge and falling edge channel characterization, and both IBIS-AMI simulations give good correlation to the transient results. For tool C, the results are good for both cases compared to transient. Randy added he does see some differences between the transient results from all 3 tools. From the transient eye diagrams, you can see the asymmetric eye. He showed with tool A the IBIS-AMI results are symmetric. The IBIS-AMI results from tools B and C show an asymmetric eye. With the EQ enabled the eyes are expected. There are some differences in the eye heights and eye widths. He noted he is generally happy with the results, but he would like to see continued improvements in this area.

Walter Katz commented there are 3 non-linearities. The rise and fall time differences were described in papers at last year's DesignCon IBIS summit. The second is the rising and falling impedance differences. He noted the reflections coming back to the Tx can be tough to deal with, since these are time varying effects. The third is for Tx equalization in the area of the transition where the impedance will be non-linear in the FFE taps. Walter noted these will be difficult to capture, and these may require some pre-analysis to factor in these impairments.

Michael Mirmak asked on slide 10 if the probe is after the Rx and if we are using ideal clocking. Randy noted the probe is after the Rx, and this is using ideal clocking. Michael asked if these results do not include any jitter parameters. Randy replied no Tx or Rx jitter was added.

A question was asked about the transient and whether that was generated with a SPICE model. Randy noted the transient simulations were run with standard IBIS models.

Pegah Alavi asked if these results were correlated to measurements or SPICE model results. Randy replied this had not yet been done.

A question was asked about the non-linearities and if these are worst case. Randy noted we are limiting the swing, and the impedances are causing differences in how the reflections are coming back from the driver.

Arpad asked if Randy had tried to use Verilog-A models to compare to the other simulators. Randy noted this could be a way to simulate with a short bit pattern to consider the non-linearities, but he has not yet tried this.

## **IBIS-AMI MODELING AND SIMULATION OF DDR5 SYSTEMS**

Fangyi Rao\*, Hee-Soo Lee\*, Jing-Tao Liu\*, Wendem Beyene\*\*  
(Keysight Technologies\*, Intel Corp.\*\* , USA)

[Presented by Fangyi Rao (Keysight Technologies, USA)]

Fangyi Rao presented work using IBIS-AMI for DDR5 system simulations. He noted that DDR5 has added equalization features such as DFE to reduce ISI. He also highlighted the need to run a large number of bits to calculate low BER rates. He compared SerDes and DDR, where DDR is single-end and lacks a CDR. IBIS-AMI is new for DDR and there are many challenges. The common mode issue for single-ended signaling will be addressed with BIRD197, which adds the DC\_Offset parameter. The input to the GetWave function is centered around 0V and the DC\_Offset is a constant passed into the Rx DLL. The Rx DLL can choose to reconstruct the waveform with the DC\_Offset parameter. The EDA simulator can also display the waveform with DC\_Offset considered. Fangyi noted DDR can have asymmetric eyes with shifted crossing

points. He showed results comparing SPICE simulation and IBIS-AMI simulation using asymmetric edges and IBIS-AMI using symmetric edges. The symmetric eye is not as accurate.

Fangyi reviewed the DFE clocking in the clock forwarded system with a DQS used to clock the data. He proposed a new GetWave function which includes a “\*wave\_ref” as a signal input for the forwarded clock DQS. The function is otherwise the same as the existing GetWave. He gave an example of a controller Rx model block diagram, which includes a CTLE, gain, and DFE clocked by DQS. The controller Rx uses a phase interpolator to align the clock to the data and achieve the optimal DFE clocking. For the DRAM, there is no phase interpolator and it directly clocks the DFE slicer. The skew of the DQ and DQS is aligned by the controller during write leveling. He noted in DDR4 the receiver DQ and DQS paths internal to the devices are matched. DDR5 has an unmatched receiver with different DQ and DQS delays, which can cause uncorrelated jitter at the slicer. He showed results that include S<sub>j</sub>. The jitter tracking can eliminate the S<sub>j</sub>. He added 5UI delay to the DQS, which impacts the jitter correlation.

Michael Mirmak asked, on slides 9 and 12, how the new GetWave function works structurally. Fangyi replied they have separate DLLs for DQ and DQS. Adrien Auge asked what the reason for two different models is. Fangyi noted they are two different buffers.

Justin Butterfield asked how to align the clock for DRAM. There is a phase interpolator for the controller. Fangyi responded that this is not clear. The EDA tool could do write leveling, then apply that to the simulation.

Walter Katz commented there are some implications for the model makers and the users with this approach. Walter noted the DQS block has significant delay. Normally S<sub>j</sub> will cancel, but that may not always be the case. Walter commented, for a wide-bus simulation for reads, the skew is defined by the standard, but for writes, the skew is adjusted by the controller. In order to get the correct crosstalk, the write-leveling must be considered. Fangyi commented the case is different for writes where the controller sets the skew. For reads the phase interpolator handles the skew.

Ambrish Varma asked if the DQS delay was included in the study. Fangyi replied this was included.

Sunil Gupta asked how the DC\_Offset is used. Fangyi commented the DC\_Offset value is passed to the IBIS-AMI executable. Sunil asked if this was the same as VREF. Fangyi stated the VREF is different.

## **IBIS-AMI & COM CO-DESIGN FOR 25G SERDES**

Nan Hou#, Amy Zhang#, Guohua Wang#, David Zhang#, Anders Ekholm##  
(Ericsson, PRC#, Sweden##)  
[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm presented on work looking at IBIS-AMI and COM co-design for 25Gbps SerDes. He noted it can be difficult to optimize tap settings in the lab. His goal is to predict tap settings with COM and IBIS-AMI simulation. He gave an overview of the IBIS-AMI simulation flow. He showed the statistical eye flow and the time-domain flow using GetWave. Anders gave an

overview of COM, which looks at signal-to-noise ratio (SNR) for several standards using channel characterization. One could do SNR based on IBIS-AMI simulation. He gave an overview of the COM flow he used, which allows for an exhaustive sweep of the tap settings to give the best SNR. The approach takes the same tap settings from COM and uses these settings in a crosstalk analysis. The COM calculation is based on the transfer function. COM does not look at eye height, as it is only considering SNR. He would like to use COM early in the design cycle to see if the design will work. The idea is to extract the channel performance from the COM calculation, get the tap settings, and use these settings in the IBIS-AMI simulation.

Anders compared two examples. He used mostly default settings from the specification in the parameter settings. COM may not be most useful for optimizing other metrics besides eye height, such as power consumption differences from use of DFE vs. FFE. The first channel was an 8-inch channel with a lossy FR4 dielectric. He ran scripts to perform the COM calculation and predict the tap settings. The same tap settings were used in an IBIS-AMI simulation. He plotted eye heights and eye widths for over 80 cases to find the best case. Case 1 works with only CTLE, no DFE. The second example was a 24-inch channel. This channel does not meet the insertion loss requirement and requires DFE. He plotted 100 cases of eye height and eye width, and in this case, COM gave a good starting point for the tap settings. IBIS-AMI sim shows there are other possible best settings of equalization. He proposed a co-design simulation flow, since we have done an exhaustive sweep of the tap settings with COM. This can be a good approach to test if the channel will work and get a first pass of the tap settings. Next steps include adding crosstalk, 56G PAM4, IBIS-AMI correlation, measurement correlation, and improving the prediction of the tap settings.

A question was asked if the channel is known. Anders noted that in his experience the adaptation does not work in many cases, and we need to prepare for this case. Walter Katz commented the COM assumes the DFE adapts perfectly.

Michael Mirmak asked, since COM does not include jitter, if these are fair tests with an eye height limited case and if there are similar tests with eye width limited channels. Anders noted the loss is the priority in his systems. This could behave differently for channels with more reflections, but this is untested currently.

## **GAP IN IBIS FOR SAMPLING WITH STATISTICAL MODE AMI MODELS**

Todd Bermensolo\*, Hansel Dsilva\*\*, Michael Mirmak  
(Keysight Technologies\*, Achronix Semiconductor Corp.\*\* , USA)  
[Presented by Todd Bermensolo\*, Hansel Dsilva\*\*, Michael Mirmak (Keysight Technologies\*, Achronix Semiconductor Corp.\*\* , USA)]

Todd Bermensolo presented on a gap in IBIS for sampling in IBIS-AMI statistical mode. He reviewed the IBIS-AMI statistical mode of simulation going from a channel impulse response to a statistical eye diagram. He compared the IBIS-AMI statistical to COM and convolution-based simulation methodologies. He also reviewed the GetWave function noting that the clock\_times is an output of the model to control the sampling in the time-domain. For a pulse response, where we select the cursor can have a big effect on the results. This decision will affect the voltage and timing margin, as well as the DFE tap selections. Todd outlined different methods and algorithms for selecting the main cursor tap, including peak of pulse, Mueller-Muller,



modified Mueller-Muller, and hula hoop algorithm. He noted the question is if we really need sampling information from AMI\_Init and what the impact is.

Hansel Dsilva outlined the experiments they ran to look at the sampling. They ran IBIS-AMI statistical in various EDA simulators with fixed settings. They bypassed the bring-in of the impulse response to remove differences in the EDA tool creation of the impulse response. The simulation setup was standardized to set the expectations for each EDA tool including the PRBS length, samples per UI, and fixed equalization settings. The channel response and equalization settings came from the COM script and the IEEE 802.3 channel. They compared the sampling index across six EDA tools and the COM tool. Hansel showed results comparing the tools with the different sampling methods including peak of pulse, Mueller-Muller, and modified Mueller-Muller. He noted that the results vary both in terms of eye opening and sampling point across the EDA tools and COM. The problem is there is no model feedback to the EDA tool. The second experiment shows the importance of sampling comparing peak of pulse and Mueller-Muller phase detectors, where the loss was swept. For the COM margin, the Mueller-Muller phase detector outperforms peak of pulse. He noted that the sampling point is critical to determine the signaling margins. When you have increased loss, the precursor is not considered in the peak of pulse. In the AMI flow, it is difficult to distinguish between the 2 phase detectors. He suggested that EDA tools are guessing the sampling in statistical mode.

Michael Mirmak commented that statistical simulation is useful for more linear circuits depending on the architecture. He noted that statistical simulation is useful for DOE analysis with many cases. This is a gap in the specifications where EDA tools must guess how to process the data. Michael would like to add sampling information for the model makers to accurately represent the device behavior and have control of the eye plotting. He suggested a few options which include, having a sampling index, options from EDA tools on phase detectors, sampling extraction method from the impulse response, and the IBIS-AMI model to provide the results directly which would output the metric. He suggested to continue the discussion on this topic.

Arpad Muranyi asked about the channel delay and the effect on the impulse response and if there are any ways to look at the length of the impulse response. He proposed to use this information to build the result.

Walter Katz commented once an EDA tool defines where it samples, this affects how DFE affects both sides of the eye. Once you have an eye, what is the metric the EDA tool will respond with or display? Standards like DDR5 say to use a mask because the shifting of DQS moves the mask around. PCI-56G has an eye and complex method of looking at eye contours to determine where to sample. The eye is a function of where you sample. SiSoft uses different rules files to apply each standard's method of defining the sampling point. He recommends creating a Reserved\_Parameter defining the standard with multiple options for rules you want. Michael stated in many cases generic models are proposed, but the problem is the specifications do not always give enough information to enable these types of models with sampling included. A message needs to go out to interface owners to tell them to put out enough information or put out a generic AMI model with sampling information.

Todd Westerhoff asked about EDA #4 and if the results are expected. Todd B. noted the difference in eye size was not expected. Todd W. suggested it could be a factor of two difference in the tool.

## **IBIS-AMI BACK-CHANNEL SYSTEM OPTIMIZATION IN PRACTICE**

Steven Parker\*, Matthew Kelly\*, Jared James\*\*, Ambrish Varma\*\*,  
Kumar Keshavan\*\*, Ken Willis\*\* (Marvell\*, Cadence Design Systems\*\*, USA)  
[Presented by Steven Parker\*, Jared James\*\* (Marvell\*, Cadence Design Systems\*\*, USA)]

Steven Parker gave an overview of the IBIS-AMI Back-Channel Interface. He highlighted that optimizing the Rx and Tx equalization together can give better results in most cases. He gave an overview of the Back-Channel process in the GetWave function flow. He reviewed the new Reserved\_Parameters used to define the BCI protocol in the AMI parameter file. A key topic for discussion is how two IC vendors can support an interoperable back-channel training.

Steven detailed the setup of a BCI training for 56G PAM4 with an IEEE channel. Marvell implemented the protocol, while Cadence implemented their protocol for the Back-Channel Interface. The two protocols were not compatible but accomplished the same task. The Marvell model was modified to use the same protocol as the Cadence model. He detailed how the packet of the protocol works.

Steven gave an overview of some lessons learned through developing the protocol. There was no formal command acknowledgment, and this made the debug more difficult. There was no sequence checking. The size of the GetWave from BCI\_Message\_Interval\_UI was important, as there is some delay in the feedback. They found a value of about 1000 to work well for their study. The BCI\_ID was also important, but there were some issues with using the same file, as it was not always clear who should write to the file and when.

Steven showed results where the co-optimized results were improved. He outlined ideas for improving the interoperability and suggested defining a protocol as a de facto standard. Another idea would be to have model makers open source their function API. IBIS could also standardize the protocol format.

Anders Ekholm asked about saving the BCI information in a file and if this could be done in memory. Steven replied this is how the IBIS specification is written. Walter Katz noted the only way we could get this BIRD approved originally was to have the EDA tool do nothing. He noted we would have to modify the AMI functions to enable this.

## **BIRD201 – BACK-CHANNEL STATISTICAL OPTIMIZATION**

Walter Katz, Eric Brock (The MathWorks, USA)  
[Presented by Walter Katz (The MathWorks, USA)]

Walter Katz presented on BIRD201, which is a proposal to perform optimization in the statistical simulation flow. He reviewed that BIRD147 allows for back-channel optimization in the GetWave flow. He noted BIRD201 is up for consideration in the Open Forum. The BIRD adds a new AMI Reserved\_Parameter BCI\_Training\_Mode. There is also a new function called AMI\_Impulse with new inputs to the function to handle the statistical optimization. Walter added the BCI BIRDS only describe the method by which the Tx and Rx models communicate. The model maker is responsible for determining the optimization methods and metrics.

Walter gave an example of a DDR5 interface equalization optimization. The results can be displayed from the statistical simulation, or they can be continued to be further optimized with GetWave. He gave an overview of the DDR5 receiver. The BCI protocol that was used included the Rx DFE taps and gain. The string gets passed back and forth from the Tx to Rx, where the Tx tells the Rx the DFE tap values. The Rx returns the metrics of eye height, eye width, eye area and BER. He noted this is a preliminary protocol, but we should settle on the metrics returned by the Rx model. The silicon vendors may want to contribute to the protocol. He showed results for a DDR5 time-domain simulation, where he did a sweep of the taps and compared statistical and time-domain.

Walter also looked at a 56G PAM4 SerDes example with significantly more adaptation combinations. This example optimizes in 30 seconds in statistical but takes hours in the time-domain. He commented these large solution spaces can be difficult to optimize both in simulation and in hardware. The next step is to use machine learning to do the co-optimization.

Anders Ekholm asked how to handle corners in these types of optimizations. Walter replied the big corner is temperature, since it affects the CTLE. One of the key points in the implementation is to have a function to control the optimization and have the same function in statistical, time domain, and hardware. The hardware could be trained at various temperatures. This could be built into a machine learning model, which can be used as a starting point then be fine-tuned.

Stefan Paret asked if it would be good to have a failed state to reflect an error. Walter noted this could be useful, but he has not had issues.

Anders asked if this is designed to optimize the eye opening rather than power. Walter commented you could penalize the high-power solutions in the optimization. This could be done with machine learning. Anders asked if this can be done with the current BIRD. Walter replied the BIRD only defines the protocol, but in the models, you can do what you want.

## **USE DATA SCIENCE TECHNIQUES IN IBIS-AMI MODELING**

Wei-hsing Huang (SPISim, USA)

Wei-hsing Huang presented on techniques for using data science in IBIS-AMI. He reviewed the IBIS-AMI file format requirements. The motivation for this work is to minimize the cases where we need to recompile the executable models. He used the model view control paradigm to minimize the coupling between the function components. Changes to the model could be made to an encrypted text file used by a more universal AMI executable. This can be used to make models of similar products, then changes between products can be handled more efficiently.

Wei-hsing outlined the AMI data science modeling process. This is a different data science from traditional machine learning as it does not require dedicated artificial intelligence processing such as with a GPU. He gave an example of a FIR equalizer, which can be made general using specification-based parameters. He noted another example is to use silicon and measurement data as an input to the model to form a lookup table controlled by datasheet parameters. This works for categorical data where there is exact mapping, but if not, you will need to perform interpolation.

Wei-hsing gave a third example where there is incomplete, insufficient, or low-quality data, and the model needs to predict the behavior with techniques such as DOE, RSM or regression. He noted there are open source Python libraries to fit the equation with a Linear Regression, such as the case for a Tx FIR. For a CTLE, equations can be used to model the pole-zero data. He noted we need to have a transform to convert to a time-domain response. Hard coding the pole-zero data in the executable model should be avoided. For performance-based models, the input is your performance metric and the outputs are the pole-zero data. For the neural network model fit he used the Keras library, which is open source and can be converted into C++ code and compiled to an executable model. The results of the training in weights can be exported to a text file and read from the AMI model.

Randy Wolff asked if there are any recommendations for encryption tools. Wei-hsing replied he does not want to expose details and used CryptoPP, since it is an open source encryption tool and will embed the keys in your executable.

A question was asked why the translation was done from Python to C++. Wei-hsing commented the rest of the model code was in C++. A question was asked about the data science and if it can work on a CPU. Wei-hsing replied, since this is a simple neural network, it can operate on a CPU.

Wendem Beyene asked if the Keras code was open source. Wei-hsing replied the Keras library is open source and you can view the code.

## **THE ON DIE DECAP MODELING PROPOSAL (BIRD198)**

Atsushi Tomishima\*, Megumi Ono\*\* (for JEITA)

(Toshiba Electronic Devices & Storage Corporation\*, Socionext\*\*, Japan)

[Presented by Genichi Tanaka (Renesas Electronics, Japan)]

Genichi Tanaka presented the on-die decap modeling proposed in BIRD198. Last year Megumi Ono presented a proposal to provide a power delivery network model in IBIS. Tanaka-san noted there have been many papers in the IBIS summit meetings on power delivery and on-die decoupling capacitance. It is difficult for the system designer to get the on-die decoupling capacitance information for the IC. They receive guidelines for the PDN requirements, but not the on-die decoupling capacitance. There is no standard format for the IC vendors to provide the models to their customers. They have proposed BIRD198 to add the on-die decoupling capacitance, which is a simplified decoupling capacitance model.

Tanaka-san showed a comparison of results with and without the on-die decap. He compared the original proposal to the current proposal, which has been updated based on feedback and discussion with the ATM task group. The latest proposal uses bus\_label and signal\_name and has new keywords at the component level. This is easier to implement for the EDA tool vendors. He gave a case study of an LSI device with different power rails and an example of the syntax using the latest BIRD198 proposal. The order of the columns is not important as these define the conditions. The latest feedback from the ATM group focused on how to specify the keywords and the default values if they are not specified. He recommended requiring all the value parameters to avoid mistakes and requiring the parser to check for these. He plans to issue a BIRD198.1 in March.

Michael Mirmak asked if this is for DDR-like interfaces or if there are other applications. Tanaka-san stated there are other applications that can use this syntax. Bob Ross noted this can be in a regular IBIS model.

A question was asked about on-package decoupling capacitance. Tanaka-san replied the IBIS 7.0 Interconnect syntax can be used to model the on-package decoupling capacitance.

Raj Raghuram asked about the inductance of the capacitance. Tanaka-san stated that this is not needed for the on-die LSI capacitance. Randy Wolff noted that IBIS 7.0 could be used for this to create a more complex model.

Stefan Paret asked about having 0s or very high resistance for the default values, as these values could lead to numerical or non-convergence issues in simulation. Tanaka-san noted that for very simple early models, these values might be included before the actual values are known. Stefan commented, if it is not intended to be there, it is best to not include the element.

## **EMD MADE SIMPLE**

Bob Ross (Teraspeed Labs, USA)

Bob Ross presented on the Electrical Module Description (EMD) proposal, which is now BIRD202. This BIRD has been the subject of the Interconnect Task group's work recently. This is a new syntax to replace the EBD syntax for modules and stacked packages. Bob gave an overview of the terminology in the BIRD. Interfaces are the key connection points. Terminals are used to connect to the models, which is very similar to the Interconnect modeling syntax and supports both IBIS-ISS and Touchstone. The [EMD Pin List] keyword is the main external interface. The [Designator Pin List] keywords are the component or module interface pins. The columns include the designator pin, signal\_name, signal\_type, and optionally bus\_label. The bus\_label can be used to break up a rail into groups. The [EMD Designator Map] keyword is very similar to the EBD [Reference Designator Map]. The designator pin list supports pre-appended component designator and pin number. For the rails, each of the designator's pin\_names connects to one rail pin. Bob noted there are terminal and terminal\_type associations as detailed in the BIRD. He showed the syntax for the terminal lines. EMD also uses [EMD Set] and [EMD Model] keywords, which follow the Interconnect syntax.

A question was asked how a component could be connected in the middle. Bob stated the connection is made by the IBIS-ISS subcircuit. Randy Wolff stated that a buffer could be in the middle, such as on a Registered DIMM. Bob noted they are only connected when the syntax says they are connected. Some signal\_names do not have to be connected to same signal\_names. Bob noted this removes the one-to-one pin-to-buffer connections requirement in the Interconnect syntax.

Michael Mirmak asked which terminals would be in the ISS model. Bob replied the terminal numbers would match to the position of the subcircuit terminals.

Bob noted there is a separate .ems file to define the EMD Sets. The syntax also defines a .emd file which contains [Begin EMD], [EMD Group], and optionally [EMD Set]. The EMD Group selects the EMD Sets which could be in the same .emd file or in a separate .ems file.

Bob discussed the similarities with the Interconnect model syntax, where some of the syntax is similar with similar naming. EMD does not have the die pad or buffer interfaces as it only considers pins. He noted EBDs can reference EBDs and EMDs can reference EMDs, but they cannot reference each other. Some differences from Interconnect model syntax include the ability to split I/Os to multiple terminal interfaces (signal forking) and handling of rail terminals.

## **IBIS BASED BUCK CONVERTER DC MODELING**

Zhiping Yang, Songping Wu, Shuai Jin, Zhenxue Xu (Google, USA)  
[Presented by Shuai Jin and Zhenxue Xu (Google, USA)]

Shuai Jin presented first. He proposed that a model for a DC-DC Buck converter could be provided by vendors through a new IBIS model format. The switching and conduction power loss could be modeled through a set of key parameters. The simulation tool would calculate the power consumption in its own solver.

Zhenxue Xu presented the equations for calculating buck converter power consumption in continuous conduction mode. Future plans include modeling the power consumption in discontinuous conduction mode and modeling a boost converter.

Michael Mirmak noted that the examples of parameters shown in the presentation were all single-valued. He asked if they could be dependent on other parameters or require table driven values. Zhenxue responded that only single values are needed.

Walter Katz asked if the presenters had tried using a 3-terminal SPICE model implementation. How do you simulate today? They responded that the models are very time consuming to simulate. Full SPICE models are available, but they need a behavioral model.

Arpad Muranyi asked if single R values are ok or if I-V type curves would be needed. Zhiping Yang responded that it is adequate to start with a first order model.

Arpad asked if the presenters were looking for a subcircuit linkage in IBIS or modeling only through new parameters. Zhiping responded that they would like vendors to supply IBIS models with parameters and the EDA tools would implement a behavioral model.

Michael asked if Verilog-A could provide a solution. Arpad agreed that a behavioral model could be implemented this way. Zhiping added that he hopes to encourage vendors to provide models, so making the solution simple is best.

## **OPEN DISCUSSION**

None.

## **CONCLUDING ITEMS**

Randy Wolff again thanked the sponsors Cadence Design Systems, Keysight Technologies, and Synopsys, the presenters, organizers and attendees.

The meeting concluded at approximately 5:00 PM.

## **NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held on February 21, 2020, and votes are scheduled for BIRD197.7 and whether to hold an IEEE SPI Summit 2020. The following teleconference meeting is tentatively scheduled for March 13, 2020.

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## **NOTES**

IBIS CHAIR: Randy Wolff (208) 363-1764

[rwolff@micron.com](mailto:rwolff@micron.com)

Principal Engineer, Silicon SI Group, Micron Technology, Inc.

8000 S. Federal Way

P.O. Box 6, Mail Stop: 01-711

Boise, ID 83707-0006

VICE CHAIR: Lance Wang (978) 633-3388

[lance.wang@ibis.org](mailto:lance.wang@ibis.org)

Solutions Architect, Zuken USA

238 Littleton Road, Suite 100

Westford, MA 01886

SECRETARY: Curtis Clark

[curtis.clark@ansys.com](mailto:curtis.clark@ansys.com)

ANSYS, Inc.

150 Baker Ave Ext

Concord, MA 01742

TREASURER: Bob Ross (503) 246-8048

[bob@teraspeedlabs.com](mailto:bob@teraspeedlabs.com)

Engineer, Teraspeed Labs

10238 SW Lancaster Road

Portland, OR 97219

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40

[ibis-librarian@ibis.org](mailto:ibis-librarian@ibis.org)

Digital Modules Design, PDU Base Stations, Ericsson AB

BU Network

Färögatan 6

164 80 Stockholm, Sweden

WEBMASTER: Steven Parker (845) 372-3294

[sparker@marvell.com](mailto:sparker@marvell.com)

Senior Staff Engineer, DSP, Marvell

2070 Route 52  
Hopewell Junction, NY 12533-3507

POSTMASTER: Mike LaBonte  
[mlabonte@sisoft.com](mailto:mlabonte@sisoft.com)  
IBIS-AMI Modeling Specialist, SiSoft  
1 Lakeside Campus Drive  
Natick, MA 01760

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Organization	Interest Category	Standards Ballot Voting Status	November	December	January	January 31,
			22, 2019	13, 2019	10, 2020	2020
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	X
Cadence Design Systems	User	Active	X	-	X	X
Cisco Systems	User	Inactive	-	-	-	X
Dassault Systemes	User	Inactive	-	-	-	X
Ericsson	Producer	Inactive	-	-	-	X
Google	User	Inactive	-	-	-	X
Huawei Technologies	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	X	-	-	-
Instituto de Telecomunicações	User	Inactive	-	-	-	-
IBM	Producer	Inactive	X	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
Keysight Technologies	User	Active	X	X	X	X
Marvell (GLOBALFOUNDRIES)	Producer	Active	X	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	X
Mentor, A Siemens Business	User	Active	X	-	X	X
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	X
SerDesDesign.com	User	Inactive	-	-	-	X
SiSoft	User	Active	X	X	X	X
SPISim	User	Active	X	X	X	X
Synopsys	User	Active	X	X	-	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Xilinx	Producer	Inactive	-	-	-	X
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Active	-	X	X	X

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