DDR Simulation with IBIS-AMI

Randy Wolff, Justin Butterfield DesignCon IBIS Summit Santa Clara, CA January 31, 2020

©2020 Micron Technology, Inc. All rights reserved. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Statements regarding products, including statements regarding product features, availability, functionality, or compatibility, are provided for informational purposes only and do not modify the warranty, if any, applicable to any product. Drawings may not be to scale. Micron, the Micron logo, and all other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.



Introduction

- IBIS-AMI simulation flows adopted for single-ended (SE) signaling (DDR5, LPDDR5, etc.) in the last 1+ years
- EDA tools are implementing unique AMI solutions to SE signaling challenges
 - Common mode voltage
 - -Tx non-linearities (rise/fall impedance and slew rate differences)
 - Forwarded Clock (DQ Strobe)
- What do these solutions look like?
- How do tools differ?
 - Subset of tools compared in simulation of LPDDR5 channel
- What's next to improve simulation flows and accuracy?



EDA Tool Comparison – Summary Table

| Tool / Features | А | В | С | D | E | F |
|---------------------------|----|-----|-----|-----|-----|----|
| Multi-Edge Time-domain | No | Yes | Yes | Yes | No | No |
| DC Offset | 0V | Yes | Yes | 0V | Yes | 0V |
| External Clock | No | Yes | No | No | No | No |

- Multi-Edge Time-domain can help improve accuracy by including more non-linear Tx effects
 - May include both rising/falling edge or multi-edge channel characterization
- DC Offset refers to the waveform input to AMI_GetWave being offset by the DC common mode voltage
 - If the DC Offset is included, the model user must set the Rx Vref AMI parameter to the DC common mode value.
- External Clock capability is currently untested. Several tools starting to add capability in new releases.



Simulation Setup

LPDDR5 DQ READ, Note: only tools A, B, and C compared in following slides

- 6.4Gbps
- Tx with 60 Ohm pulldown
- 80 Ohm ODT at each DRAM
- Rx DFE tap 1 set to -20mV





Tool A

Transient vs. AMI with Rising Step Channel Characterization



Probe 1: Green=transient, Red=AMI rising char.



Tool B

Transient vs. AMI with Rising and Rising/Falling Step Channel Characterization



Probe 1: Green=transient, Red=AMI rising char., Blue=AMI rising/falling char.



Tool C

Transient vs. AMI with Rising and Rising/Falling Step Channel Characterization



Probe 1: Green=transient, Red=AMI rising char., Blue=AMI rising/falling char.



Transient Sim. at Probe 1: Tool A/B/C Comparison





AMI Sim. at Probe 1: Tool A/B/C Comparison



and C results use rise/fall edge channel characterization



AMI Sim. at Probe 2 (-20mV DFE): Tool A/B/C





Results Summary

Eye Diagram Measurements

| ΤοοΙ | Metric | Transient | AMI | AMI -20mV DFE |
|------|-----------------|-----------|-----|------------------|
| А | Eye Height (mV) | 130 | 128 | 138 |
| | Eye Width (ps) | 122 | 142 | 147 |
| В | Eye Height (mV) | 133 | 136 | 140 |
| | Eye Width (ps) | 132 | 141 | 146 |
| С | Eye Height (mV) | 138 | 148 | 153 |
| | Eye Width (ps) | 131 | 144 | 145 |



Summary

- Multi-edge channel characterization is improving AMI simulation accuracy for non-linear Tx
 - Still room for improvement
 - -Tx models with Equalization have not been tested for accuracy
- EDA tools are inconsistent with handling of DC common mode voltage in the input waveform to the Rx AMI_GetWave
 - Requires a Rx Vref parameter be set by the user specific to the EDA tool
 - -BIRD197.7 should clarify this, but some tools will need to change their existing flows
- External Clock for Rx AMI models needs further attention
 - -BIRD will be needed to define this



