IBIS Open Forum Summit Minutes

Meeting Date: **July 28, 2009**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2009 PARTICIPANTS

Actel	(Prabhu Mohan)
Agilent	Brian Andresen*, Radek Biernacki*, Saliou Dieye, Yutao Hu, Fangyi Rao
AMD	Nam Nguyen
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
ARM	V. Muniswara Reddy
Cadence Design Systems	Terry Jernberg, Ambrish Varma
Cisco Systems	Luis Boluna, Tram Bui, Bill Chen, Syed Huq*, Mike LaBonte, Pedo Miran, Huyen Pham, AbdulRahman (Abbey) Rafiq*, Ashwin Vasudevan, Zhiping Yang
Ericsson	Anders Ekholm*
Green Streak Programs	Lynne Green*
Hitachi ULSI Systems	(Kazuyoshi Shoji)
IBM	Adge Hawes
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Myoung J. Choi*, Michael Mirmak*, Vishram Pandit*, Jon Powell, Sirisha Prayaga
IO Methodology	Li (Kathy) Chen, Lance Wang*, Zhi (Benny) Yan
LSI	Brian Burdick
Mentor Graphics	Weston Beal, Vladimir Dmitriev-Zdorov, Zhen Mu, Arpad Muranyi*
Micron Technology	Randy Wolff
Nokia Siemens Networks GmbH	Eckhard Lenski
Samtec	(Corey Kimble)
Signal Integrity Software	Barry Katz, Walter Katz*, Todd Westerhoff
Sigrity	Brad Brim*, Sam Chitwood
Synopsys	Ted Mido
Teraspeed Consulting Group	Bob Ross*
Toshiba	(Yasumasa Kondo)
Xilinx	[David Banas]
ZTE	(Ying Xiong)
Zuken	Michael Schaeder, Ralf Bruening

OTHER PARTICIPANTS IN 2009

AET	Mikio Kiyono
Altera	Hui Fu*
Ansoft Corporation	Steve Pytel
Apache	Yu Lin*
ATE	Nob Tanak*, Kenny Suga*
Bayside Design	Stephen Coe, Elliot Nahas
Circuit Spectrum	Zaven Tashjian
CST	Antonio Ciccomancini, Martin Schauem
Curtiss-Wright Embedded Computing	J. Phillips
EM Integrity	Guy de Burgh
Exar	Helen Nguyen
Freescale	Jon Burnett, Om Mandhama
Huawei Technologies	Xiaoqing Dong, Chunxing Huang, Guan Tao
ICT Solutions	Steven Wong
IdemWorks	Michelangelo Bandinu
Juniper	Kevin Ko
Kineret Design	Ricardo Teliuteuesh*
Leventhal Design & Communications	Roy Leventhal
Maxim Integrated Products	Ron Olisar
Mindspeed Technologies	Bobby Alkay
NetLogic Microsystems	Eric Hsu
Politecnico di Torino	Igor Stievano
Sanmina SCI	Vladimir Drivanenko
Sedona International	Joe Socha
Siemens	Manfred Maurer
Signal Consulting Group	Timothy Coyle, Nicole Mitchell
Simberian	Yuriy Shlepnev
TechAmerica (GEIA)	(Chris Denham)
Texas Instruments	Pavani Jella
Xsigo Systems	Robert Badel
Independent	Ian Dodd

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The logistical details of future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
August 7, 2009	207 965 694	IBIS

For teleconference dial-in information, use the password at the following website:
https://cisco.webex.com/cisco/j.php?J=207965694

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, press 1 to attend the meeting, then follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in San Francisco, California at the Westin Market Street Hotel San Francisco during the 2009 Design Automation Conference. About 19 people representing 13 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/ibis/summits/jul09/

Michael Mirmak opened the meeting by welcoming the attendees. He thanked Mentor Graphics for sponsoring the event. He then asked people in the room to provide brief introductions for themselves.

CHAIR'S ANNUAL STATUS REPORT

Michael Mirmak, Intel Corporation

Michael highlighted several recent achievements, including the approval of Touchstone 2.0, the progress on development of an IBIS 5.0 parser, finalization of revision 1.1 of the IBIS Quality Specification and work on a standard SPICE subcircuit representation for interconnects. He noted that membership renewals were slightly lower than necessary, but that recent economic turmoil had not seriously affected IBIS Open Forum activities. He predicted a rise in BIRD submissions and appealed to the members to purchase IBIS and Touchstone parsers. Michael concluded with a few personal observations regarding ways in which organizations and individuals can be most effective in standards work.

TOP 10 ISSUES AS SEEN DURING IBIS MODEL REVIEWS

Lynne Green, Green Streak Programs

Lynne presented an overview of the IBIS Model Review committee's procedures. She noted that IBIS, Touchstone, *-AMS and AMI models are eligible for review. Half of the submitted models are not distributed to reviewers other than Lynne because they are so poor. Typically, Lynne executes parser and graphical checks before models are distributed to reviewers. Reviewers donate their engineering time to review, and are only required to be employed by an EDA

vendor. The committee cannot accept models from EDA vendors or IC vendors. Trends are that more reviewed IBIS files are passing IBISCHK4, with more migration from s2ibis2 to s2ibis3 being seen. New issues include proper extraction of data and use of keywords for differential models.

Lynne summarized her top-ten list. The first four items are related to headers. In particular, she noted that parentheses tend to break existing tool flows, including their use in copyright notices. She also mentioned having an Rref value for timing test loads and R_load for ramps above 200 ohms can cause issues with currents in simulations, due to SPICE resolutions being expressed in percentages. Non-monotonic data can also cause convergence issues. Not as many issues have been seen regarding waveforms ending too soon in terms of V-t tables, but more often ending too late – too little transition is provided for a lot of unchanging waveform data. Lynne added that tools are getting smarter about handling extra V-t data. Other common data issues include ringing due to I/O behavior instead of package issues and improperly adjusted clamp curves.

Lynne ended with speculations regarding variations in quality. Employees who do good IBIS modeling work may get promoted out of their position, leaving interns and junior engineers to do the work. This causes issues, particularly with complex structures such as differential models. As time passes, Lynne has to communicate less with the originators and reviewers, with over half of the incoming models going straight to reviewers. A need still exists for the committee.

Lance Wang asked whether true differential models are coming in and/or being reviewed. Lynne responded that they do show up in large files, usually containing 20 or 30 models. Arpad Muranyi asked who the Mentor and SiSoft reviewers were. Michael Mirmak asked about updates to the IBIS and IBIS quality specifications using differential model examples. Lynne responded that she did not see changes being needed yet. Arpad Muranyi asked whether the specification has any issues on differential loads such as Rdiff and Cdiff. Lynne stated that she was aware of no issues in the specification, but complete descriptions were missing in the Cookbook.

IBIS QUALITY REVIEW

Mike LaBonte, Cisco Systems (presented by Bob Ross, Teraspeed Consulting Group)

Bob Ross reviewed the history of the IBIS Quality Committee. The original specification version used a numbering sequence involving 0 as passing the fundamental checks of IBIS. The new definitions in the IBIS Quality Specification version 1.1 use “IQ0” as meaning "not checked". Special designators in the new definitions include “X” for a waiver of parser rules. Note that the “IQ4” level specifically describes checking vs. power integrity. Level 3 checks include timing, which now covers RLCs for pins. Power integrity checks include the [Pin Mapping] keyword as a minimum requirement. Several sections were removed or minimized in 1.1, with some debate over overshoot requirements. Some tentative updates are being discussed, once version 1.1 is deemed complete. Because the changes are substantial, the Quality Committee is likely to elevate this version from 1.1 to 2.0.

Bob noted that regular participants in IBIS Quality activities include model makers from IC vendors. He continued by summarizing recent problems considered by the Quality Task Group. Some DDR support issues involve JEDEC definitions and dependencies, particularly with [Receiver Thresholds]. A known issue is whether IBIS has the keywords to deal with the specific JEDEC requirements.

Lance Wang asked about any future directions for IQ checks specific to interconnect models like Touchstone 2.0 or package models. Bob responded that these are mixed objectives as IQ doesn't deal with extensions of IBIS concepts but only with basic IBIS. At this point, the IBIS Quality Task Group does not have the skill set or time to deal with ICM, S-parameters, power integrity, algorithmic models or multi-lingual models. Lynne Green added that the Cookbook has some of the same issues, as no cookbook support exists for multi-lingual models or Touchstone 2.0 issues. Arpad Muranyi observed that, for IBIS quality purposes, there's not much checking that can be done in IBIS-AMI, as so much is determined by the executable content of the model. Bob responded that these are possible discussions but that going too deeply into certain areas is impossible due to the volunteer nature of group. Walter Katz stated that the group must distinguish, per Michael Mirmak's presentation, between what is needed versus what is possible, meaning that quality efforts need to address the pin section and the I-V and V-t data sections. Everything else is not used, at least by SiSoft. JEDEC specifications, not IBIS, are observed after that point, with derating being added as a proprietary keyword. Slew rate rules are an example of changes that are needed in the IBIS specification. Walter continued, noting that lots of items were added to IBIS that are premature. Bob responded that a key issue is prioritization, as certain second and third level obscurities just cannot be addressed.

CASE STUDY: ANALYZE THE DIFFERENT RESULTS FROM IBIS SIMULATORS

Lance Wang, IO Methodology

Lance reported on results observed when using an unusual IBIS model under four major SPICE/IBIS tools. The model uses a 1.2 V supply, is output-only and uses differential pin, but has only pulldown and pullup curves defined. Only one set of V-t curves is provided: 1 rising and 1 falling. The model passes IBISCHK 4.2.2 with no errors or warnings.

A first test with simple stimulus into a differential load showed radically different results in output between four different simulators. Three simulators encountered a time shift or delay; the fourth tool showed completely different output DC levels. Arpad Muranyi noted that the DC levels in the I-V tables may cause a shift in output. Lance's second test involved connecting the driver to an IBIS receiver through small series resistors. Simulator 1 now caused mismatches in differential outputs relative to the other tools. Arpad identified this as a V-t issue, asking why the parser did not catch the V-t issues. Lance responded that this was due to having a single V-t table only. The problem is with the receiver load (5 ohms) and how small it is relative to the driver characterization load (100 ohms). Lance also noted that the I-V tables are inconsistent. Arpad responded that this was a given once only two V-t waveforms were given as part of the model. Lance highlighted that the proper approach is to use the working voltage range for creating consistent IBIS models. Taking out the V-t tables and only using ramps results in consistent output from simulator 1, but the DC output is still undesirable in terms of its offsets per single-ended response. Michael Mirmak suggested this was a good application of the [Test Load] and [Test Data] keywords. Bob Ross asked whether Lance could send the model out for analysis. Lance responded that this was not possible, but that he could put simulator teams in touch with the vendor. Arpad asked whether the point of the presentation was to show how bad EDA vendors are. Lance responded that he wanted to remind participants that they should not ever think that simulators never "guess." Arpad noted "garbage in, garbage out," in that the parser and IBIS quality checks will only tell you generic syntax and check points, but will not address specifics.

SI/PI CO-SIMULATIONS FOR I/O INTERFACES

Myoung Joon Choi and Vishram Pandit, Intel Corp.
Joon began by asking the audience to view him as a user, presenting a summary of a specific application. Joon observed that having an engineer just perform SI or PI analyses separately will miss some key effects. Sockets can have power-to-signal cross-talk, as an example. For good analyses, power grid and Cdie, Rdie effects are absolutely required. He presented a method for how peak distortion analysis and complete system models can be used to analyze power delivery and signal integrity together. Walter Katz commented that, for board, package and device power delivery (PD) analyses, we need the equivalent of a bedspring model. Joon noted that he and his team use S-parameters, but a distributed model is certainly required. Arpad Muranyi asked whether the system model assumes connections are localized between buffers and PDN grids. Joon answered yes, with ports connecting to the on-die power grid. Arpad followed up by asking whether the combined SI and PD model includes gate modulation effects. Joon confirmed this, adding that variation of the current through the buffer was also included.

Joon noted that the team needed to support several simulation tools, so a coworker developed a tool to combine an IBIS 3.2-style model with PDN currents. Verilog-A can do this, but the algorithm to do this is a topic for another day. The model used is based on IBIS-table-driven data in Verilog-A, with data on power supplies to substitute for ISSO_PD, ISSO_PU, etc. The system relies on 2D and 3D models, with S-parameters. Walter asked whether this analysis included 300 separate buffers. Joon answered that effects do not propagate too widely, so only localized areas were studied, to look for resonances. Syed Huq asked whether this includes core current switching profiles. Joon responded that, if it is on the same domain, Icc(t) can include this. This presentation data is from a different domain, so core currents were not included (for example, interactions between DDR and PCI Express). Joon noted that new tools appear to be doing fairly well at converging in the time domain, and explained the minimum model requirements for S-parameter or frequency-domain data. By analyzing combined responses between ISI, crosstalk and SSN, decomposition of individual effects can be performed. Anders Ekholm asked whether crosstalk multipliers assume perfectly aligned, in-phase signaling. Joon stated that this particular one assumes in-phase, but not much out-of-phase is assumed. Walter asked what Intel assumes customers will do with this data; are they expected to use all this data? Joon responded that this assumption is not warranted. This analysis is for internal use but is also useful for platform design guidelines. Walter responded that he, as a designer, would want his tool to be able to analyze what the eye at the receiver looks like, as not everything is included in the buffer model. Joon noted that simulations of 70 ns in duration take only a few hours for the full system. Walter asked several questions about where PDA applies. Syed Huq followed up by asking whether LTI assumptions truly apply to the buffer being used. Joon responded that the SI-PI combination seems to cause a superposition error, even if SI and PI responses are LTI independently.

Joon showed correlation data with PDN probed on-die. Package and Cdie decoupling capacitance comparison shows “no free lunch” – a reduced number of layers in the package means adding more Cdie to compensate. Increased Rdie in the package reduces resonance points in Z plane, so peak noise gets reduced with bigger Rdie, but overall the peak-to-peak envelope gets bigger. Architectural controls can limit some of these issues. Joon concluded by mentioning investigations of keywords in IBIS 5.0, as designers need accuracy for good simulation. Michael Mirmak commented that issues have been observed with causality and passivity for combined S-parameters (cascades), which may explain the non-passivity, non-causality behaviors. Lynne Green added that the same problem exists with cascaded transmission lines of equal characteristics. Arpad Muranyi asked what the message to the summit attendees is. Joon answered that some teams are moving toward SI-PI co-simulation,

so buffer modeling accuracy is critical. Here, the designers are using IBIS data under Verilog-A, but if IBIS can support this co-simulation directly, the analysis process would be a lot easier. Syed noted that what is needed by Cisco is very similar to what Intel does, adding that, while lots of information is proprietary, the core current profile needs to be standardized.

ELECTION OF OFFICERS

Michael Mirmak announced the available positions and responsibilities. He also presented the nominees for the various positions and the process for conducting elections. Two nominations were received before the meeting for the position of Librarian: Pavani Jella of Texas Instruments and Eckhard Lenski of Nokia Siemens Networks. All other positions only received one nominee each.

During the meeting, Lynne Green nominated herself as a candidate for Librarian. Anders Ekholm was also nominated for Librarian. Michael invited the candidates present to make public statements regarding their candidacies.

Nine (9) member companies were present at the meeting at the time of the election. A paper ballot was issued for the election of the librarian, but no candidate received a majority of votes and the two candidates to receive the most votes were tied. A second paper ballot was issued as a run-off between these two candidates.

The following individuals were elected by the voting membership present at the Summit as officers for 2009-2010:

Chair:	Bob Ross, Teraspeed Consulting Group
Vice-Chair:	Lance Wang, IO Methodology, Inc.
Secretary:	Randy Wolff, Micron Technology
Librarian:	Anders Ekholm, Ericsson AB
Webmaster:	Syed Huq, Cisco Systems
Postmaster:	Mike LaBonte, Cisco Systems

Michael thanked the outgoing officers and congratulated the new officers. Michael then presented some commemorative items to the outgoing board members, and Bob Ross presented one to Michael.

SERIAL LINK / IBIS-AMI TERMINOLOGY REVIEW

Walter Katz, Signal Integrity Software (SiSoft)

Walter summarized his presentation as a method to summarize the terminology, assumptions and intent behind IBIS-AMI. Syed Huq asked what happens if the transmitter output is nonlinear. Walter noted that a solution exists, but in general this does not happen. In general, compensation can be done to linearize the operating region.

Walter presented the equations being used in IBIS AMI and the assumptions behind them. All models must have the INIT function, with GetWave being optional. An all-INIT system is essentially equivalent to the StatEye open-source program. INIT supports peaking and FIR filters, but non-linear features like DFE drives need GetWave. The flow shown in the presentation should include stimulus going into the transmitter's GetWave, rather than resulting from the analog channel. Syed asked where the impulse response comes from. Walter answered that this comes from the channel. He added that the IBIS ATM team is looking to

make Touchstone files an option for buffer analog response. A participant asked whether the analog model is always completely linear. Walter confirmed this. He added that transmitter AMI GetWave as currently written implies compensation is done for an unknown receiver; this will be completed in the future. Lynne Green asked whether the DLL or EXE file must support N different tools. Walter answered that multiple operating systems must be supported, not tools. A representative from Apache suggested that Linux issues might arise across versions, as Redhat has different versions, etc. Richard Teliuteuesh responded that this occurs only when the DLL depends on other DLLs. Lynne noted that the parser is a good equivalent example. Syed commented that TX and RX have to be compiled under the same OS to make the tool work.

TOUCHSTONE TO TOUCHSTONE 2.0, TOUCHSTONE 2.0 TO TOUCHSTONE TOO

Bob Ross, Teraspeed Consulting Group

Bob began by noting that he was providing a "low-level" presentation on the history of Touchstone and Touchstone 2.0. The motivation for enhancing Touchstone to Touchstone 2.0 was to avoid making major changes but improve support for S-parameters in common applications. Initially, interest by IBIS in Touchstone was based on ICM needs. Bob noted that a Touchstone 2.0 parser is likely to be available soon. Lynne Green asked about a specific timeline. Bob responded that the parser is likely to be released within three months. Bob next showed the fixed format of S-parameters from Touchstone 1.0. He noted that Touchstone 2.0 has 13 keywords and provided simple explanations for each. He continued that upgrading to Touchstone 2.0 from the original format is simple, adding that the new mixed-mode format will work very well for single-ended port remapping. Downgrading from 2.0 to 1.0 is somewhat difficult, unless the tool being used retained both Touchstone and Touchstone 2.0 export rules. In this case, the user may simply remove keywords, remove [Matrix Format] and carefully check [Two-Port Data Order]. Radek Biernacki noted that reference impedances must be the same for all ports in this case. Bob continued that Y- and Z-parameters are much the same between versions, except that technically the original Touchstone format describes normalized Y- and Z-parameters whereas Touchstone 2.0 defines them as un-normalized. So software is needed to support such conversions. H- and G- transformations might be supported under general-purpose converters. Future support of sparse matrices, being considered by the IBIS Interconnect Task Group, means enormous reductions in file size. Bob concluded by suggesting that a great student project would be a general conversion utility for Touchstone 2.0.

MODEL CONNECTION PROTOCOLS FOR CHIP/PACKAGE/BOARD

Brad Brim, Sigrity

Brad summarized his presentation by noting that mapping of die pad to package nets and nodes is difficult and non-standard. Today, in Touchstone 2.0, the task group is discussing how to match nodes and port names. Many people ask, "How do I wire this stuff up?" In a netlist, many will do it manually but in an EDA tool, you can do this automatically. Sigrity has a solution, which is not being proposed as a standard but is just being shown as an example. A key issue is that not all connections have pin-level resolution. Many physical connections exist, making manual attachments difficult. For nets or net-level models, such as "ground", tools can lump all ground bumps together, but this inadequately groups signals together into a single net. For example: try to move a probe around a chip and look at the PDN. The resulting impedance may vary as much as 5:1.

Industry needs to support mixed models in a system (net-based, pin-based and grid-based). Such a model format could support connectors, but most format authors have chosen not to.

Pin-level connections would need to be added, and are now implemented as comments in either (a) data models or (b) SPICE-level circuits. Walter Katz asked whether these connections could have been pin numbers. Brad confirmed that these are names or strings. X, y positions of nets are supported, but are not shown in slide examples. Pin names may not be the same between board, pin and die models. Circuit and data models are commonly applied and should be supported - an industry standard model connection protocol should be defined. Walter observed that Brad is basically describing a header to a SPICE subcircuit to the outside world. This implies a need for a standard SPICE, which is where EMD can help. Lynne Green asked whether a standard format exists for defining bond pads on-die mapping to on-package attach points. Brad responded negatively - sometimes this is done by name and sometimes by package. Walter responded that only the flip-chip position mapping is reliable.

IBIS INTERCONNECT SPICE SUBCIRCUITS IBIS-ISS

Walter Katz, Signal Integrity Software (SiSoft)

Walter summarized the need for IBIS to standardize a SPICE interconnect format as an industry requirement to have interoperable interconnect modeling sufficient to today's technical needs. This includes signal coupling, power distribution and signal/power coupling. Unfortunately, IBIS today does not support these needs. Walter provided a few simple illustrations of the insufficiency of IBIS interconnect models. Lynne Green asked about S-parameters. Walter responded that S-parameters are not supported under IBIS today and that the specification does not support any means of connecting separate S-parameter data files. The current approach planned by the IBIS-ATM Task Group is to use the proposed EMD format as a container for subcircuits, while a format – IBIS-ISS – based on Synopsys HSPICE* would be used as a standard language for the subcircuits. Elements in this format will be assumed to be LTI, with a sparse Touchstone file being a highly useful addition to support. No main netlist will be defined in the specification - only subcircuits. EMD can point to this format, as can other specifications. Rules for node naming, W-element parameters, etc. will be formalized in the specification.

Bob Ross added that the task group used HSPICE* as a reference by a consensus decision of the EDA community, based on their existing linkage to HSPICE. Arpad Muranyi added that this presentation is meant to introduce this document to the IBIS Open Forum as a proposal from the ATM task group. The next steps are to bring it into a teleconference, perhaps as a BIRD or as a separate document. The goal is to make the proposal available for general review, though document distribution is limited until legal permissions have been finalized. Richard Teliuteuesh noted that the parameters for RLCs are highly complicated and asked whether these are defined in IBIS-ISS. Walter confirmed this. Richard added that the IBIS document defines what is allowed and what is not, but there's no BNF or equivalent for the HSPICE language, as the expression definitions are murky. Walter responded that he had to review six manuals to assemble the pieces into one document, as part of a lengthy process. Lynne Green noted that parameters are non-standard today in multiple tools, and asked whether this was addressed by forcing all to use HSPICE format. Walter answered that parameter ordering is only an issue in R, C, etc. components. As IBIS-ISS is restricted to use with LTI systems, no voltage or temperature dependencies are expected. Arpad commented that this represents a very, very reduced subset of HSPICE. Bob noted that, as soon as IBIS-ISS is approved, it is considered independent from HSPICE as a specification. Richard asked whether an IBISCHK-like parser is envisioned. Arpad Muranyi asked whether the document is ready to be handed off, commenting that work is essentially done in technical areas. Walter commented that anyone can object to any aspect of the specification, but we may not have a lot of discussion about it. One fundamental issue remains, in that IBIS-ISS does not define what a capacitor is, or a w-element,

etc. The presentation closed by Bob clarifying the distinction between a specification and a standard.

AD HOC PRESENTATION: 2003-2009 ACCOMPLISHMENTS

Bob Ross, Teraspeed Consulting Group

Bob summarized the achievements of the last six years of IBIS, showing the changes in specifications and standards managed by the IBIS Open Forum. He noted that considerable effort is spent on the "hidden stuff" to keep the organization moving. Bob observed that, after a period of consolidation, the EDA market is again becoming fragmented, noting that the two top officer positions (Chair and Vice-Chair) come from companies with a combined corporate employee base of 35 to 40 people. He closed his brief summary with a note of thanks to Michael Mirmak for his assistance in making these come to fruition. Michael responded with thanks in kind, and also noted the work needed by the individual task group and subcommittee chairs, plus the efforts of any experts "publicly" known to answer e-mail questions on IBIS.

AD HOC PRESENTATION

Lynne Green, Green Streak Programs

Lynne used the overall approach mentioned by Brad Brim in his presentation to suggest a single standard for linking PCB nets to device package pads and pins, with additional links to die pads. She asked about industry applications. Arpad Muranyi asked about multiple instances of devices on the PCB. Walter Katz added that multiple dice can be placed in a single package. Michael Mirmak asked why EBD did not handle these cases. Walter noted that the EMD proposal would address all these cases.

Michael asked whether a standard for physical structures, in the sense of a field solver input specification, was called for. Lynne suggested that package designers would resist this, due to a need to protect proprietary information. Walter suggested that the need for package standardization is similar to the evolution of [Receiver Thresholds]. The keyword was not adopted rapidly enough, leaving EDA vendors to develop proprietary solutions. Now, any standard derating cannot be adopted without EDA resistance.

OPEN DISCUSSION AND CONCLUDING ITEMS

During the open discussion period, Arpad Muranyi asked about Bob Ross' Touchstone presentation, in particular about the need for a translation Perl script. Bob confirmed that this would be useful, for conversion of Touchstone 1.0 files to 2.0 format. Walter noted that this was relatively trivial, but that converting 2.0 to 1.0 would be highly difficult. Vishram Pandit asked about why normalization was removed from the specification, particularly as Y- and Z-parameters are not affected. Brad Brim noted that normalization was implemented in the 1980s to save computation and file-writing time. The original specification mentioned it, but few observed it. As this is a problem for cross-compatibility, it was removed in 2.0. Bob Ross and Michael Mirmak also contributed a few background comments on the normalization rules written in Touchstone 2.0.

Michael Mirmak closed the meeting by thanking the participants, presenters and co-sponsors and reminding those present of the dates for the next summit and teleconference meetings. The meeting was adjourned at approximately 3:50 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held August 7, 2009 from 8:00 AM to 10:00 AM US Pacific Time.

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NOTES

IBIS CHAIR: Bob Ross (503) 246-8048, Fax: (503) 239-4400
bob@teraspeed.com
Staff Scientist, Teraspeed Consulting Group
10238 SW Lancaster Road
Portland, OR 97219

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President / CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
anders.ekholm@ericsson.com
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network
Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Syed Huq (408) 525-3399, Fax: (408) 526-5504
shuq@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive
San Jose, CA 95134-1706

POSTMASTER: Mike LaBonte
milabont@cisco.com

This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda-stds.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda-stds.org)
IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

* Other trademarks, brands and names are the property of their respective owners.

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	June 5, 2009	June 26, 2009	July 17, 2009	July 28, 2009
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Inactive				
Agilent Technologies	User	Inactive				√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Inactive	√			
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Inactive	√			√
Green Streak Programs	General Interest	Inactive		√		√
Hitachi ULSI Systems	Producer	Inactive				
IBM	Producer	Inactive		√		
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Active	√	√	√	√
IO Methodology	User	Active			√	√
LSI	Producer	Active	√	√	√	
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Inactive	√	√		
Nokia Siemens Networks	Producer	Active	√	√	√	
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active	√	√	√	√
Sigrity	User	Inactive				√
Synopsys	User	Inactive				
Teraspeed Consulting	General Interest	Active	√	√	√	√
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive				
ZTE	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.