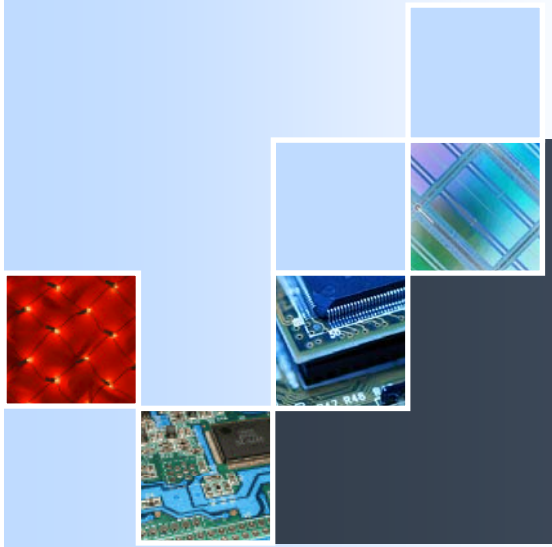

Model Connection Protocols for Chip-Package-Board

IBIS Summit
Design Automation Conference
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SIGRITY

Agenda

- Discuss concepts related to electrical model connectivity for chip/package/board system-level analysis
- Review existing solutions
  - no standards exist
  - some existing solution specifications are under NDA
- Observations

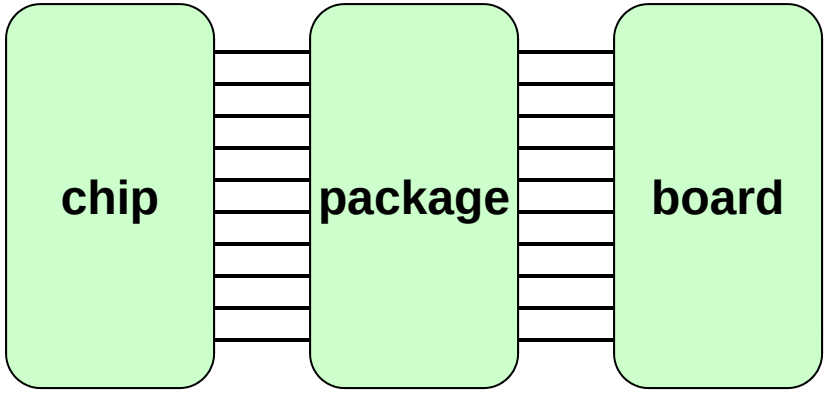
NOTE:

- The Sigrity model connection protocol discussed in this presentation is not being proposed as a standard, merely as an example of an existing solution created in reaction to short term need and lack of existing standard protocols.

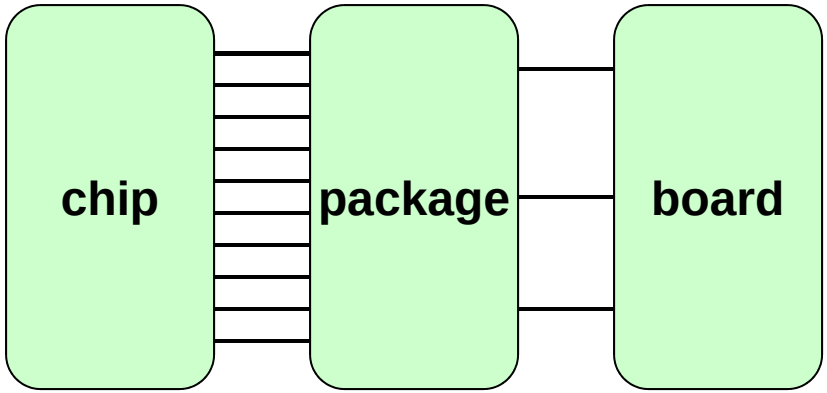
Requirements

- Chip/package/board systems have many physical connections (pins)
  - chip-package boundary ≈ 100 – 5000
  - package-board boundary ≈ 100 – 2000
- Not all electrical models can have pin-level resolution
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools
- Adequate modeling may not be possible with net-level resolution
  - especially, if throughout entire system
- Support is required for
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools

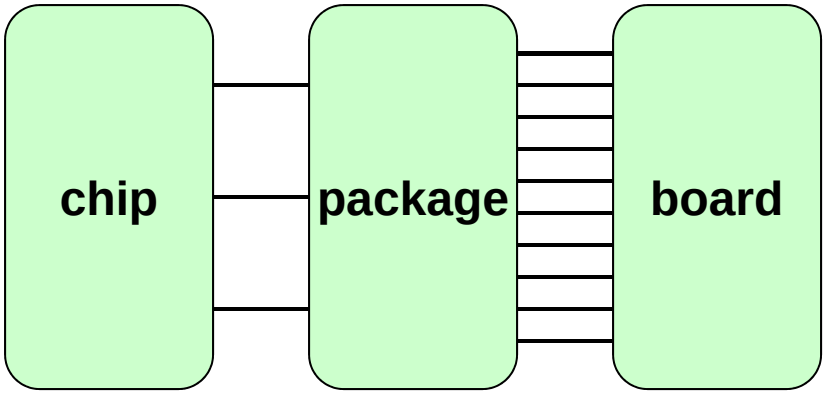
System Analysis



Physical connectivity



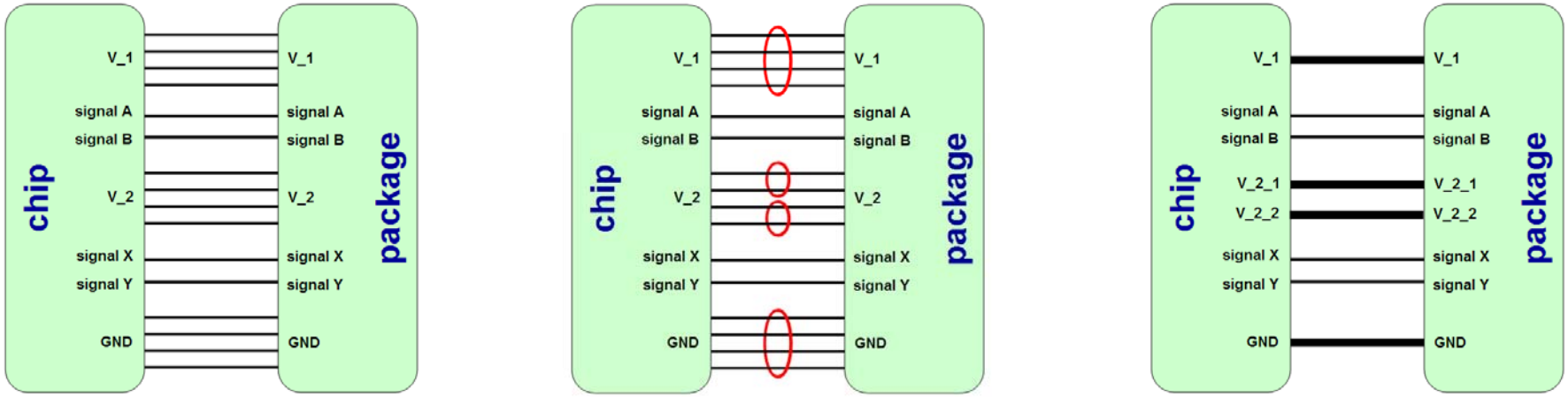
Chip-centric model abstraction



Board-centric model abstraction

System Analysis

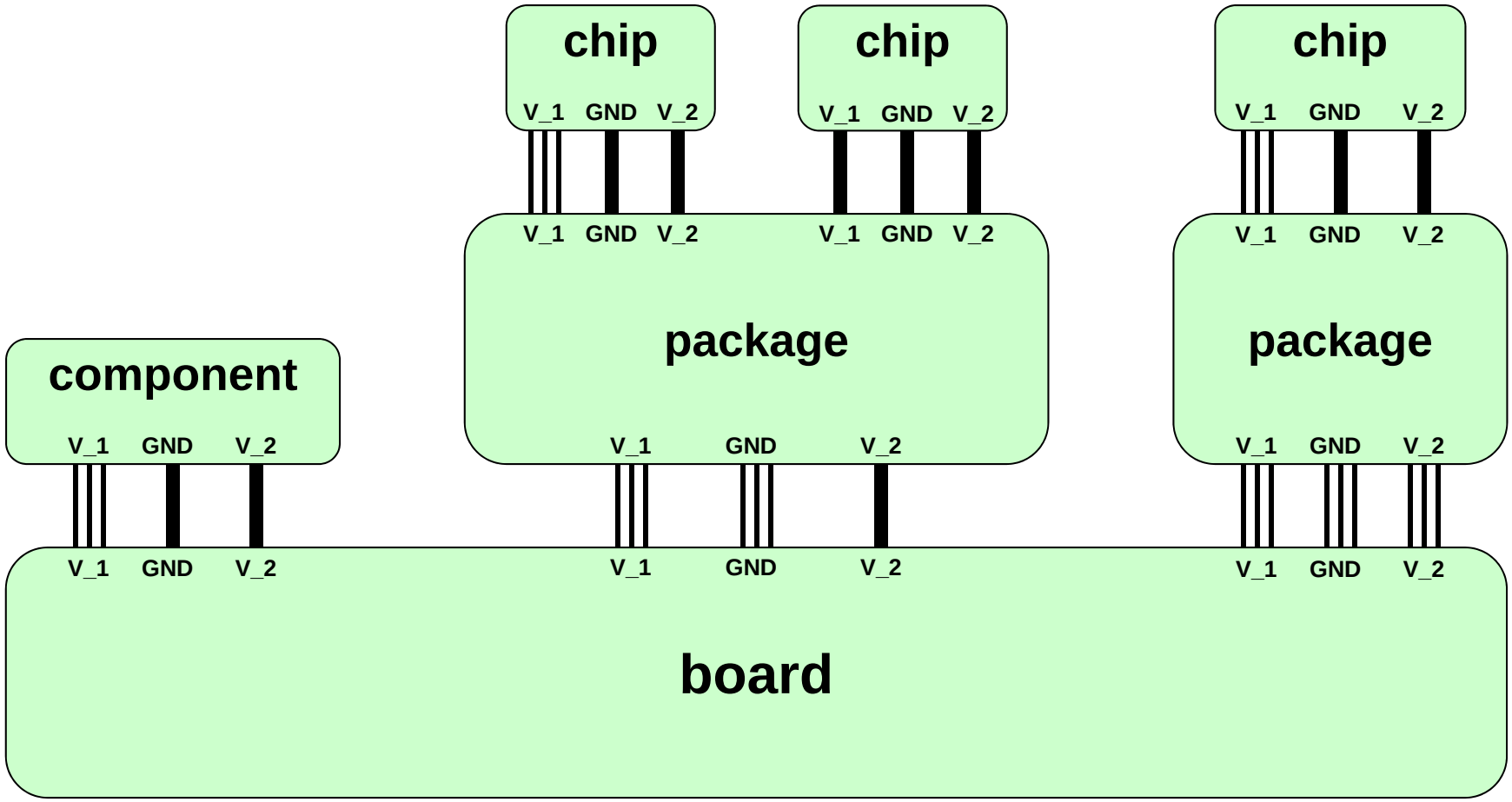
- A bit more detailed view of electrical model resolution through pin grouping, for one domain boundary



decreasing model resolution

System Analysis

- a more general system



Existing Model Connection Protocols for Chip/Package/Board Analysis

- Sigrity MCP (**M**odel **C**onnection **P**rotocol)
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board systems
  - presently Version 1.0
    - 1.1 available soon with user-requested pin locations
- Apache CPP
  - defined by Apache
    - definition covered under NDA

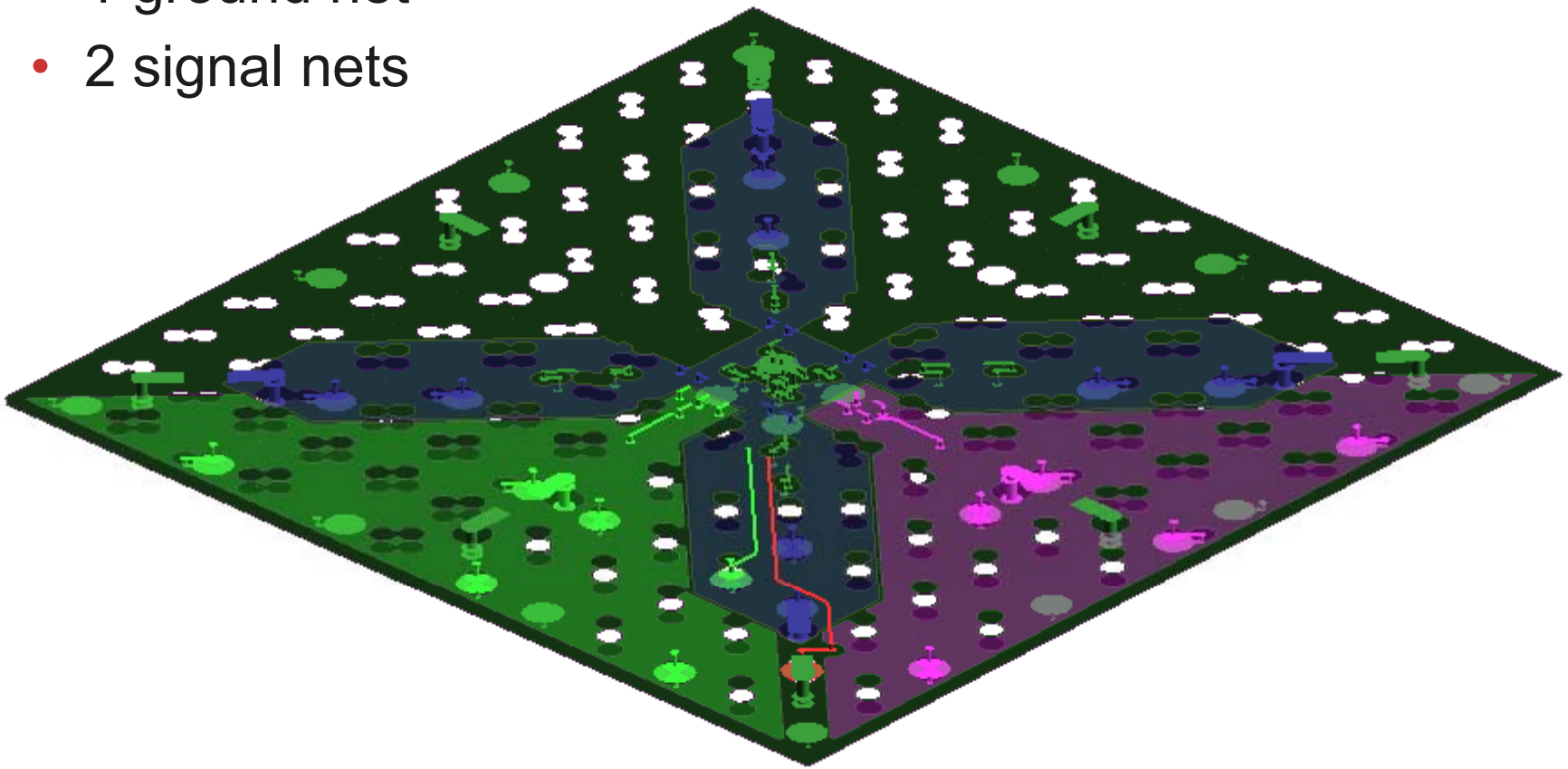
- Implemented as “headers”
- Contained within model-native comment lines

A Typical Model Connection Protocol
(Sigrity MCP)

* [MCP Begin]
* [MCP Ver] *1.1*
* [Structure Type] *PKG*
* [MCP Source] *source text*
* [Coordinate Unit] *unit*
* [Connection] *connectionName partName numberPhysicalPins*
* [Connection Type] *DIE*
* [Power Nets]
* *pinName* model*NodeName netName x y*
* …
* *pinName modelNodeName netName x y*
* [Ground Nets]
* *pinName modelNodeName netName x y*
* …
* *pinName modelNodeName netName x y*
* [Signal Nets]
* *pinName modelNodeName netName x y*
* …
* *pinName modelNodeName netName x y*
* [MCP End]

A Physical Example

- small flipchip BGA
  - 3 power nets
  - 1 ground net
  - 2 signal nets



A SPICE circuit with MCP header

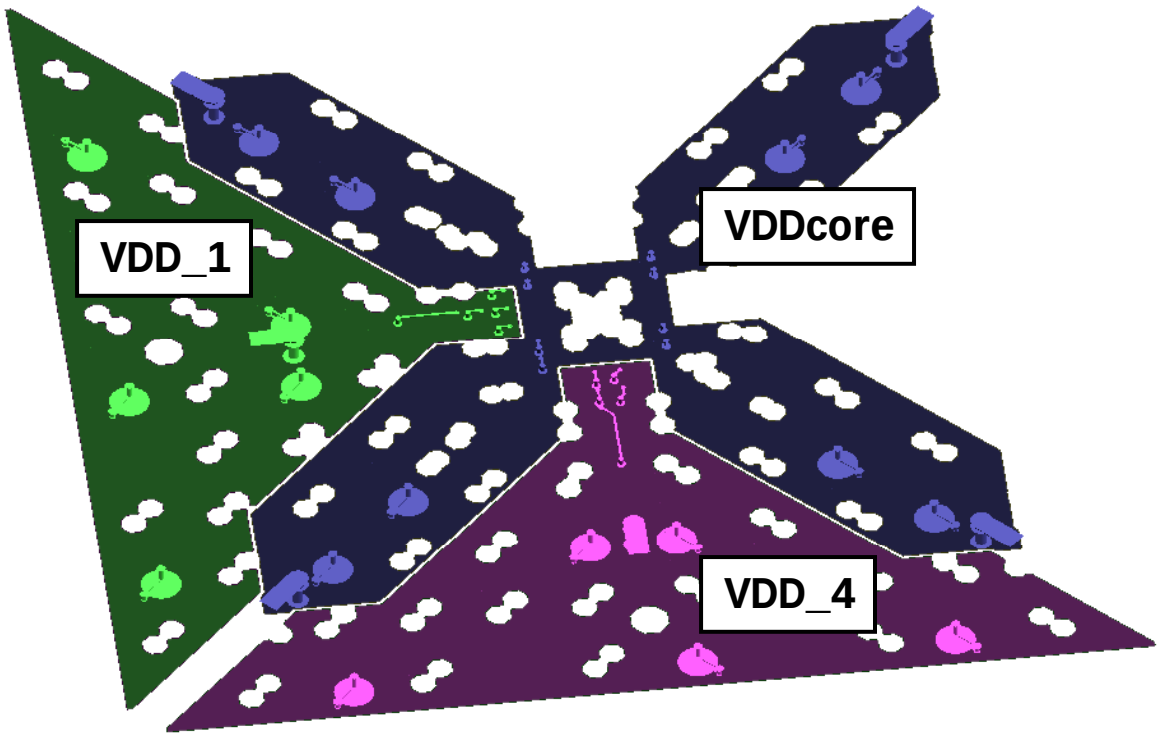
(*a pin-base model*)

```
.SUBCKT FlipChip_pkg_SPICE_T
+            U1_U1-E3       BGA1_BGA1-C1
+            U1_U1-K6       BGA1_BGA1-K6
+            U1_U1-D4       BGA1_BGA1-C10
+            U1_U1-L1       BGA1_BGA1-L2
+            U1_U1-K1       BGA1_BGA1-J3
+            Node__GND
*
*The following is the Sigrity MCP (model connection protocol) Section
**********************************
*[MCP Begin]
*[MCP Ver] 1.0
*[MCP Source] Sigrity XtractIM 3.0.2.07061  7/18/2009
*
```

A SPICE circuit with MCP header

(*a pin-base model*)

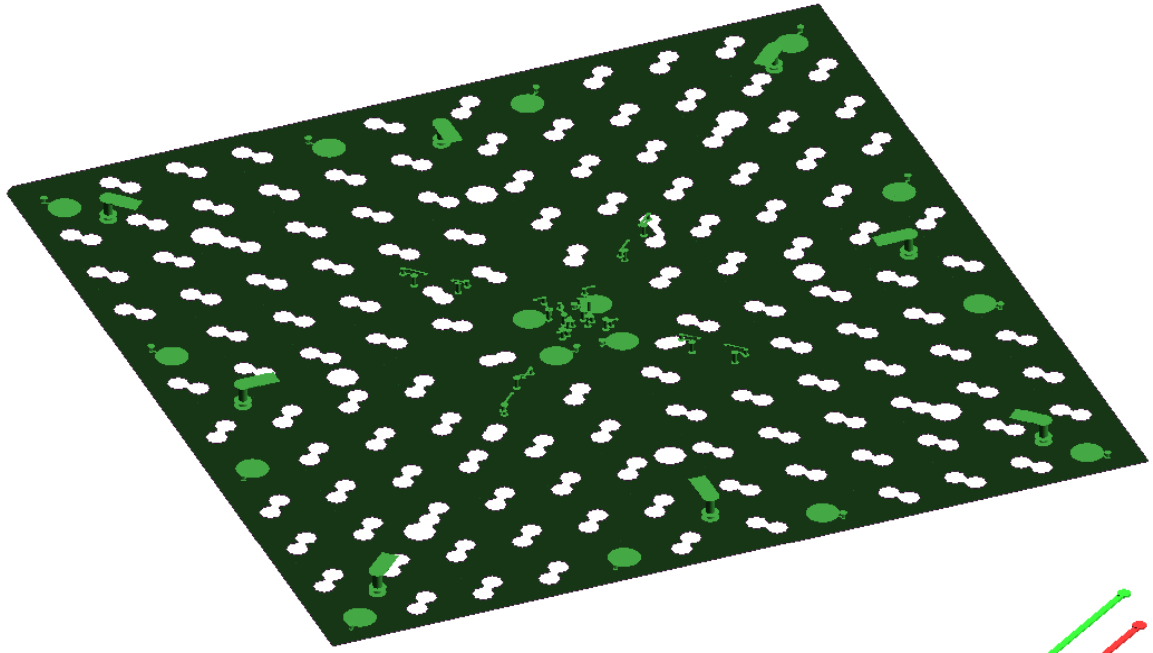
```
*[Connection] U1 flipchip 144
*[Connection Type] DIE
*[Power Nets]
* U1-E3   U1_U1-E3 VDD_1
* U1-F1   U1_U1-E3 VDD_1
* U1-F2   U1_U1-E3 VDD_1
* U1-F3   U1_U1-E3 VDD_1
* U1-G3   U1_U1-E3 VDD_1
* U1-K6   U1_U1-K6 VDD_4
* U1-K7   U1_U1-K6 VDD_4
* U1-L6   U1_U1-K6 VDD_4
* U1-L7   U1_U1-K6 VDD_4
* U1-M6   U1_U1-K6 VDD_4
* U1-D4   U1_U1-D4 VDDcore
* U1-D9   U1_U1-D4 VDDcore
* U1-E4   U1_U1-D4 VDDcore
* U1-E9   U1_U1-D4 VDDcore
* U1-H4   U1_U1-D4 VDDcore
* U1-H9   U1_U1-D4 VDDcore
* U1-J4   U1_U1-D4 VDDcore
* U1-J9   U1_U1-D4 VDDcore
```

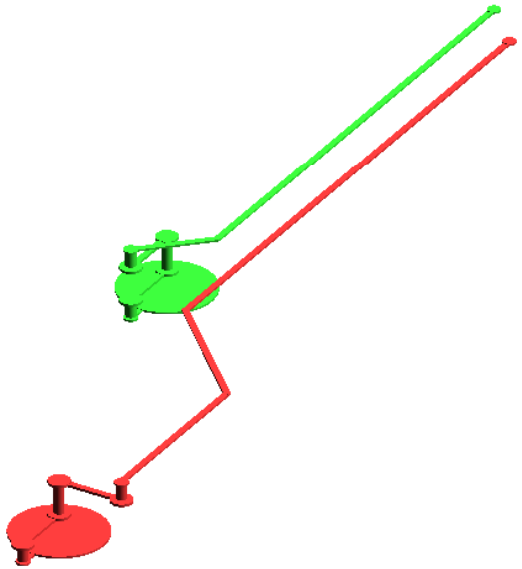


A SPICE circuit with MCP header

(*a pin-base model*)

```
*[Ground Nets]
* U1-A1    Node__GND  VSS
* U1-A12    Node__GND  VSS
* U1-B11    Node__GND  VSS
* U1-B2    Node__GND  VSS
* U1-E5    Node__GND  VSS
* U1-E8    Node__GND  VSS
* U1-F6    Node__GND  VSS
* U1-F7    Node__GND  VSS
* U1-G6    Node__GND  VSS
* U1-G7    Node__GND  VSS
* U1-H5    Node__GND  VSS
* U1-H8    Node__GND  VSS
* U1-L11    Node__GND  VSS
* U1-L2    Node__GND  VSS
* U1-M1    Node__GND  VSS
* U1-M12    Node__GND  VSS
*
*[Signal Nets]
* U1-L1    U1_U1-L1  Net_1
* U1-K1    U1_U1-K1  Net_2
```

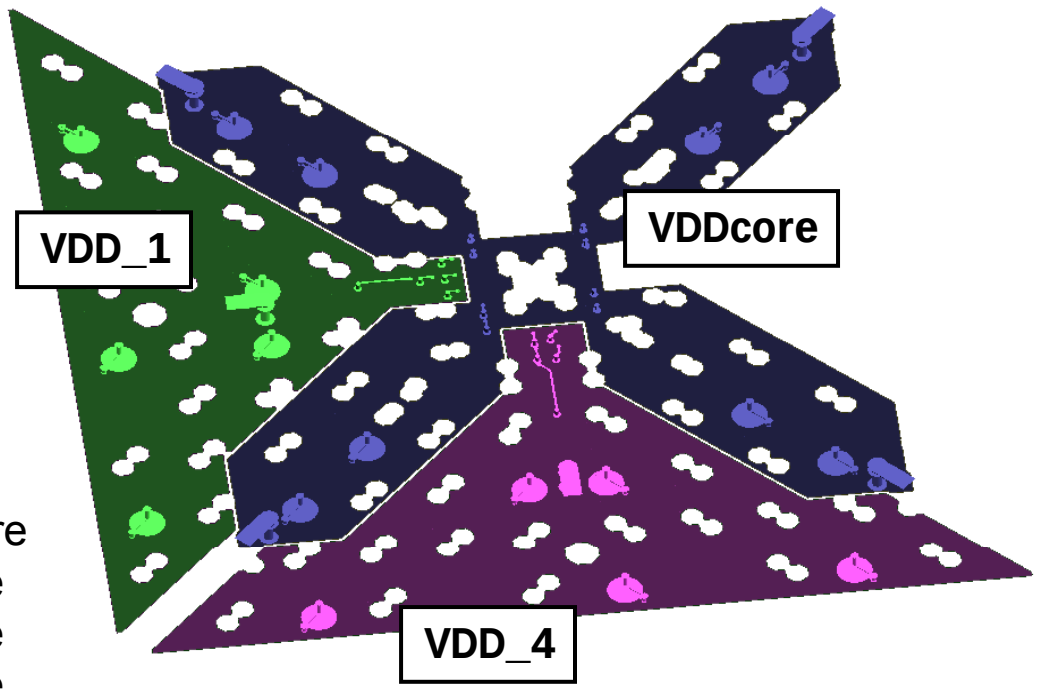




A SPICE circuit with MCP header

(*a pin-base model*)

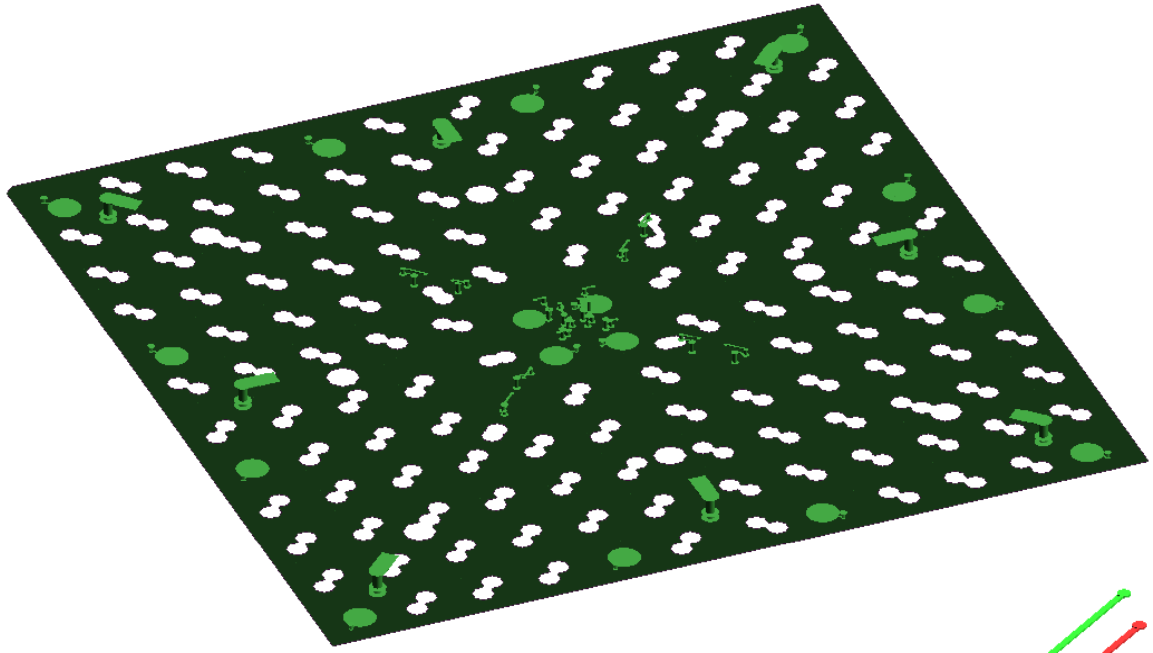
```
*[Connection] BGA1 board 144
*[Connection Type] PCB
*[Power Nets]
* BGA1-C1    BGA1_BGA1-C1  VDD_1
* BGA1-F3    BGA1_BGA1-C1  VDD_1
* BGA1-G1    BGA1_BGA1-C1  VDD_1
* BGA1-G3    BGA1_BGA1-C1  VDD_1
* BGA1-K1    BGA1_BGA1-C1  VDD_1
* BGA1-K6    BGA1_BGA1-K6  VDD_4
* BGA1-K7    BGA1_BGA1-K6  VDD_4
* BGA1-M10    BGA1_BGA1-K6  VDD_4
* BGA1-M3    BGA1_BGA1-K6  VDD_4
* BGA1-M7    BGA1_BGA1-K6  VDD_4
* BGA1-C10    BGA1_BGA1-C10  VDDcore
* BGA1-C3    BGA1_BGA1-C10  VDDcore
* BGA1-D4    BGA1_BGA1-C10  VDDcore
* BGA1-D9    BGA1_BGA1-C10  VDDcore
* BGA1-J4    BGA1_BGA1-C10  VDDcore
* BGA1-J9    BGA1_BGA1-C10  VDDcore
* BGA1-K10    BGA1_BGA1-C10  VDDcore
* BGA1-K3    BGA1_BGA1-C10  VDDcore
```

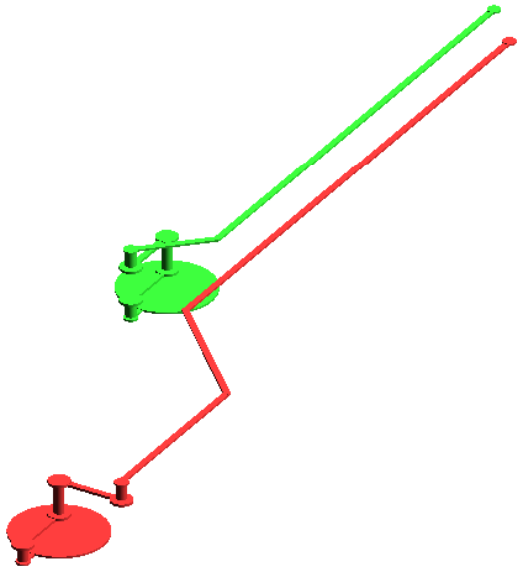


A SPICE circuit with MCP header

(*a pin-base model*)

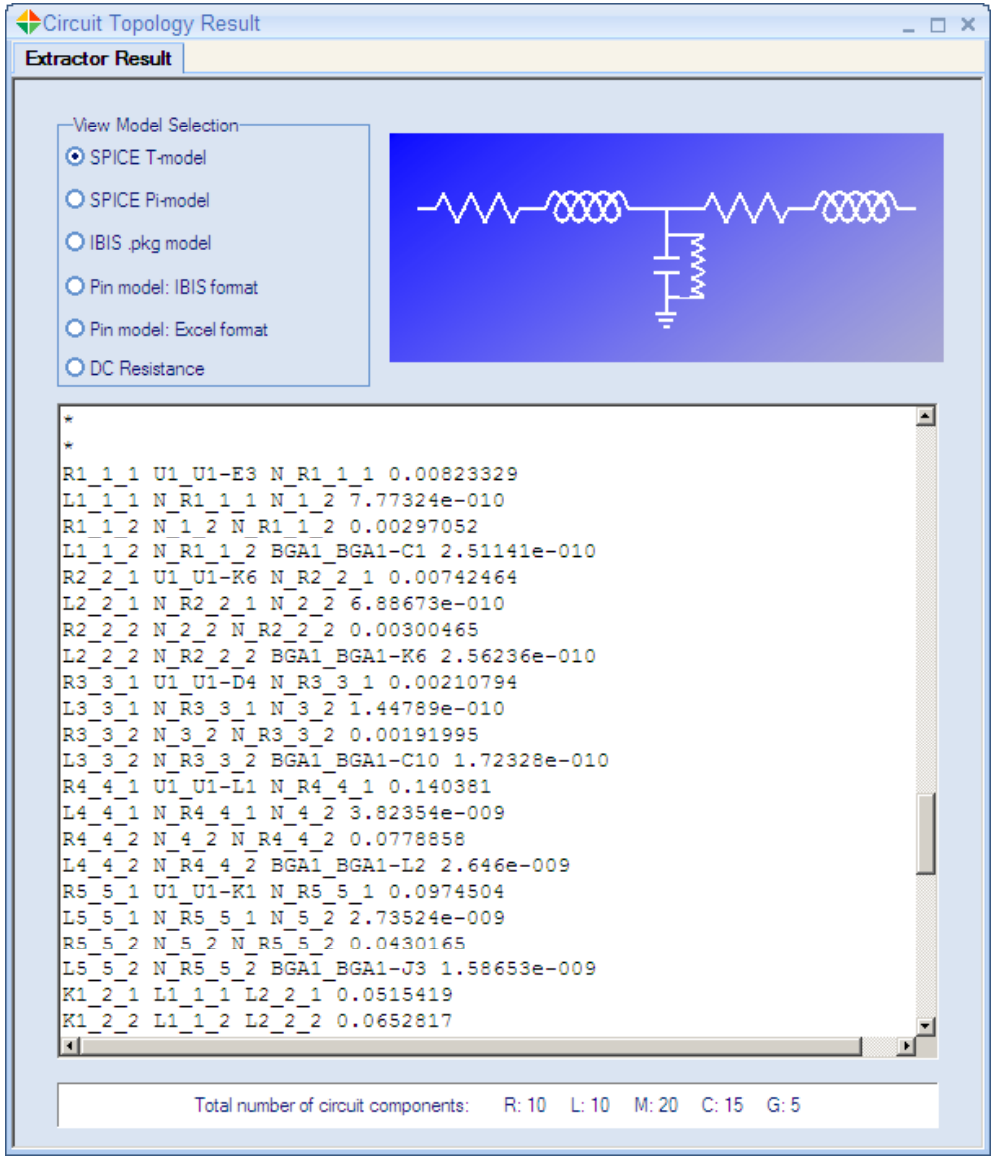
```
*[Ground Nets]
* BGA1-A1    Node__GND  VSS
* BGA1-A12    Node__GND  VSS
* BGA1-A5    Node__GND  VSS
* BGA1-A8    Node__GND  VSS
* BGA1-E1    Node__GND  VSS
* BGA1-E12    Node__GND  VSS
* BGA1-F6    Node__GND  VSS
* BGA1-F7    Node__GND  VSS
* BGA1-G6    Node__GND  VSS
* BGA1-G7    Node__GND  VSS
* BGA1-H1    Node__GND  VSS
* BGA1-H12    Node__GND  VSS
* BGA1-M1    Node__GND  VSS
* BGA1-M12    Node__GND  VSS
* BGA1-M5    Node__GND  VSS
* BGA1-M8    Node__GND  VSS
*
*[Signal Nets]
* BGA1-L2    BGA1_BGA1-L2  Net_1
* BGA1-J3    BGA1_BGA1-J3  Net_2
*
*[MCP End]
```





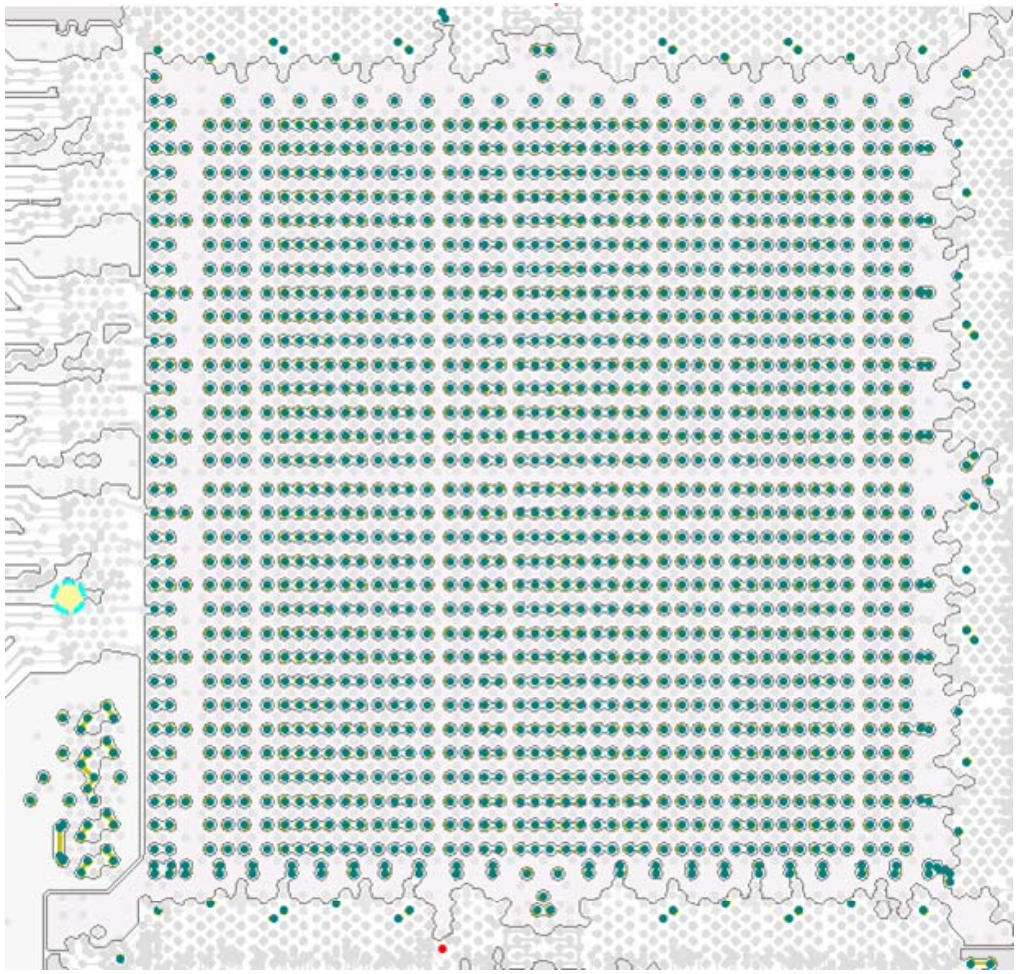
A SPICE circuit with MCP header

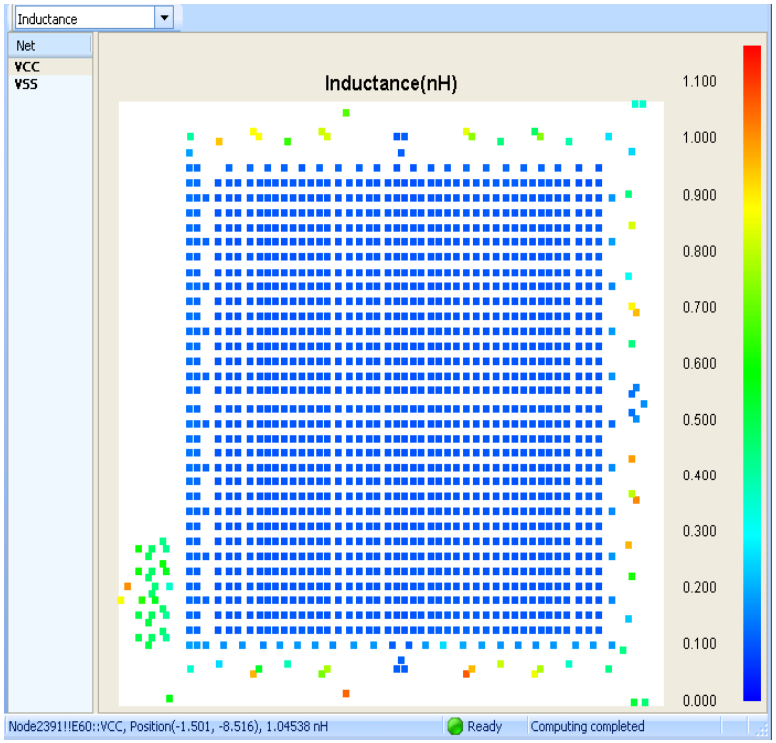
(*a pin-base model*)

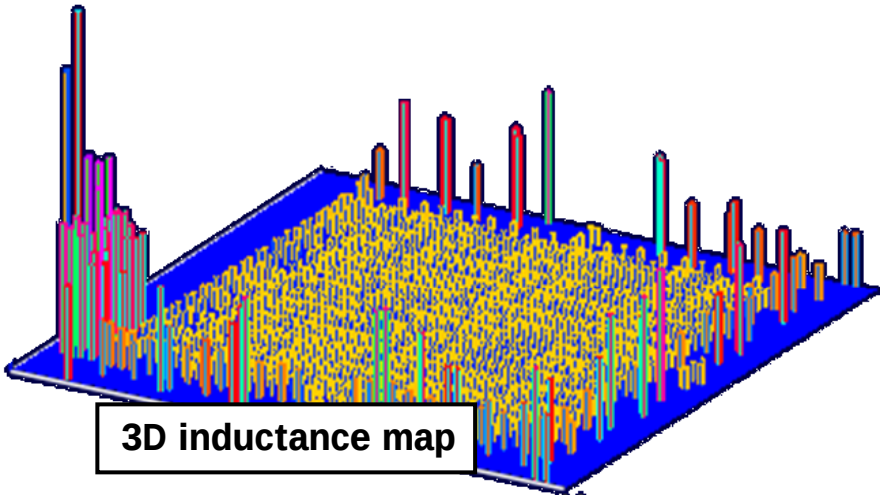


A Typical Package Pin Map

(*one power net*)







3D inductance map

Observations

- Chip/package/board designs have thousands of pins
- Chip/package/board system analysis requires
  - user-definable model resolution
  - automated connection support
- Circuit and data models are commonly applied
  - both should be supported by any connection protocol
- Model connection protocols are much more than simply “port names”
- Proprietary model connection protocols are currently being applied
- An industry standard model connection protocol should be defined
  - user and EDA vendor participation will be required to agree on a standard
  - active participation by more than a few individuals will be required

Thank You!