Case Study: Analyze different results from IBIS simulators

Lance Wang
lwang@iometh.com
DAC 2009 IBIS Summit
San Francisco, CA
July 28th, 2009

Motivations

- Found some unexpected results when validating an IBIS output model
- Then, used 4 commercial spice/ibis simulators, trying to see how others predict
- Sharing the experience ……

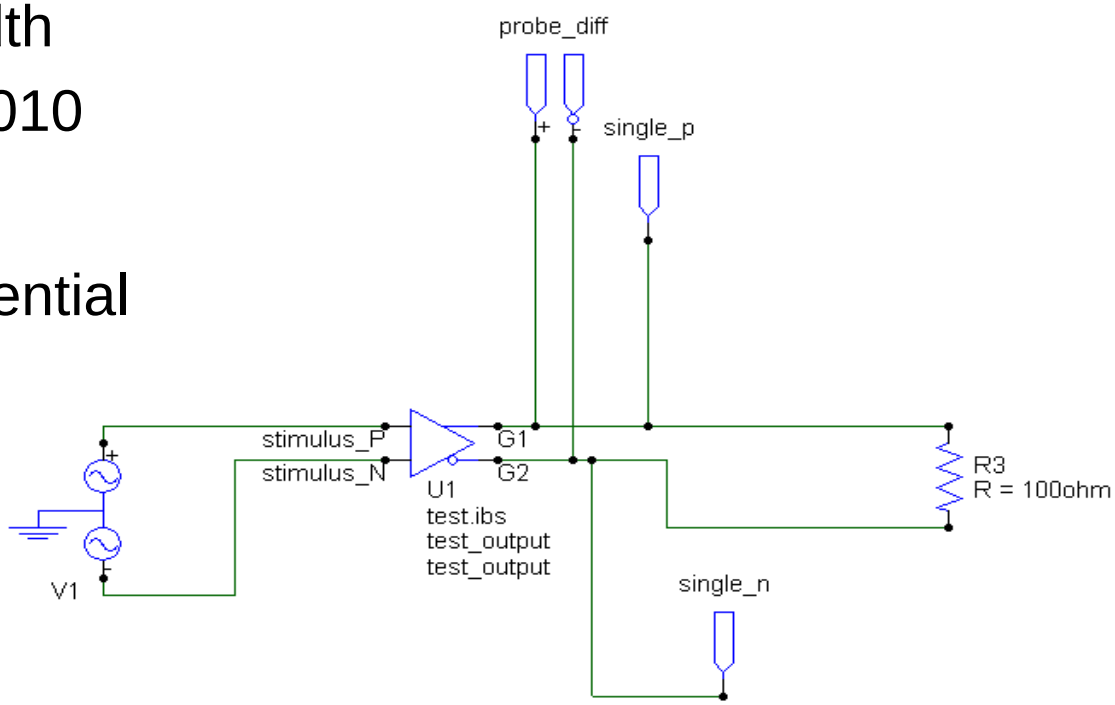
IBIS model

- An Output model
  - 1.2 v VCC (typical corner)
  - Output type model with pullup and pulldown curves only
  - Differential Pin defined
  - One set of VT curves
  - Passed IBISCHK with 0 error, 0 warning

```
|
[Package]
| variable        typ                min                max
R_pkg             0m                 0m                 0m
L_pkg             0n                 0n                 0n
C_pkg             0p                 0p                 0p
|
|------------------------PIN-------------------------------------------------
[Pin]  signal_name          model_name          R_pin     L_pin     C_pin
G1     TXP            test_output
G2     TXN            test_output
|
|----------------------DIFF PIN-----------------------------------------
[Diff_pin]     inv_pin     vdiff      tdelay_typ   tdelay_min   tdelay_max
  G1           G2          NA         NA           NA           NA
|
|-----------------------------------------------------------------------
[Model]      test_output
Model_type     Output
Polarity       Inverting
Enable         Active-High
|
Vmeas = 0.65
|
|                             typ               min               max
|
C_comp                      1.2p  1.1p  1.3p
[Voltage Range]             1.1   0.938  1.2
[Temperature Range]         50  113   -3
|
|*************************************************************************
|
[Pullup]
```

The first test

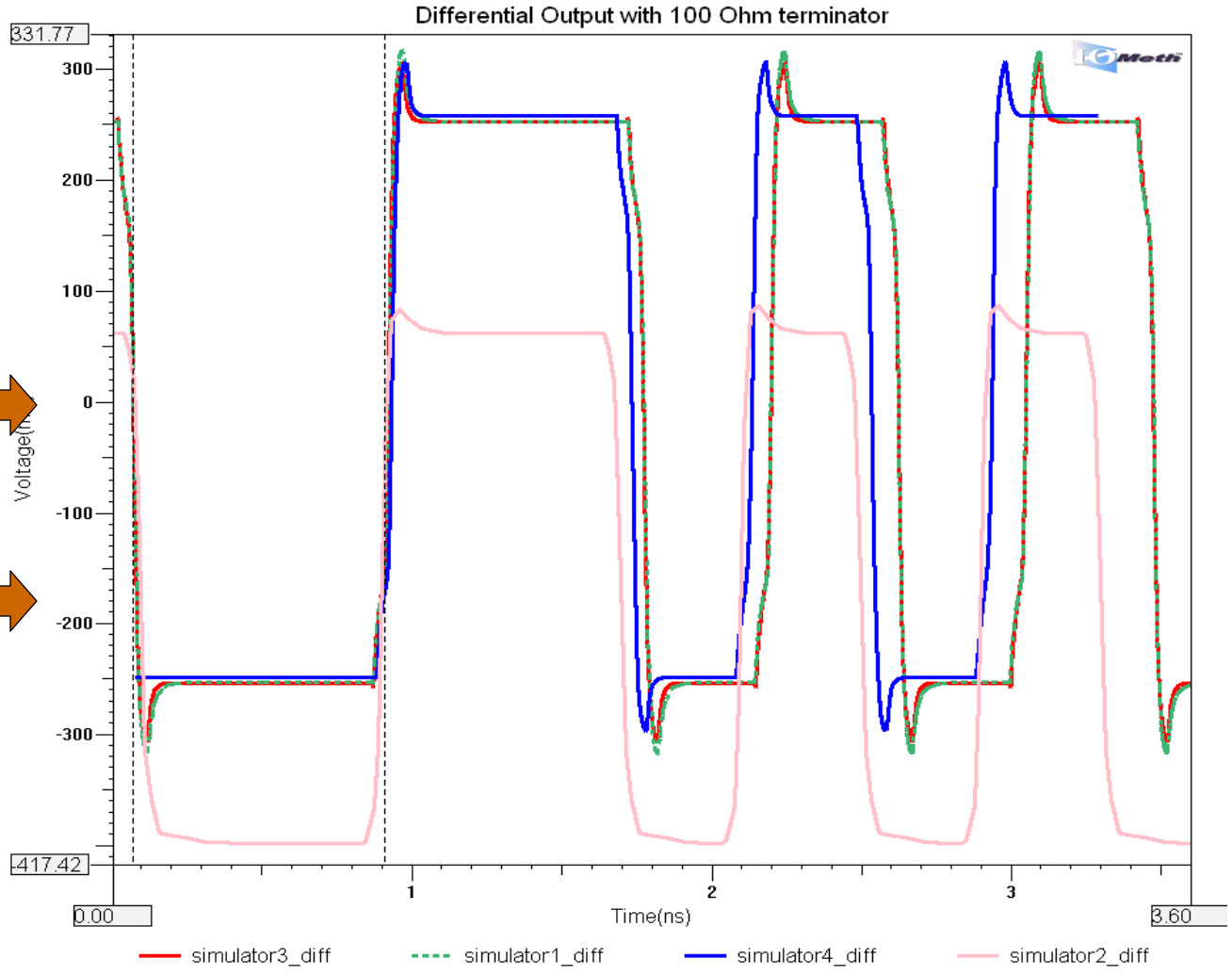
- Stimulus
  - 22ps rising/falling edges
  - 0.4ns pulse width
  - Pattern: 11001010
- Test Load
  - 100 Ohm differential termination



Differential outputs

~ 0mv

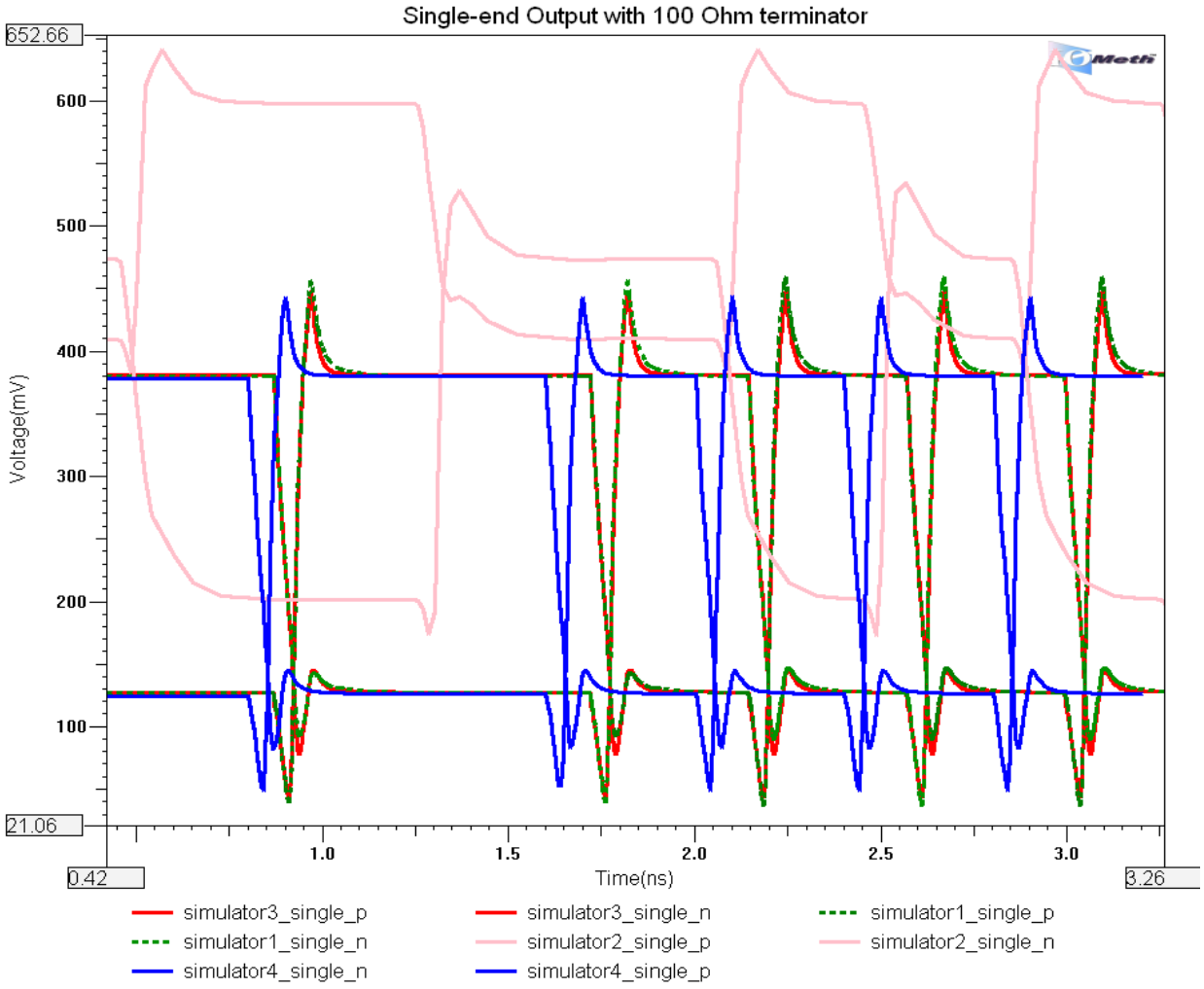
~ -180mv



Single-end outputs

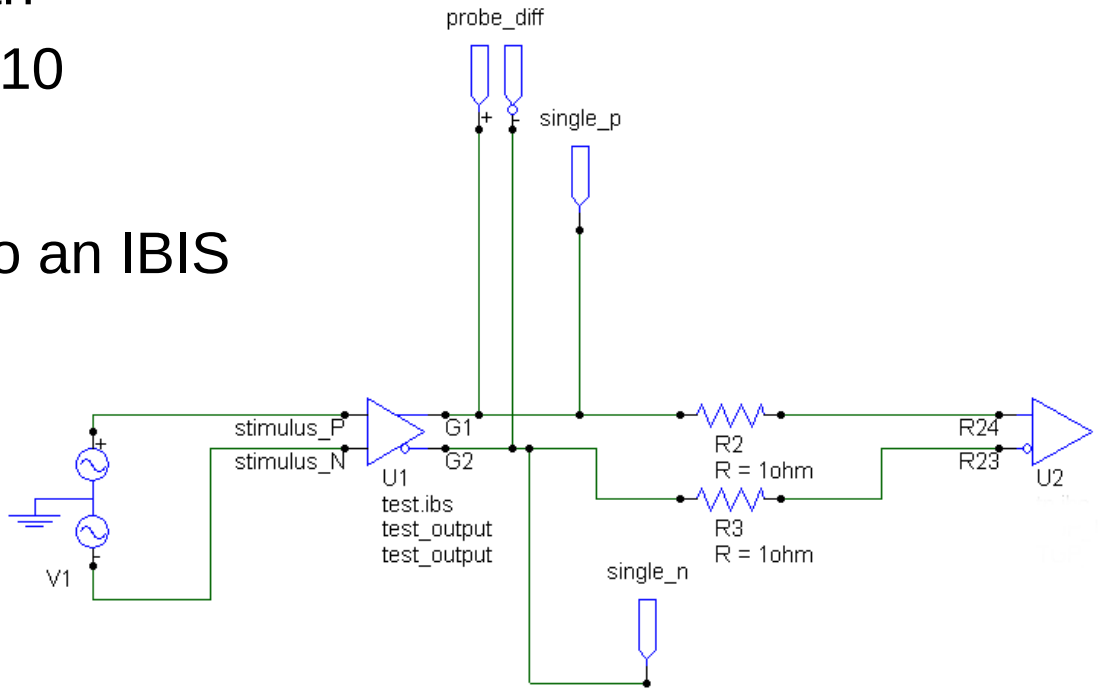
~ 440mv

~ 250mv



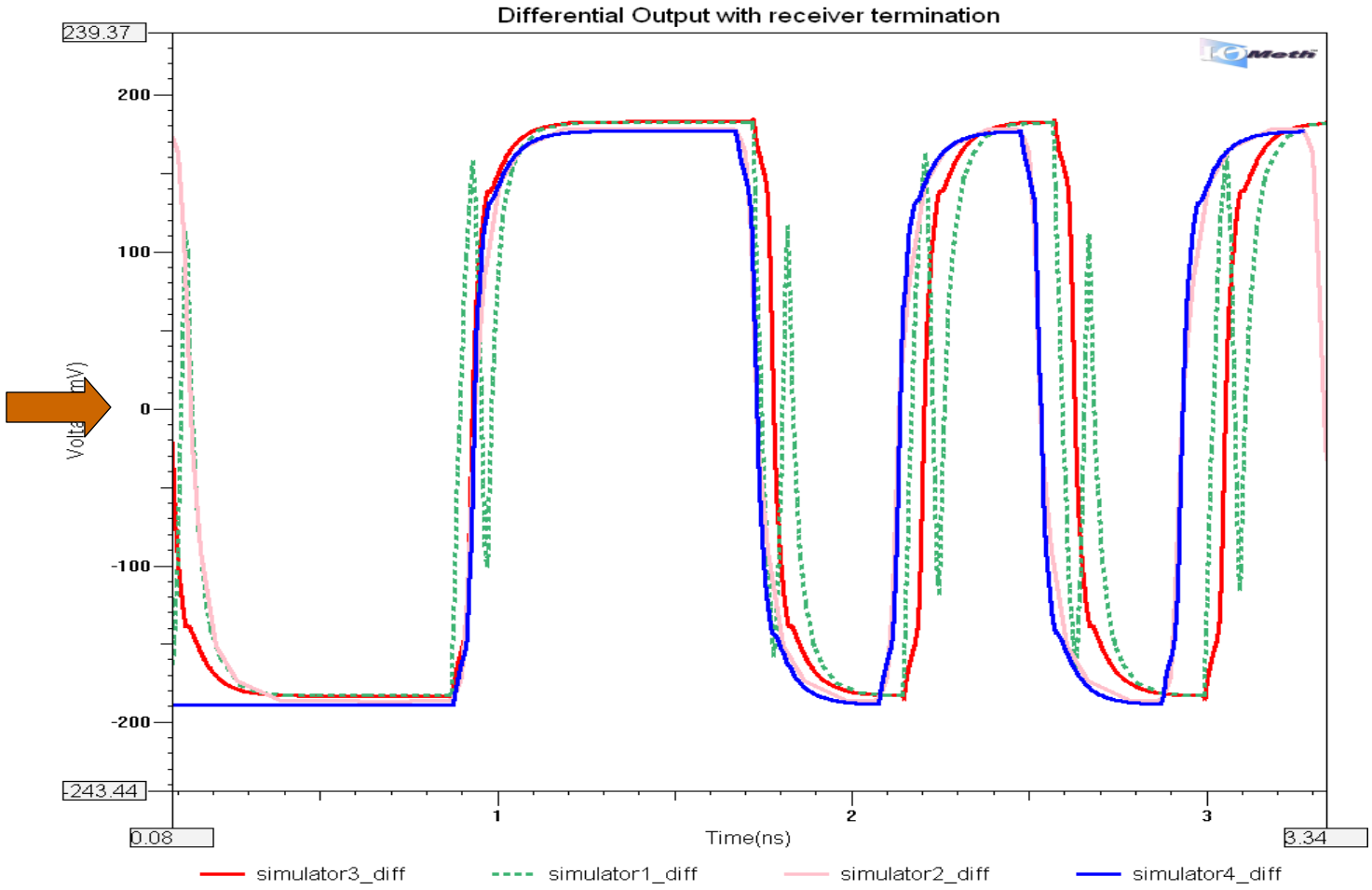
The second test

- Stimulus
  - 22ps rising/falling edges
  - 0.4ns pulse width
  - Pattern: 11001010
- Test Load
  - Direct connect to an IBIS receiver (Input)



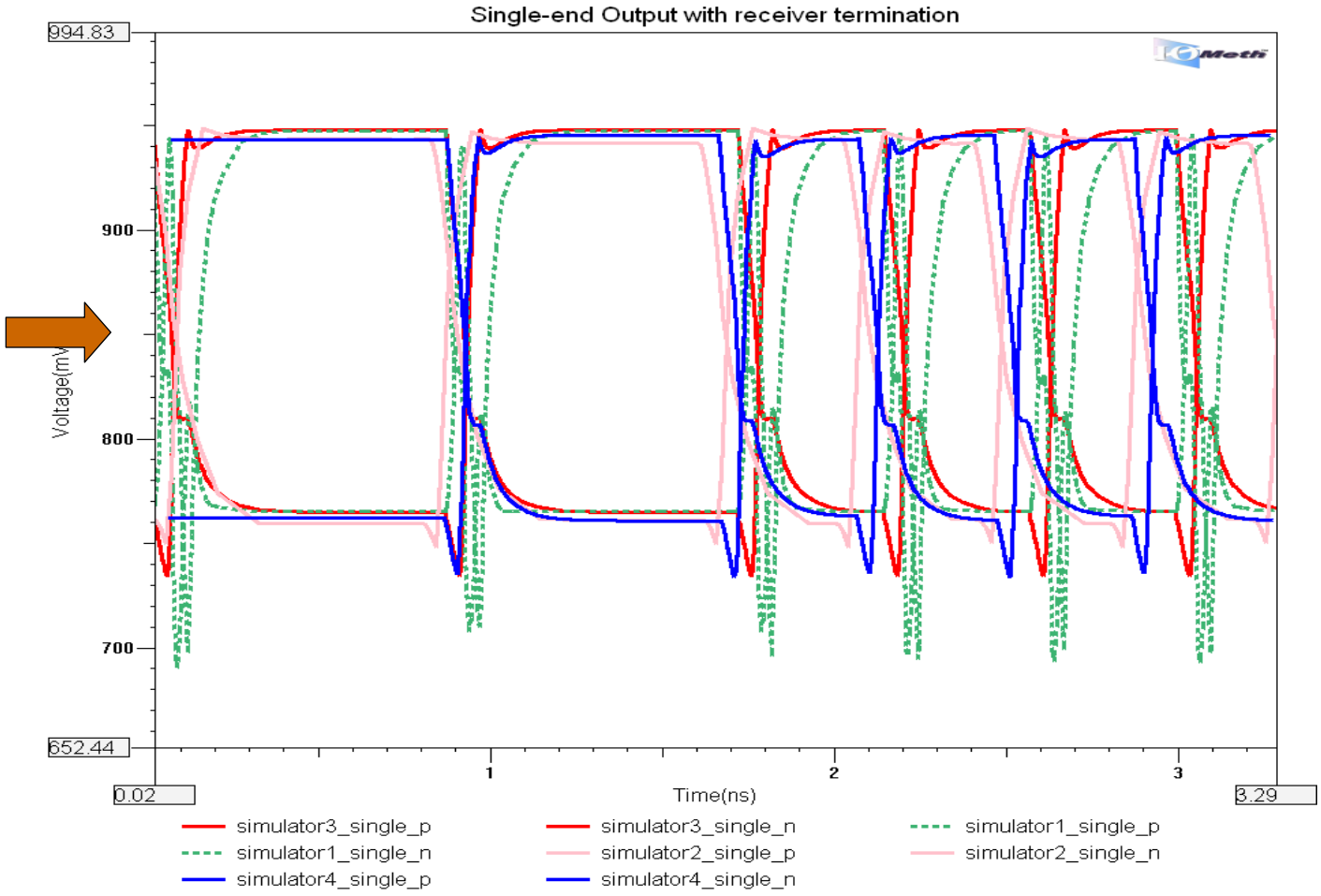
Differential outputs

~ 0mv



Single-end outputs

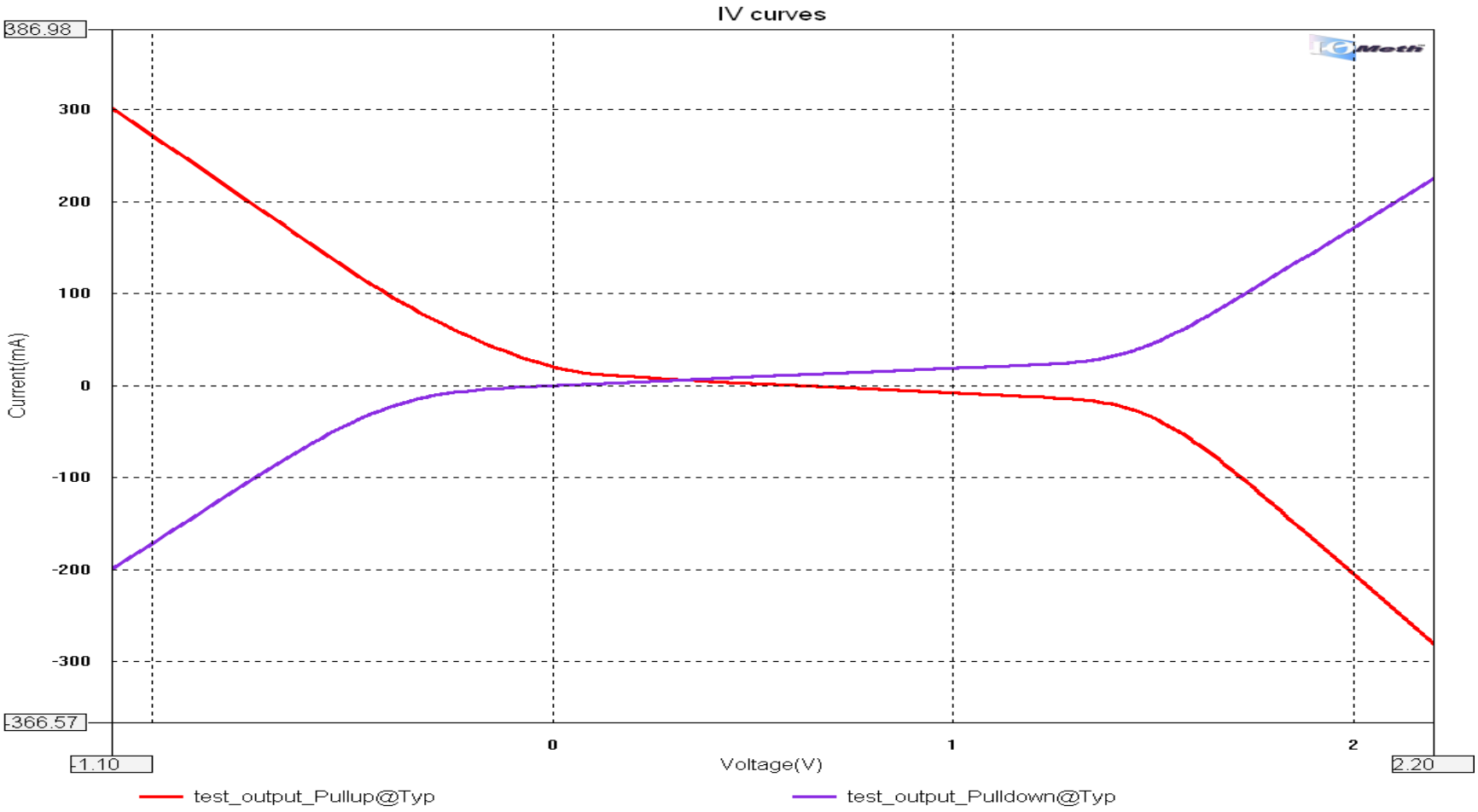
~ 850mv



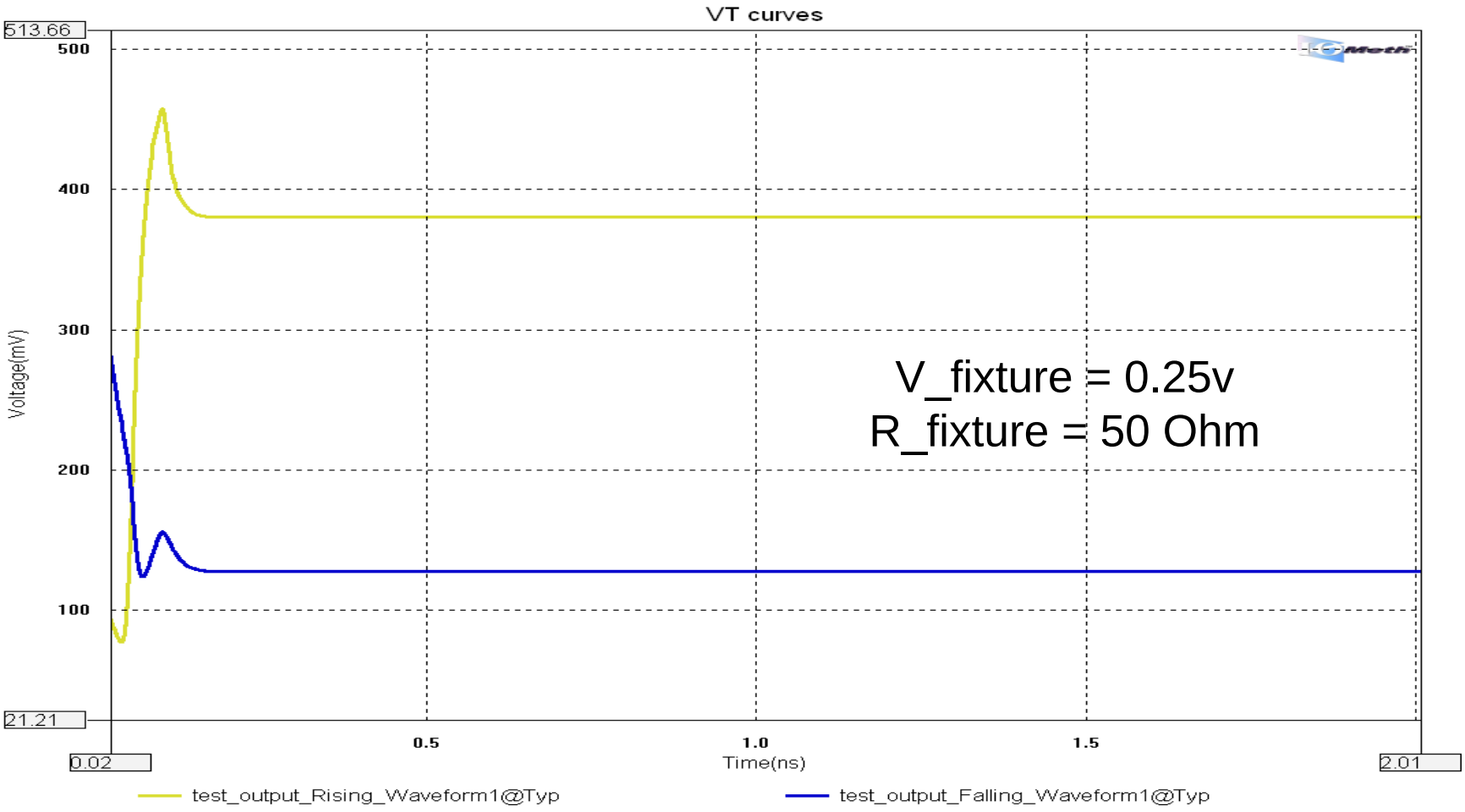
Try to analyze ……

- Check IBIS files
  - Driver and receiver
  - IV curves and VT curves
- Check with simulation results
- Some conclusions?

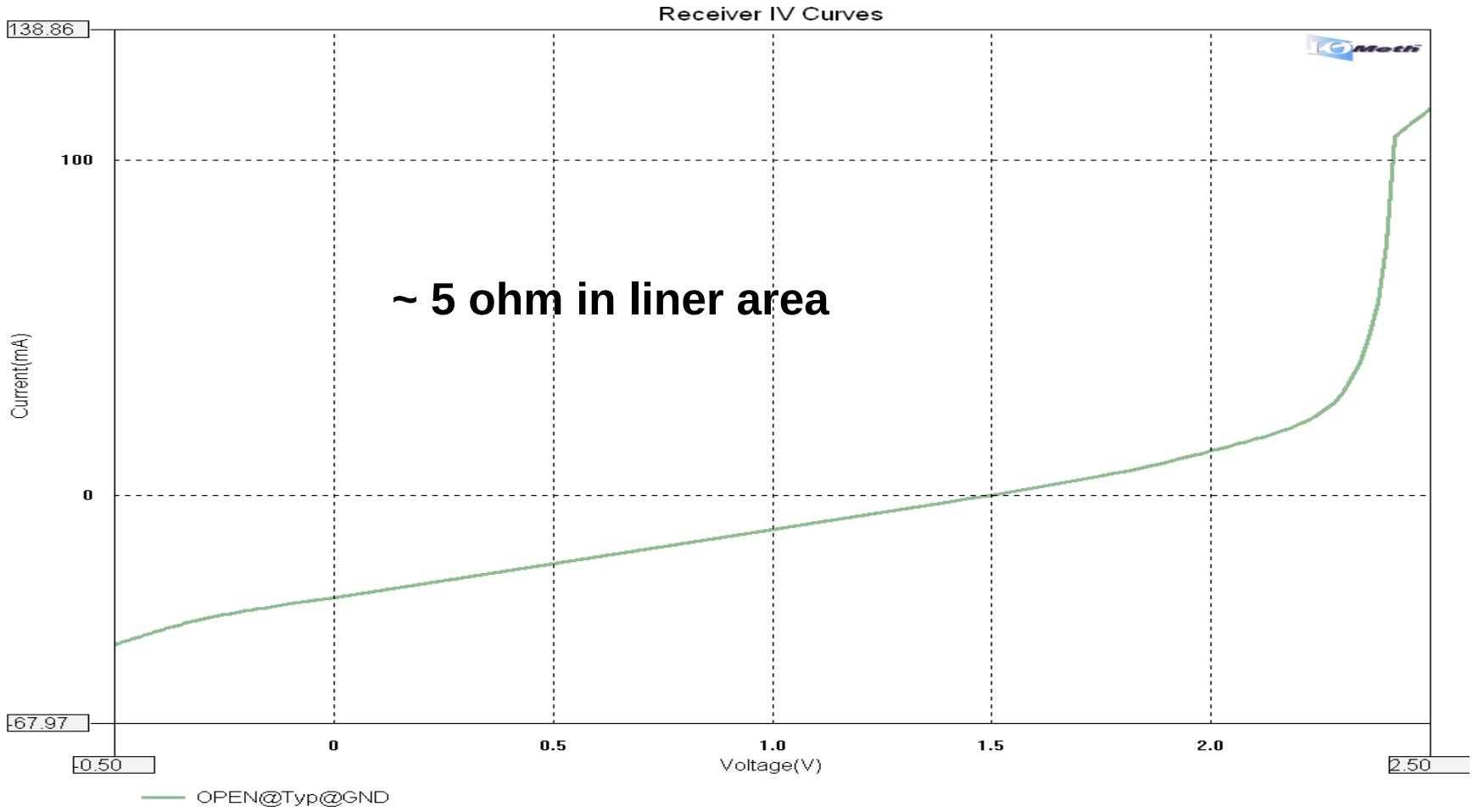
Driver IBIS IV curves



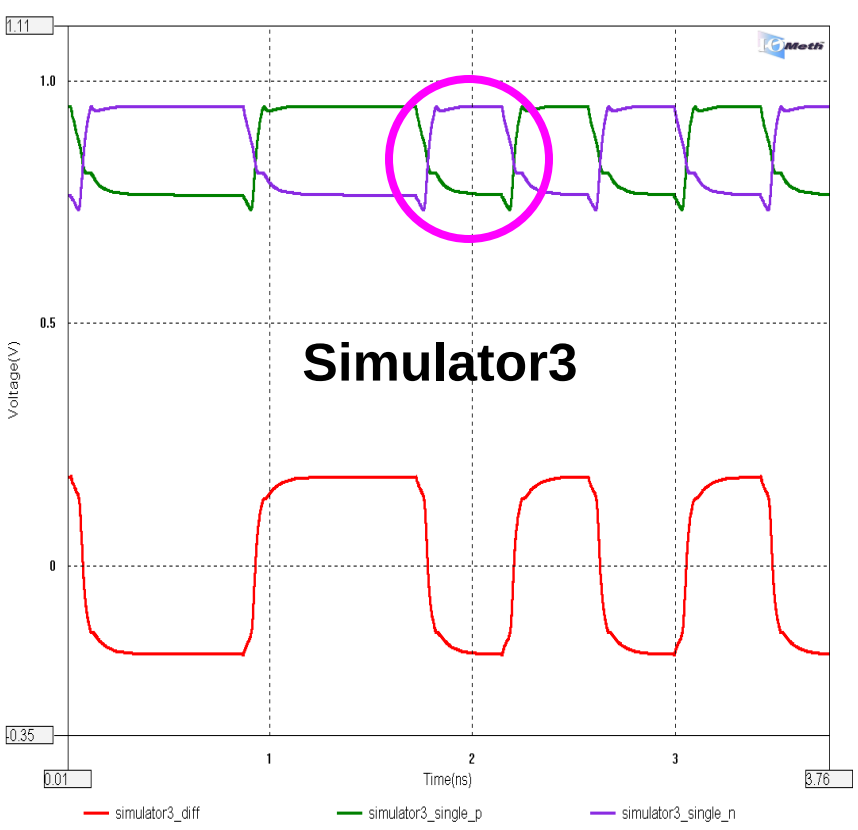
Driver IBIS VT curves

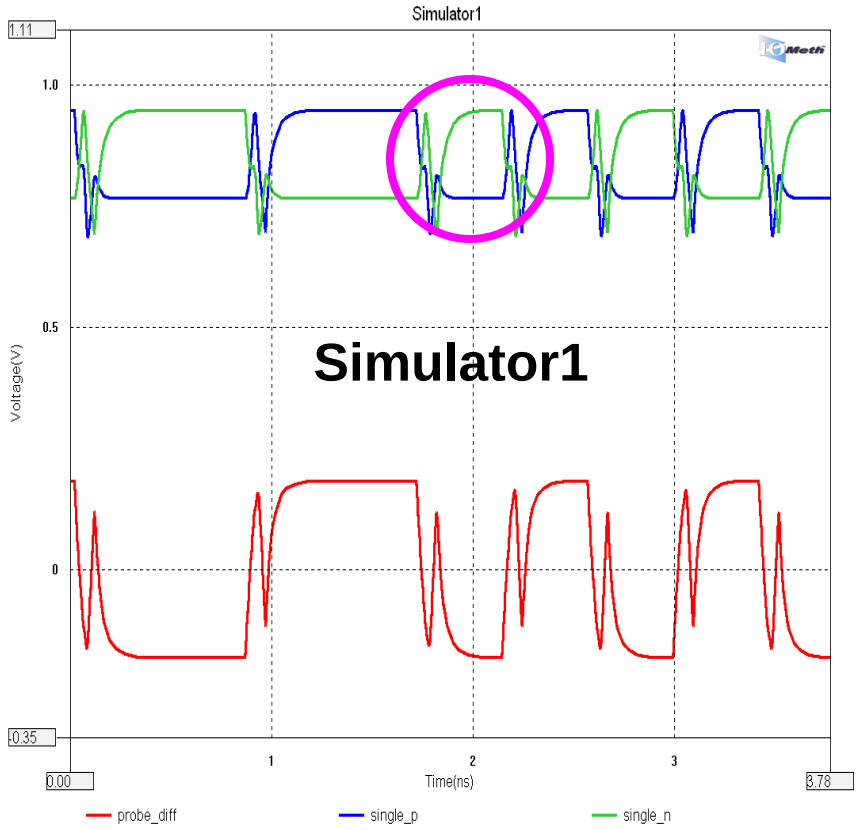


Receiver IBIS IV curves

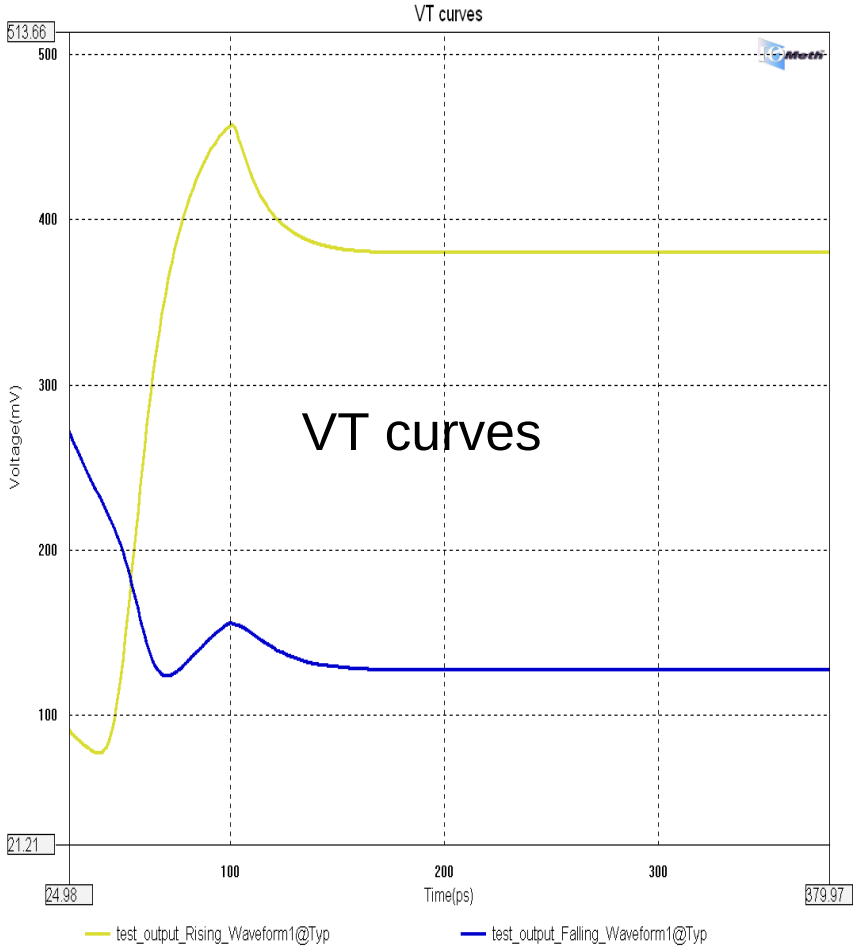


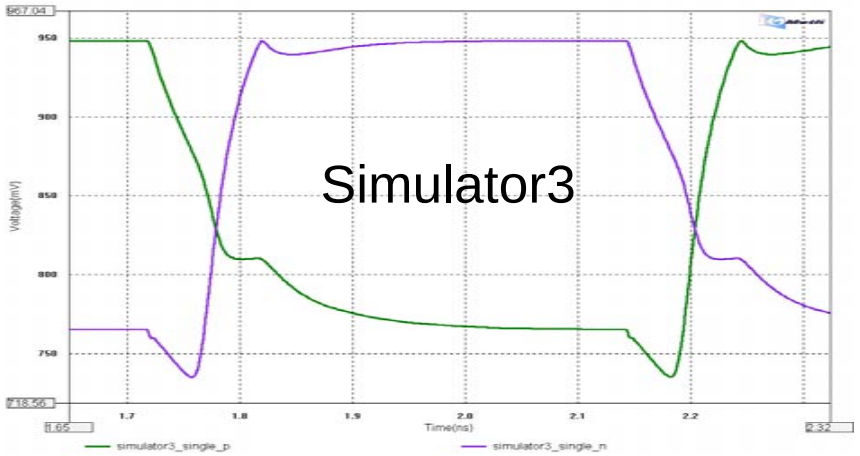
Simulator1 and Simulator3 results

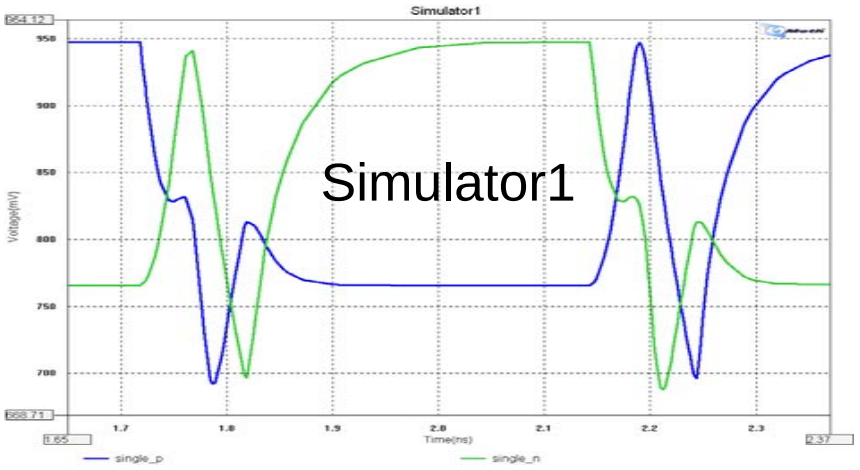




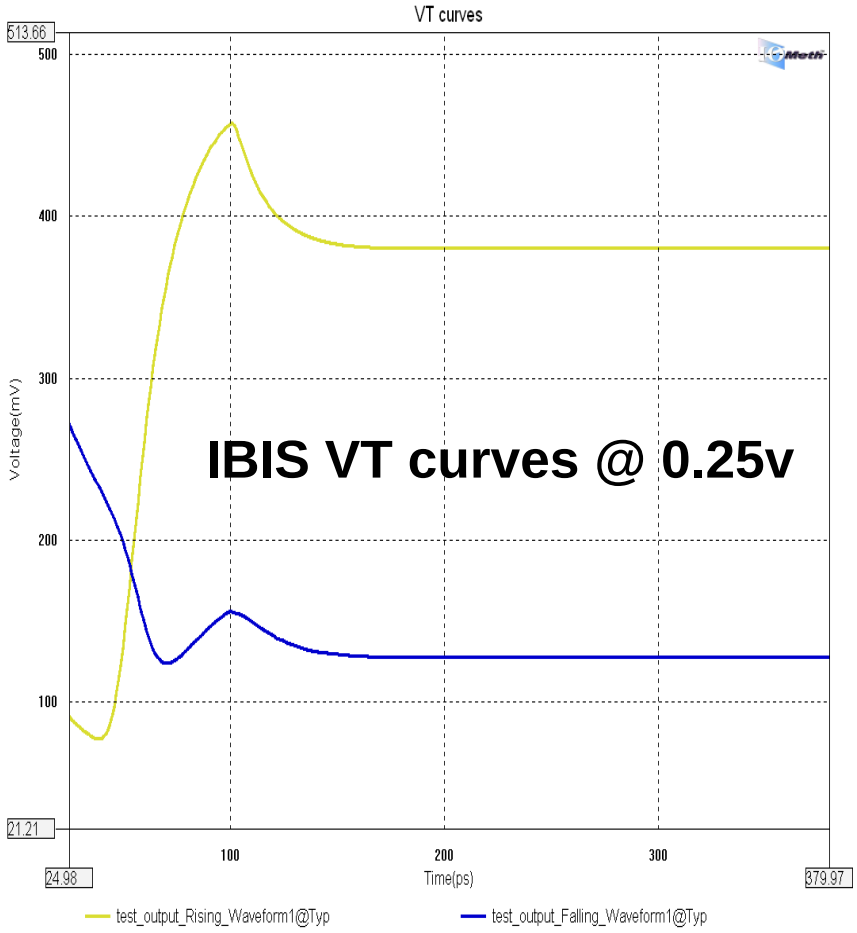
VT curves and Simulator1 / Simulator3 results

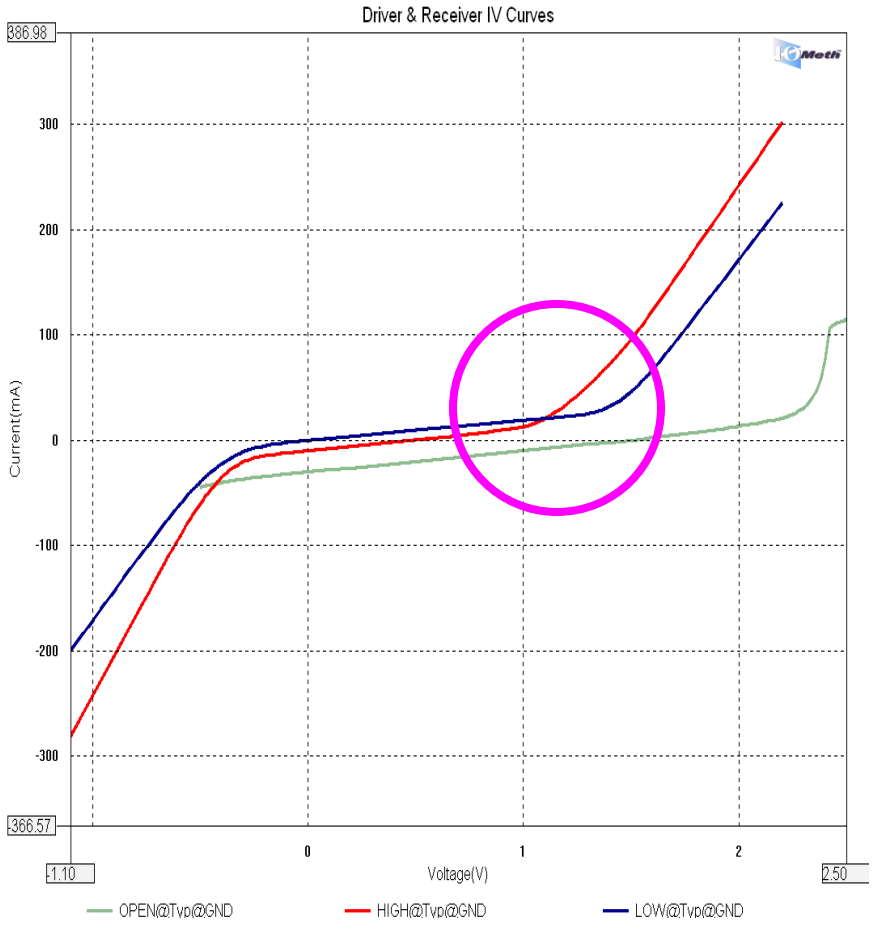






Inconsistency in pullup/pulldown & VT curves in the working range





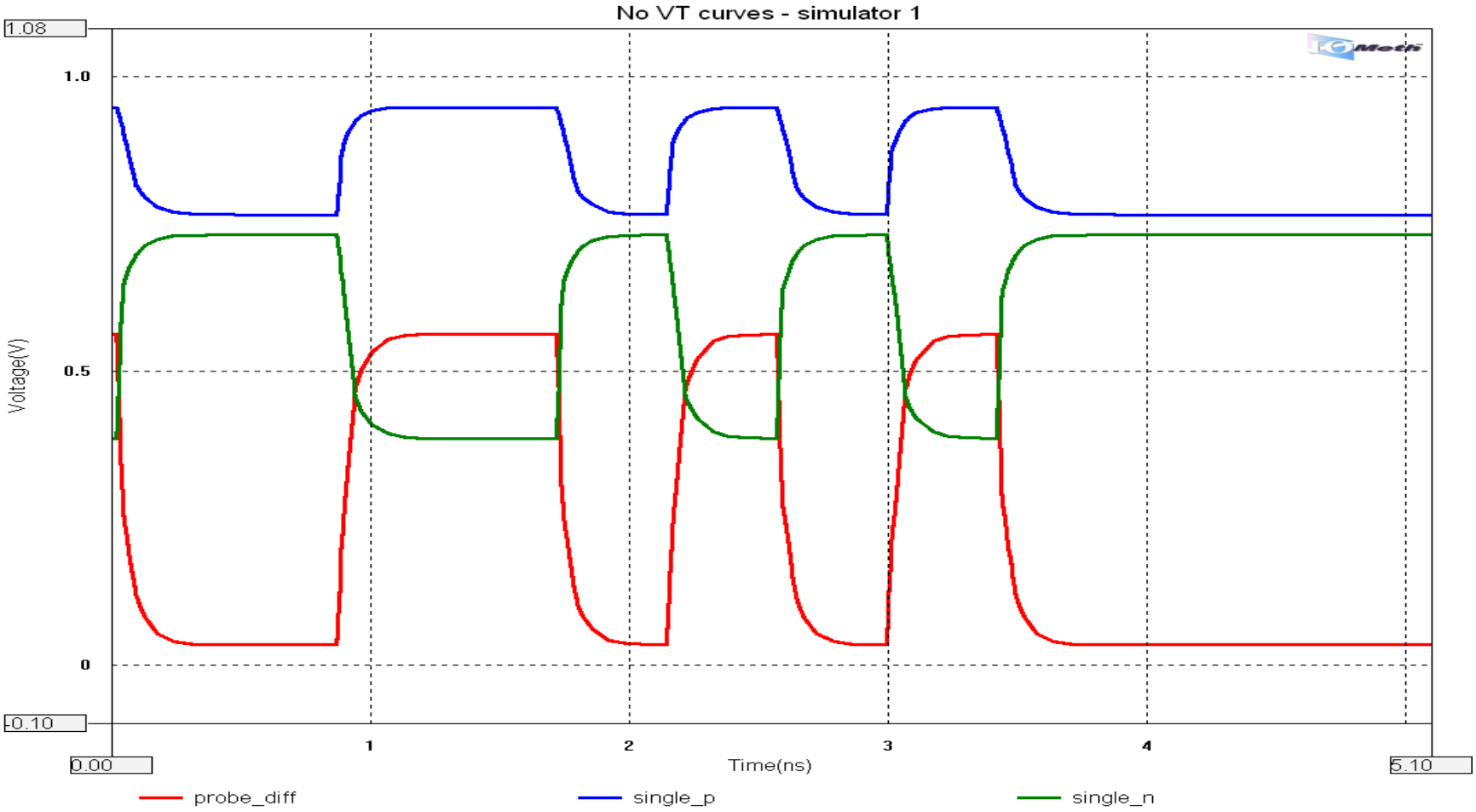
Analyze

- Single_p and Single_n swings are between ~760mv and ~940mv
- Small receiver load (~ 5 ohm) moved working range up to inconsistency driver IV/VT curve area
- Simulators are guessing the results

Conclusions – It should be what we learned

- For validations
  - We need to go down to the application level. The normal test load validation maybe not enough.
  - Simulators will guess if there is no enough data to be calculated. No one could claim the guessing is accurate.
- For IBIS models (Making)
  - Make sure to give consistent VT/IV curves in your buffer working range.
  - The accurate IBIS models should give simulator enough data for processing. Anything simulator has to guess, it will be not accurate.

Simulated without VT curves



Low cost, High Performance & Accurate

IOMeth™

Professional SI Consulting Services & Tools

www.iometh.com