IBIS 4.1 Status and Update

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IBIS 4.1

- IBIS 4.0 status
- IBIS 4.1 status
- Approved BIRDs
- Open BIRD
- Next steps

IBIS 4.0 Status

- Voted in July 2002
- Parser expected Q3/03
- IBIS 4.0 contains
  - 11 new BIRDS
    - Expanded input threshold specifications
    - Golden waveforms
  - The usual parser bug fixes

IBIS 4.1 Status

- First pass document

  http://www.eda.org/pub/ibis/wip/ver4_1a.ibs

- Five approved BIRDs
  - BIRD75.8, BIRD77.2, BIRD78.1, BIRD80.1, BIRD81.1
  - The usual parser bug fixes
- One open BIRD
  - Not expected to be in IBIS 4.1

Five Approved BIRDs
BIRD75.8

- Multi-lingual support
- First submitted: 3/29/02
- Approved: 1/10/03
- Supports SPICE 3f5, Verilog-AMS, VHDL-AMS
- External model files (subcircuits)
- No parameter passing into model files

Five Approved BIRDs
BIRD75.8

|-- [Component]

| ...

|-- [Node Declarations]

|-- [End Node Declarations]

| ...

| ...

|-- [Circuit Call]

|-- [End Circuit Call]

| ...

|-- [Model]

| | ...

| |-- [External Model]

| |-- [End External Model]

| | ...

| ...

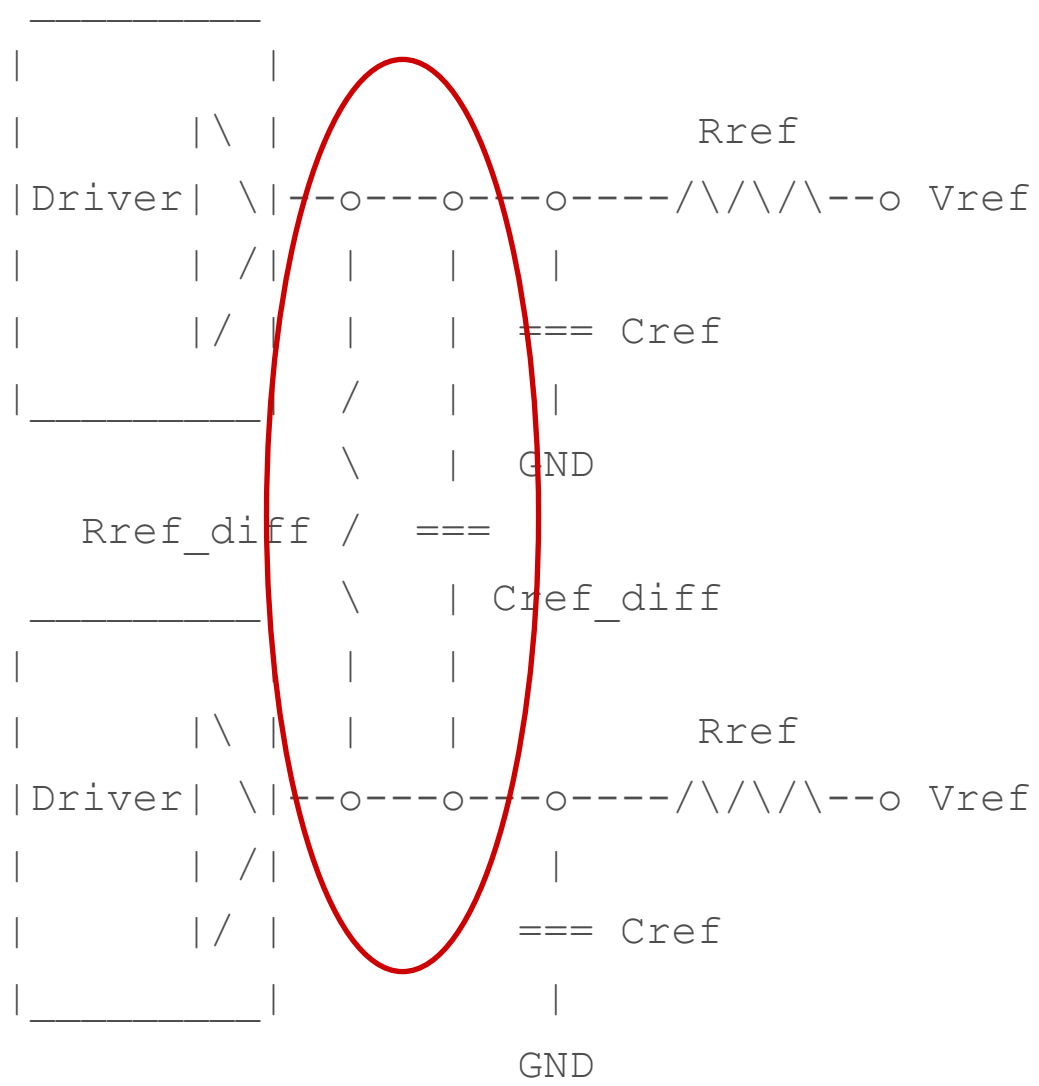
|-- [External Circuit]

|-- [End External Circuit]

| ...

Approved BIRDs
BIRD77.2

- New model types
  - Input_diff
  - Output_diff
  - I/O_diff
  - 3-state_diff
- New timing subparameters
  - Rref_diff
  - Cref_diff



Approved BIRDs

- BIRD78.1
  - Extend line length to 120 char
- BIRD80.1
  - Add ext_ref as new [Pin Mapping] column
- BIRD81.1
  - Clarification of models in [Pin] section
  - Using [Series Pin Mapping] description earlier

Open BIRDs

- BIRD 74.4, EMI Parameters
  - Add EMI parameters to IBIS
  - First submitted, March 19, 2002
  - Discussions in IBIS Open Forum
  - Several revisions

Next Steps

- IBIS Futures Committee edits rough draft
- Draft version of 4.1 goes to IBIS Open Forum
- Open Forum discusses draft
  - Revisions
  - Additions
  - On third meeting, can come up for a vote
- Parser development (bidding, funding, coding)
- Submit to EIA as IBIS 656-B

Examples of AMS models

- Dan Fitzpatrick and Ira Miller, “Analog Behavioral Modeling with the Verilog-A Language”, Kluwer Academic Publishers, 1998. Includes software and models on CD.
- http://www.eda.org/verilog-ams/htmlpages/examples.html
- Lynne Green, DesignCon 2003 Summit.
- Arpad Muranyi, today.

Late-breaking News

- Business Wire, June 2, 2003
  Accellera Approves Four New Design Verification Standards

  NAPA, Calif.--(BUSINESS WIRE)--June 2, 2003--Accellera, the electronics industry organization focused on language-based electronic design standards, today announced that its Board and Technical Committee members -- systems, semiconductor and design tool companies -- have approved four new standards for language-based design verification. The new Accellera standards include Property Specification Language (PSL) 1.01, Standard Co-Emulation Application Programming Interface (SCE-API) 1.0, SystemVerilog 3.1 and Verilog-AMS 2.1.