Simultaneous Switching Noise in IBIS models

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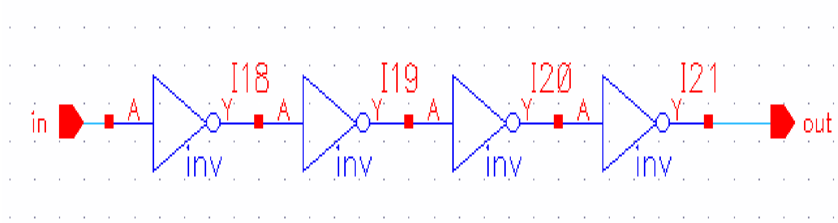
Outline

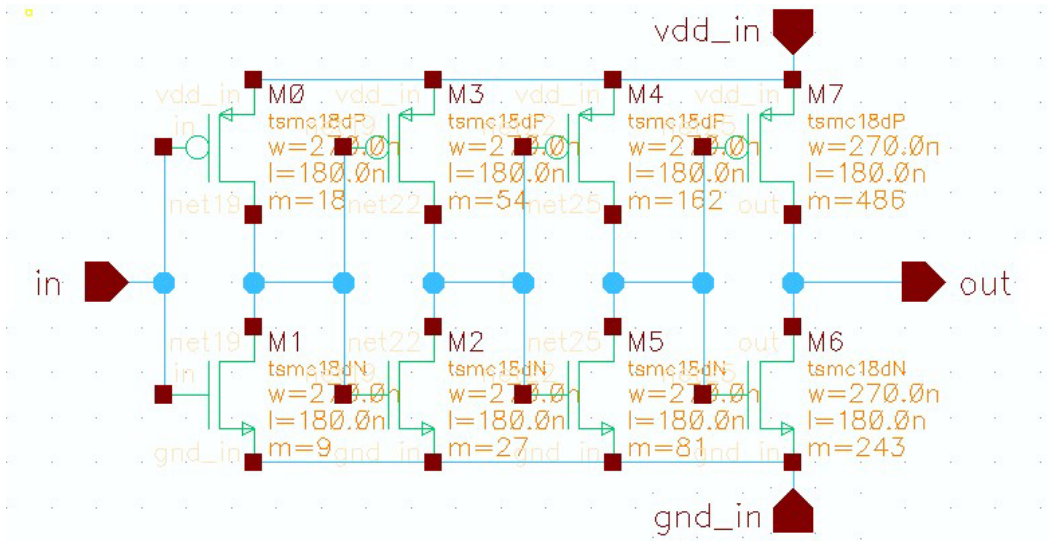
- **Background**
- **IBIS V Spice**
  - Buffer Cct
  - B Model
  - Results
- **IBIS V Spice V Spline**
  - Spline Functions and Finite Time Difference approximation
  - Methodology
  - Results
  - Conclusion
- **Future Work**

Background

- **s2ibis1 and s2ibis2**
- **SSN issues.**
- **IT table and other proposed solutions.**

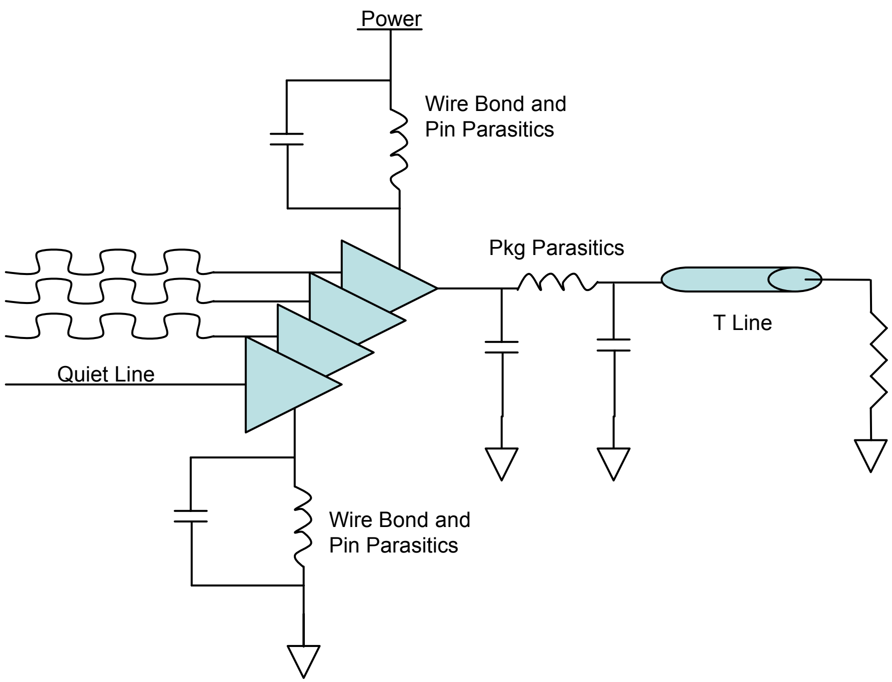
Comparing SPICE and IBIS





- Cascaded Driver
- Non-Inverting

Comparing SPICE and IBIS..



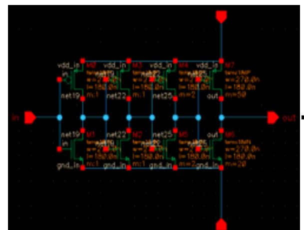
- **Each driver connected to a lossless 25 ohms T Line.**
- **25 ohm terminations used.**
- **3 drivers given simultaneously switching inputs**
- **4th driver kept quiet.**
- **Power/Ground supplied through pin parasitics.**

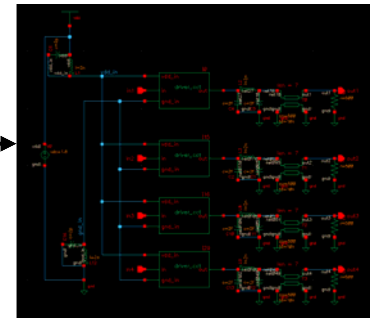
B Element in HSPICE

```
.subckt  buffer11 nd_pu0 nd_pd0 nd_out0 nd_in0
b0 nd_pu0 nd_pd0 nd_out0 nd_in0
+ file = 'driver_s.ibs'
+ model = 'driver'
+ typ = typ power = off
.ends
```

- Sub-Circuit of driver is recreated using IBIS model.
- To simulate power/ground bounce and SSN, internal Power Sources are not used.

Comparing SPICE and IBIS





s2ibis3

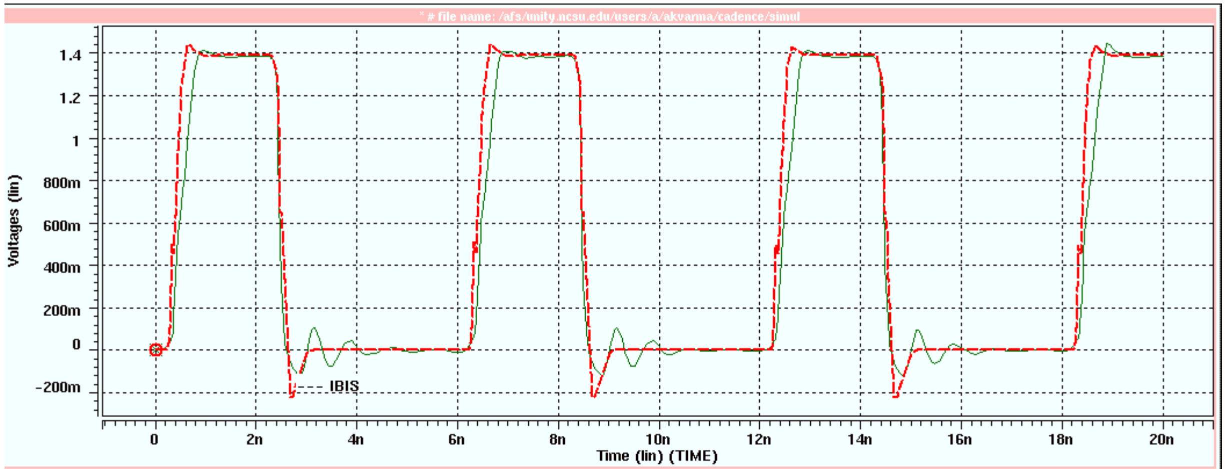
IBIS MODEL

B Element (Hspice)

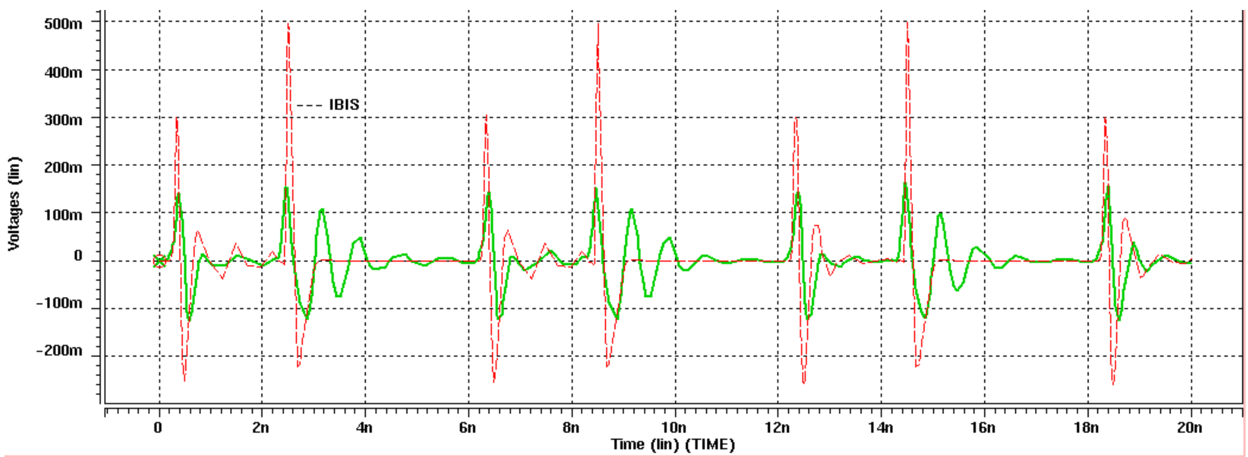
Reads in IBIS model of **b**uffer from *.ibs file

Construct Equivalent circuit of 4 drivers

Output from Drivers

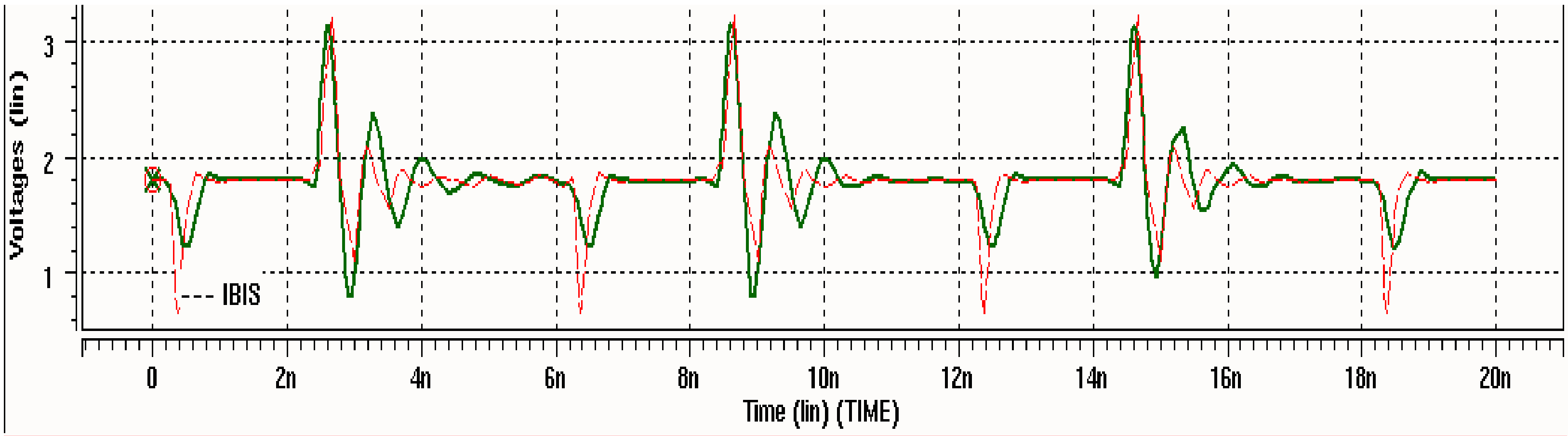


Output in the Switching Drivers

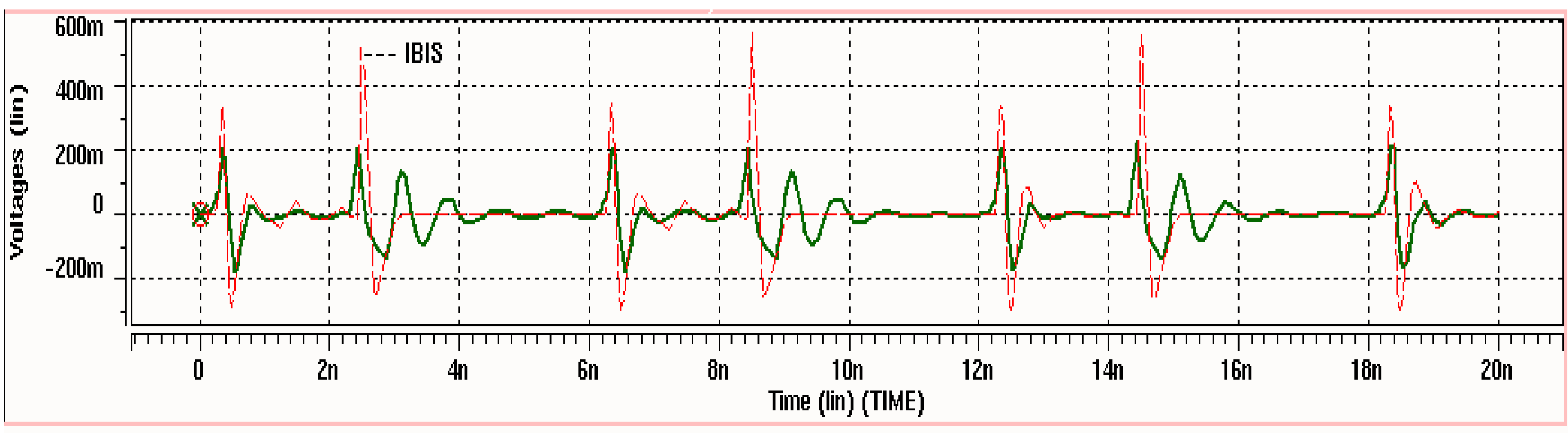


Output in the Quiet Driver

Power/Ground Bounce



Power



Ground

Spline Functions and Finite Difference Approximation[1]

- BLACK BOX
  - Knowledge of Internal circuitry not necessary.
- Output load independent
- Static Characteristic Modeling + Dynamic Characteristics (by capturing the previous time instances)

1. *Macro-Modeling of Non-Linear I/O drivers using Spline Functions and Finite Time Difference Approximation, B Mutnury, Jim Liibous and Madhavan Swaminathan, EPEP 2003.*

Spline Functions (cont)

- **Non-Linear relation is drawn between driver O/P current and voltage.**

$$i_o(k) = w_1(k) f_1(v_o(k)) + w_2(k) f_2(v_o(k))$$

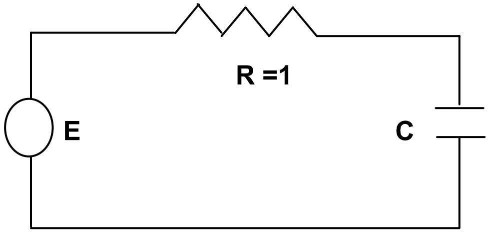
- **f_1 and f_2 are submodels relating O/P currents and voltages when driver is set high(f1) and low(f2) and have both static and dynamic information**

$$f_1(v_o(k)) = fs_1(v_o(k)) + fd_1(v_o(k))$$

$$f_n(k) = A_{nm} v_o^{m}(k) + A_{nm-1} v_o^{m-1}(k) + \ldots$$

- **Static values can be obtained using DC sweep and using n^th^ order cubic spline.**

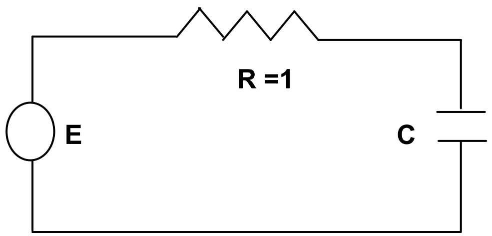
$$\frac{f_1(t) - f_1(t - \Delta t)}{\Delta t} = \frac{\Delta i_{oh}}{\Delta t} = i'_{oh}$$



Spline Functions (cont)

- Dynamic values can be obtained by including the previous time instances of the driver output current.

$$\frac{f_1(t)-f_1(t-\Delta t)}{\Delta t}=\frac{\Delta i_{oh}}{\Delta t}=i'_{oh}$$



- W_1 and W_2 are used for transitioning from 1 logic state to the other. They are obtained by estimating submodels (f_1 and f_2) for 2 loads and by linearly inverting

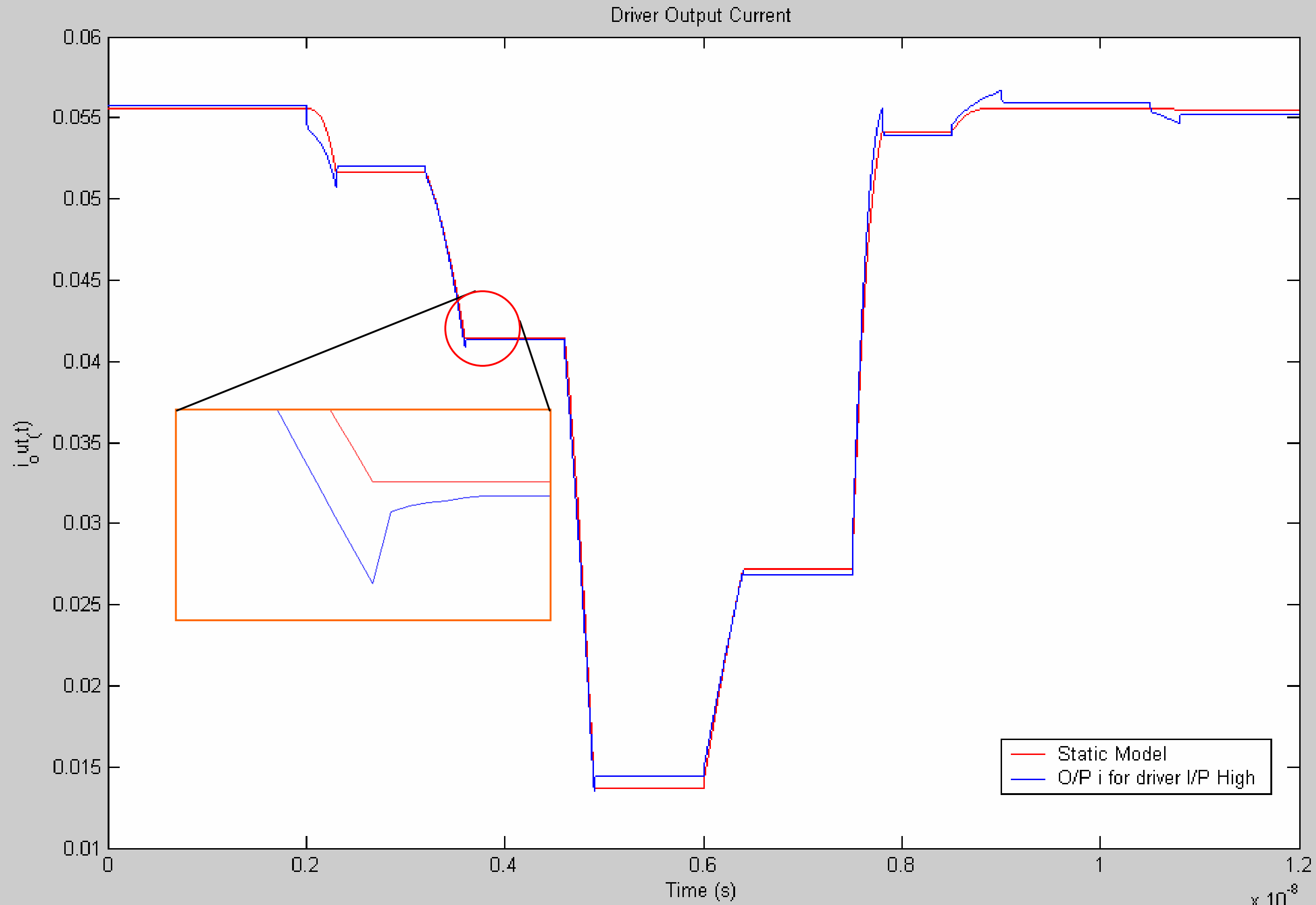
$$\begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} f_{1a} & f_{2a} \\ f_{1b} & f_{2b} \end{bmatrix}^{-1} \begin{bmatrix} i_a \\ i_b \end{bmatrix}$$

$$i_o(k)=w_1(k)f_1(v_o(k))+w_2(k)f_2(v_o(k))$$

and are represented as PWL voltage source.

Static Modeling Using Spline

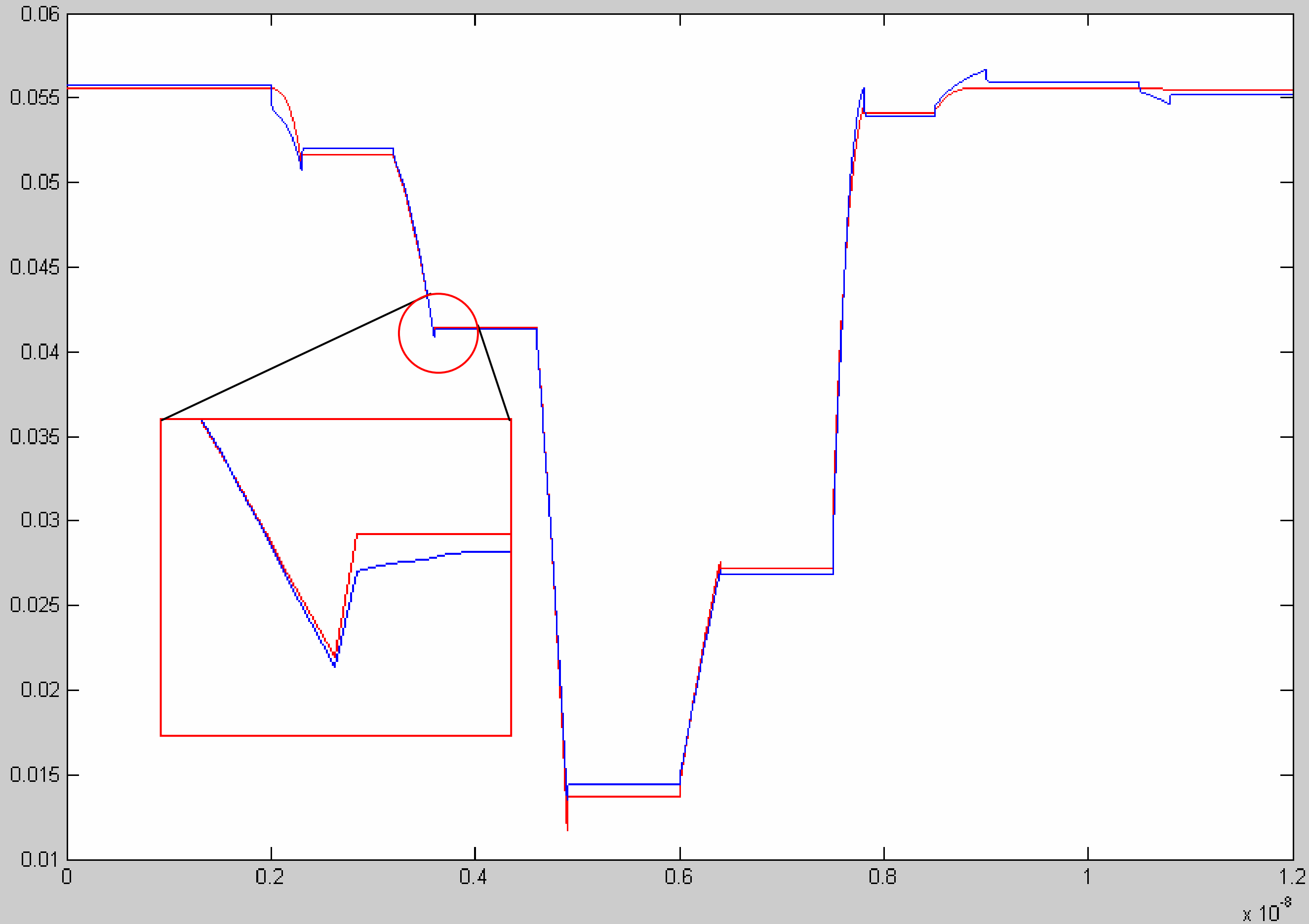
Driver Output Current Vs Time



STATIC MODEL

(Using 3rd Order Cubic Spline)

Capturing Dynamic Behavior



Spline Function with Finite Time Difference

(Using 1 previous time instance)

Spline Modeling

Spice Netlist

- **Spice Macromodel generated using VCVSs (E elements) and CCCs (F elements).**
  - Static Characteristics can be represented using VCVS
  - Dynamic Characteristics represented using state equations

$$i_o(k) = w_1(k) f_1(v_o(k)) + w_2(k) f_2(v_o(k))$$

  - Non-Linear relation between driver o/p current and voltage is now a subcircuit.

```
.subckt driver1 out1 gnd
…
...
.ends (driver1)
```

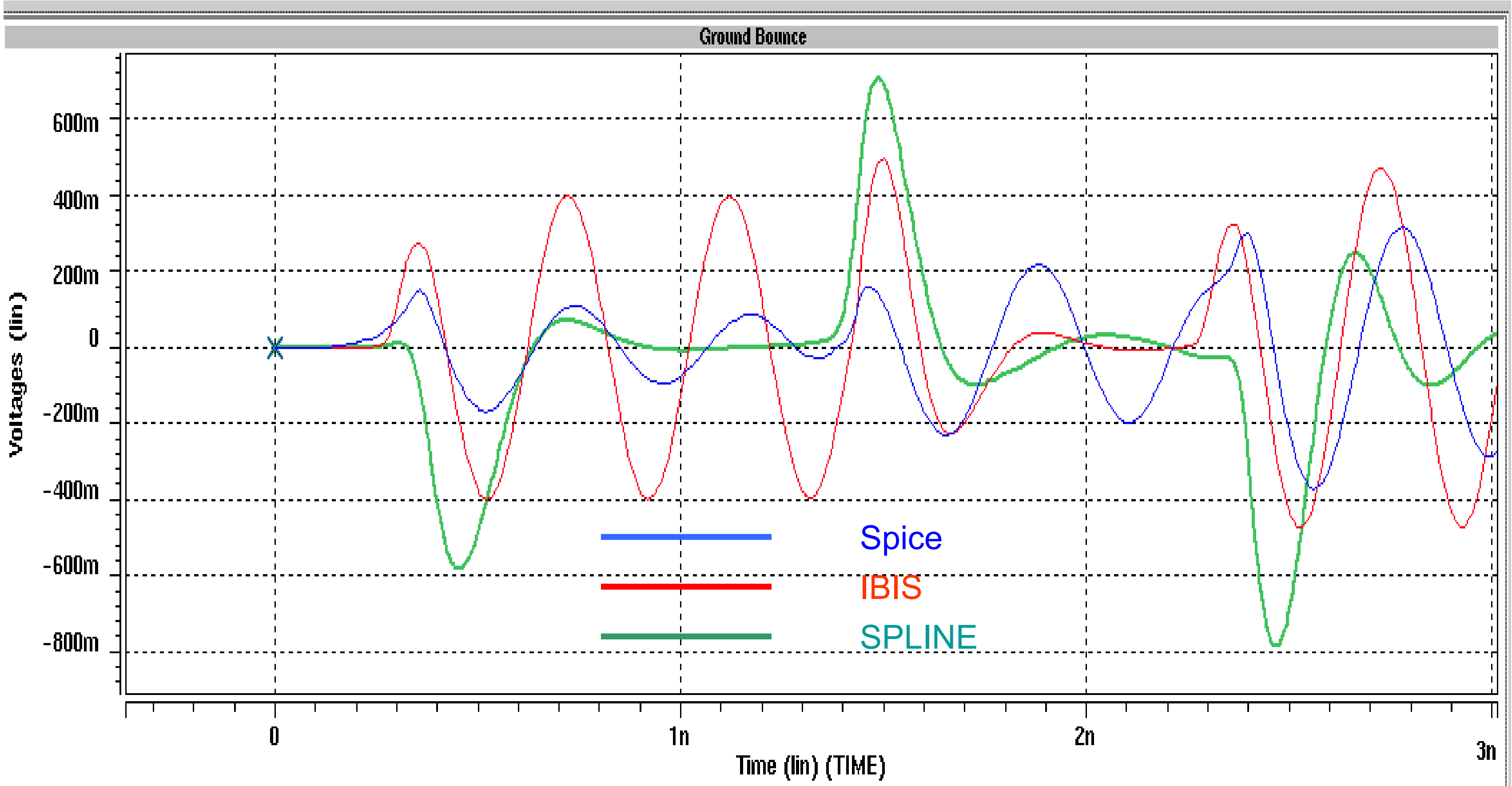
Comparing SPICE, IBIS & SPLINE

- Spline method is complex and no IBIS like automation exists.

- The models resulting from IBIS, and SPLINE are compared with SPICE simulation of the transistor model.

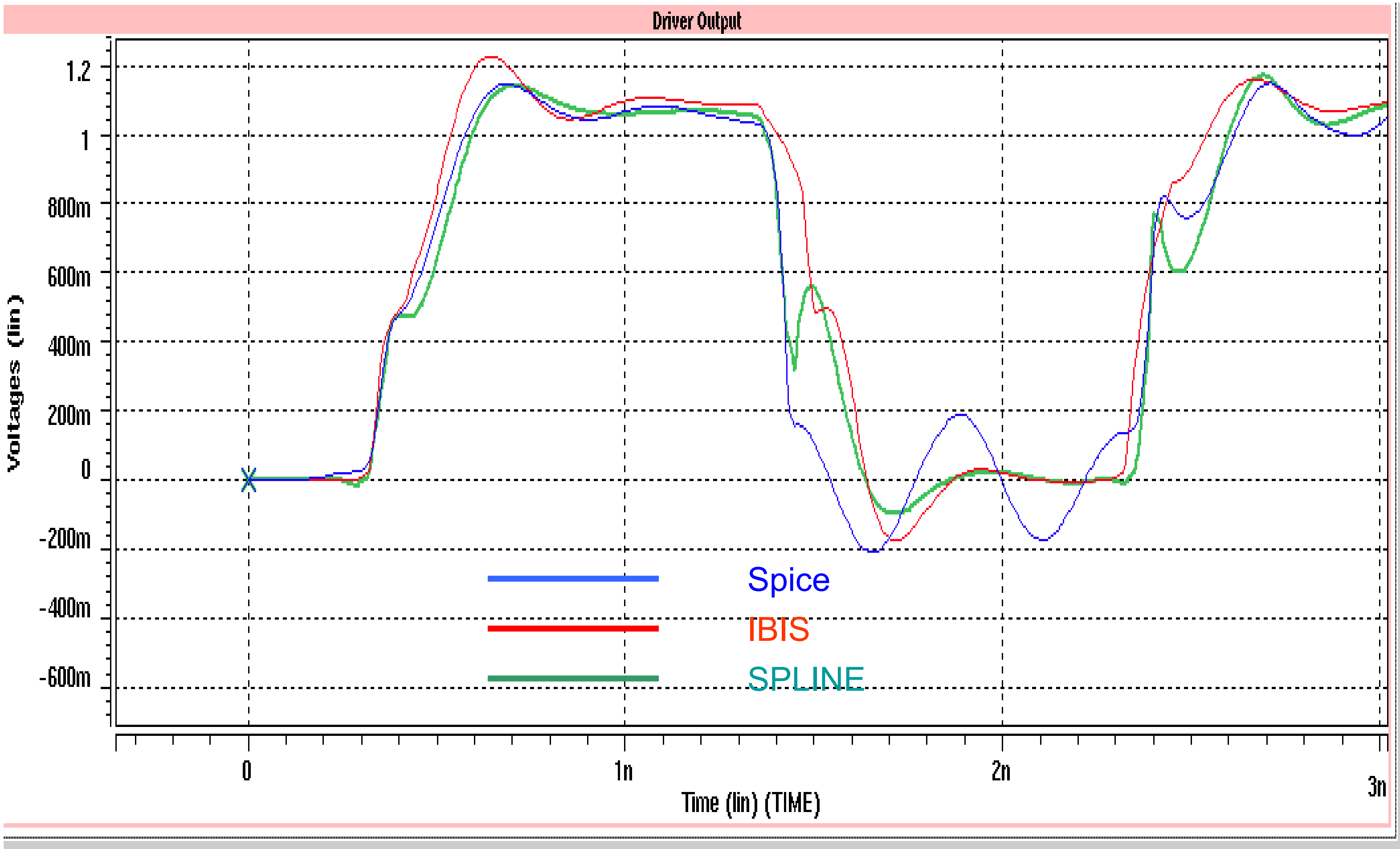
Comparing SPICE, IBIS & SPLINE

Ground Bounce



Comparing SPICE, IBIS & SPLINE

Output Comparison



Comparing SPICE, IBIS & SPLINE

	IBIS	Spline
Mean Square Error	3.05E-02	1.87E-02
Maximum Error	6.08E-01	5.08E-01

IBIS and Spline method compared with Spice Simulation of the Transistor Model

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Comparing SPICE, IBIS & SPLINE

Conclusions

- <u>SPLINE Pros</u>
  - More accurate than IBIS
  - More general than IBIS
    - Mathematical

- <u>SPLINE Cons</u>
  - Not automated
  - Computationally intensive
  - Complex to implement
  - Slower

Questions

- **Is it worth having a 50% improvement in SSN simulation accuracy?**
  - How much is speed valued when IBIS is used?
- **Can SPLINE models be generated using measurements?**

Future Work

- A combination of Spline method and IBIS is under study.
- The integrated solution would include
  - **the accuracy and the mathematical background of the spline methodology and**
  - **the automation and the simplicity of IBIS.**

Acknowledgments

Prof. M. Swaminathan and B. Mutnury, Georgia Instt. of Technology for sharing code to model using Spline functions and Finite Time Difference Approximation