2005 DAC IBIS SUMMIT MEETING
AGENDA

June 14, 2005
Gold Key I and II, Anaheim Marriott
Anaheim, California

8:00 AM **Refreshments & Sign In**

8:30 AM **Introductions**
- Welcome to Summit
- Introductions
- Opens for Issues, Discussion Topics

8:45 AM **IBIS Chair's Report and Roadmap**
Michael Mirmak, Intel Corporation

9:00 AM **Library Modeling Project at Silicon Integration Initiative (Si2)**
Sumit Dasgupta, Si2
H. John Beatty, IBM

9:30 AM **Power Integrity Proposal Regarding BIRD95.5**
Ken Willis, Cadence Design Systems

10:15 AM **BREAK**

10:30 AM Election of Officers for 2005-2006

10:45 AM Multi-buffer Simulation Using BIRD95.5
Dr. Zhiping Yang and Ilyoung Park
Cisco Systems, Inc

11:15 AM Multi-Gigabit SerDes Simulation Using IBIS v4.1 (VHDL-AMS)
Syed Huq, Cisco Systems, Inc
Ian Dodd, Mentor Graphics

12:00 PM LUNCH
Pre-registration required

1:00 PM IBIS 4.1 Macros for Simulator Independent Models
Arpad Muranyi, Intel Corporation

1:30 PM Things You Can Learn From VI Curves
Todd Westerhoff, Cisco Systems, Inc.

2:00 PM JEITA-IBIS Joint Meeting Report and Asian IBIS Summit
Takeshi Watanabe, NEC
Chair, JEITA EDA WG

2:30 PM Asian IBIS Summit
Bob Ross, Teraspeed Consulting Group

3:00 PM BREAK

3:15 PM Opens/Discussion

4:55 PM Concluding Items
- Next Open Forum Meeting - June 24, 2005

5:00 PM End of IBIS Summit Meeting