EIA IBIS Open Forum Minutes

Meeting Date: **June 5, 2007**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2007 PARTICIPANTS

Agilent	Ian Dodd*, Radek Biernacki, Saliou Dieye, Riccardo Giacometti
AMD	Nam Nguyen, Tadashi Arai
Applied Simulation Technology	(Fred Balistreri)
Apple Computer	(Bill Cornelius)
Cadence Design Systems	[Lance Wang], C. Kumar, Hemant Shah*, Patrick dos Santos
Cisco Systems	Syed Huq*, Tram Bui, AbdulRahman Rafiq, Huyen Pham, Darja Padilla, Mike LaBonte*, Paul Ruddy, Gurpreet Hundal, Luis Boluna, Ehsan Kabir, Jehyoung Lee, Susmita Mutsuddy, Eddie Wu
Ericsson	Anders Ekholm*, Ole Segtum
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji*
Intel Corporation	Michael Mirmak*, Arpad Muranyi*
LSI	Frank Gasparik, Kim Helliwell, Dinh Tran, Praveen Soora
Mentor Graphics	John Angulo*, [Ian Dodd], Eric Rongere, Stephane Rousseau, Bill Hargin*, Patrick Carrier*
Micron Technology	Randy Wolff, Pavani Jella
Samtec	(Corey Kimble)
Signal Integrity Software	Barry Katz*, Douglas Burns, Mike Steinberger, Walter Katz, Todd Westerhoff*
Sigrity	Sam Chitwood*, Sandy Dung
STMicroelectronics	Antonio Girardi, Giacomo Bernardi, Roberto Izzi
Synopsys	Ted Mido
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino
Texas Instruments	Otis Gorley, Richard Ward*, Bonnie Baker
Toshiba	(Yasumasa Kondo)
Xilinx	Bruce Bandeli, David Banas*
ZTE	(Shunlin Zhu)
Zuken	Michael Schaeder, Ralf Bruening, John Berrie*

OTHER PARTICIPANTS IN 2007

74ze Engineering	Linc Jepson
Actel	(Prabhu Mohan)
Agere	(Nirav Patel)
Altera	Hui Liu, Zhe Lin, Ravindra Gali, Salman Jiva
Ansoft Corporation	(Michael Brenneman)
Apache Design Solutions	(Ji Zheng)
Applied Telisis, Inc. (ATI)	Vladimar Mandrusov
Cavium Networks	Johann Nittmann
ChipX	Jay Hidy, Oren Dvir
Cybernet Systems	Kazuhiki Kusunoki
EFM	Ekkehard Miersch
Enterasys	Robert Haller
Extreme Networks	Kevin Ko
Fluent	(Chetan Desai)
Force10 Networks	Robert Badal
Free Electron Software	Al Davis*
Freescale	Jon Burnett
GEIA	(Chris Denham)
Hewlett Packard	Shafiq Rahman
Huawei Technologies	ChunXing Huang, Bob He
IBM	Michael Sorna, Adge Hawes
Infineon	Christian Sporrer
Integrated Circuit Systems (ICS)	(Dan Clementi)
IO Methodology	Lance Wang*
JEITA	Atsushi Ishikawa*
Juniper Networks	Raul Lozano
Leventhal Design	Roy Leventhal
Lynguent	Andrew Levy
National Institute of Applied Science (INSA)	Etienne Sicard
National Instruments	Lee Maixman
Netlogic	Eric Hsu
NEC Electronics Corporation	Takeshi Watanabe*, Hock Seow, Huy Tran
NESA	Edward Sayre
Nokia Siemens Networks GmbH[1]	Eckhard Lenski, Flavio Maggioni, Roberto Preatoni, Umberto Gatti, Massimo Ceppi
Northrop Grumman	Dusan Radosevic*
Nuova Systems	Zhiping Yang, Lin Shen
NXP	H N Sudarshan
Optimal Corporation	Marc Kowalski*
Panasonic	(Atsuji Ito)
Politecnico di Torino	Igor Stievano, Michelangelo Bandinu
Renesas Technology	Takuji Komeda
Samsung	Sang-Soo Park

Sedona International	Joe Socha
Siemens AG [1]	[Eckhard Lenski], Manfred Maurer
Silego	(Joe Froniewski)
Sun Microelectronics	Leon Yang
Tiburon Design Automation	Patirick Challacn
White Electronics Designs	John Perez
Xyratex	Paul Levin, Joseph Chan
ZTE	(Shunlin Zhu)

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

[1] Nokia Siemens Networks is a new company formed by the merger with a former group at Siemens active with the IBIS Committee.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
June 22, 2007	1-916-356-2663	3	673-0535

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in San Diego, California at the Omni Hotel during the 2005 Design Automation Conference (DAC). 25 people from 19 organizations attended. The attendees were approximately evenly split between EDA tool vendors, model users and model makers.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis-information.org/summits/jun07/

Michael Mirmak opened the meeting by thanking event sponsors Mentor Graphics and the IBIS Open Forum for their financial and logistical support. Michael also thanked the presenters and participants for attending.

Michael asked if there were any new issues or discussion items to add to the agenda. No issues were raised.

PRESENTATIONS AND DISCUSSION TOPICS

The rest of the meeting consisted of presentations and discussions. These notes capture some of the content and discussion. More details are available in the documents uploaded to the location noted above.

IBIS CHAIR'S REPORT AND ROADMAP

Michael Mirmak, Intel Corporation

Michael Mirmak summarized the current state of the IBIS Open Forum and its activities. IBIS membership in 2006 was 34, with member renewals continuing. Successful events were held in Japan and China, while IBIS 4.2 was standardized by ANSI. A new parser, version 4.2.1, was completed and distributed to the IBIS community. He also noted the efforts of the IBIS task groups, including the work of the Ad Hoc Interconnect group in completing a proposal for a Touchstone® 2 S-parameter specification.

Finally, Michael thanked the members and current officers -- Syed Huq, Randy Wolff, Lance Wang and Bob Ross -- for their help in "making IBIS happen" over the past year.

IBIS QUALITY REPORT

Mike LaBonte, Cisco Systems

Mike provided an overview of the Quality Task Group's work by using a board-game analogy, showing their efforts as eventually resulting in a new quality level specification, but getting there in a very indirect fashion. The new specification provides updated quality levels, in addition to special designators for correlation. The group has completed reviews of the header and [Component] keywords, and is about to begin analyzing the [Model] section of the specification, with a brief leap ahead to address issues with [Receiver Thresholds] also discovered in earlier parser editions. Feature-selective validation will be addressed near the end of the group's analysis.

Some questions emerged regarding the validity check on pin parasitics. The team's recommendation is to check the R, L and C values to ensure the delays and impedances are reasonable, but this may imply that lumped values are appropriate for all interface signaling speeds and edge rates. Mike will raise this at the next meeting.

IBIS-TO-SPICE CORRELATION – A STORY OF FIVE METRICS

David Banas, Xilinx Inc.

David presented a brief historical overview of the development of IBIS quality efforts, from the original IBIS Accuracy Specification, by the use of an extended "Star Wars" motif. He then suggested that, while curve-overlays may be generally effective for comparing IBIS to measurement or transistor-level simulation data, more specific metrics are needed to quantify problems. He proposes five: high DC level, low DC level, rise time, fall time and duty cycle.

He showed a specific example of models compared in a large group, between IBIS and their original SPICE implementations. Most of the parameters matched well, but rise and fall times were significantly different. David blames this on poor interpolation of points in the table for the transitions, thereby assuring incorrect linearization for the buffer output edge. Some discussion erupted whether this was properly executed in S2IBIS3. David concluded by noting that many of the accuracy handbook checks can be automated through common SPICE tools and measurement techniques. He requested specific feedback on the metrics, asking whether others would be needed.

IBISCHK VERSION 4.2.1 AND FUNNY IBIS MODELS

Bob Ross, Teraspeed Consulting Group

Bob provided a summary of the recent work on the development of IBISCHK4, version 4.2.1, as released to the public. The new parser implements monotonicity checking of combined I-V tables, Caution flags as recommended by the IBIS Quality Task Group, and a fix to a bug with [Receiver Thresholds]. Unfortunately, the parser also reports new warnings not seen in previous editions, while reducing the total number of warnings and errors and also eliminating line-number reporting of specific issues. These are being addressed in an IBISCHK4, version 4.2.2, expected later this quarter. Lance Wang asked if the -caution flag should be eliminated and the Caution messages always printed. Bob stated that this could be considered.

In addition, Bob noted that Agilent Technologies provided a list of changes to the parser code structure suggested to help EDA tool vendor integration of the code into their software products. This may be discussed at a future meeting of the IBIS Open Forum. Bob closed by showing two pathological IBIS model cases. One provides zero values for almost every keyword and subparameter entry in the file, while the other inverts I-V and V-t tables from their expected polarities. Both pass the parser with few, if any, warnings or errors. These illustrate that errors of intent may not be detected by even sophisticated parsers.

MORE ON INITIAL DELAY ISSUES

Lance Wang, IO Methodology Inc.

Lance provided an update on voltage-versus-time table correlation issues that have been frequently discussed at previous summits and on the IBIS e-mail reflectors. He noted that a “good” IBIS model, showing perfect correlation to transistor-level simulations for individual rising and falling edges, may fail to correlate when data patterns are involved. The problem stems from data patterns violating the transition limitations of the buffer, and cannot be resolved by trimming initial time delays from the V-t tables or by using only [Ramp] data.

Arpad Muranyi noted that this is the “switching into an unfinished edge” problem that is commonly ignored in generating IBIS model data. Lance recommended, at a minimum, keeping V-t tables shorter than the bit width of the signal to be simulated. While documented in the IBIS Cookbook, this is not necessarily observed or well-understood in the IBIS community. Lance suggested that adding a state-transition factor to the commonly understood IBIS table equations may help address the problem. Arpad noted that the two-equations, two-unknowns format of the IBIS table formulas is already unable to deal with reactive characterization loads; additional factors to address transitions would not solve this issue.

CORRELATION OF MODEL SIMULATIONS AND MEASUREMENTS

Roy Leventhal, Leventhal Design and Communications

David Banas presented the material on behalf of Roy Leventhal, who could not attend the Summit. David summarized the basic theory behind statistical analysis of variance, including distributions, accuracy and precision. While direct waveform correlation, as defined by Figures of Merit in the IBIS Accuracy Specification, is useful, a new method called Feature Selective Validation (FSV) has become popular for both frequency- and time-domain validation. This tends to be qualitative, but systems for converting this comparison to a quantitative measure have been developed.

The difficultly of FSV is that it compares only two specific measurements or waveforms. Broad statistical methods must be used to analyze groups of measurements or designs. These include Monte Carlo and DOE analysis, to help find the relationships between target outputs and input parameters based on a limited number of cases. ANOVA can also be used to help limit the inclusion of dependent variables that can skew a statistical analysis. Finally, careful measurement itself, through a number of good practices and industry standards, can be combined with all these methods to ensure quality data for correlation.

ELECTION OF OFFICERS

Michael Mirmak announced the available positions, responsibilities and the existing slate of nominees. No other candidates were nominated at the meeting. Without dissent, the following candidates were elected by the voting membership as officers for 2007-2008:

Chair: Michael Mirmak, Intel Corp.
Vice-Chair: Syed Huq, Cisco Systems
Secretary: Randy Wolff, Micron Technology
Postmaster: Bob Ross, Teraspeed Consulting Group
Webmaster: Syed Huq, Cisco Systems
Librarian: Lance Wang, IO Methodology, Inc.

Michael thanked the outgoing officers and congratulated the new officers. Later during the meeting, Michael presented some commemorative items to the outgoing board members, and Bob Ross presented one to Michael.

ASIAN IBIS SUMMIT REVIEW

Bob Ross, Teraspeed Consulting Group

Bob provided a summary of the attendance and feedback received on the October 2006 IBIS Summits in Asia. The Japan event hosted 35 participants at JEITA headquarters in Tokyo. The China summit, held in Shanghai, attracted over 160 participants who responded very positively in surveys regarding the event. Demand for technical topics for future events was evenly split between traditional topics like power delivery and more recent ones like interconnects or algorithmic modeling. Attendees requested publication of technical papers on-line, more time for questions and an announced “theme,” among other changes for future events. Bob closed by reminding the audience of the upcoming Asian summits in September of this year.

ISSUES WITH INTERFACING "2N" and "N+REF" BEHAVIORAL MODELS

Sam Chitwood, Sigrity

Sam compared and contrasted two different methods for modeling passive interconnects using S-parameters for signal integrity power delivery analysis applications. S-parameters, being a port-based representation, require terminals to be modeled using a pair of nodes, with one node acting as a reference (the "2N" representation). Such systems can also be represented, in a mathematically equivalent way, by representing all the physical nodes singly, with respect to a single REF reference terminal. This REF terminal has no physical meaning in itself, but is a mathematical convenience. As encrypted models and the use of global ground or ground-reduced interconnect models are prevalent, having a common reference node enables consistent connections and analysis when multiple interconnect models are connected together in a system simulation. These referencing issues have particular impact on the ICM improvements being discussed in the Ad Hoc Interconnect Task Group.

THE *-AMS EXPERIENCE

Arpad Muranyi, Intel Corporation

Arpad provided a comprehensive overview of the state of VHDL-AMS and Verilog-AMS integration with IBIS, in his experience, over the past several years. The *-AMS languages were originally intended to supplement traditional IBIS keywords and techniques by moving control over algorithms and data to the model author, thereby removing the time-consuming burden of defining and implementing new IBIS keywords for new functions. However, the *-AMS languages have not received widespread support, due to their cost of implementation to SI tools, which are typically less expensive than IC design tools. Further, the languages are more difficult to learn than SPICE and are believed not to be as convenient for expressing SERDES algorithms as other methods. Though the Macromodeling Library effort was designed to help bridge the gap between SPICE and IBIS, slow adoption of the core *-AMS languages mean that the library has not seen public acceptance.

In contrast, more general purpose application languages like Matlab* enjoy support due to availability of simple analysis functions without significant programming overhead. These languages are increasing in popularity for SERDES algorithmic analysis, but still suffer due to a lack of PCB and SI system-oriented analysis and element definitions (such as transmission lines, input thresholds for switching analysis and the like). Arpad recommended that either the *-AMS support in the IBIS community be enhanced, perhaps through new development environments, or SI-oriented libraries and templates for the more general purpose programming languages be developed, to support PCB and system SI analysis.

THE 3S PROPOSAL: A SPICE SUPERSET SPECIFICATION FOR BEHAVIORAL MODELING

Michael Mirmak, Intel Corporation

Michael presented a proposal for standardizing the SPICE format, to support behavioral, non-active-device modeling. As many tool and device vendors find SPICE a reasonably simple and familiar format, having a standard SPICE instead of proprietary versions, would significantly ease model distribution and reduce conversion costs. SPICE is also useful for system netlist exchange. However, few elements are shared between proprietary SPICEs, forcing any standard SPICE to define a macro-model element, as well as a compatibility "switch," to cover

incompatible native element definitions. Other hard choices remain regarding options and evaluation methods. Finally, allowing different results due to different algorithms is increasing intolerable by some parts of the SI community, as speeds increase. Verilog-A represents a viable alternative to defining a standard SPICE, as it is already standard, supports behavioral modeling, is gaining widespread support and is capable of representing system netlists. Verilog-A also does not carry any of the burdens of a digital language syntax.

Several suggestions were made by participants in response to the proposal. The suggested use of an A-element as a way to instantiate macromodels was opposed, as at least one university SPICE defines different A-element functionality. Additionally, participants suggested that the exclusion of active devices may make a standard SPICE less desirable. Subcircuits were suggested as a simple way to ensure common behavior by proprietary SPICEs.

IBIS-ATM UPDATE - SERDES MODELING AND IBIS

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd summarized the recent work of the IBIS Advanced Technology Modeling Task Group in creating a standard API for algorithmic modeling under IBIS. Currently, the analysis of advanced serial-differential (SERDES) interfaces relies on linear-time-invariant (LTI) behavior and network theory to predict channel performance quickly. This ties the analog behavior of a passive channel, in response to a pulse response, to the non-LTI behavior of equalizing drivers and/or receivers. These devices may perform complex computations on outgoing and incoming data, beyond what current IBIS techniques support.

The proposed algorithmic modeling API would enable device designers to express their device algorithmic behaviors as compiled code, responding to pulse response waveforms or streams of data. Analog simulation would only be conducted on the channel response. A C-language wrapper around the executable code would allow EDA tools to link analog simulations with standard parameters and data streams passed in and from the algorithmic code.

Work is nearly complete on a proposal eligible for consideration by the Open Forum, and support from EDA vendors and model authors is strong. Test equipment vendors have also expressed interest in the proposal. The team expects to submit the proposal as a BIRD for IBIS 5.0 after working demonstrations have been created and provided to the IBIS community. This is expected in the fall of 2007.

CONCLUDING ITEMS AND NEXT MEETING

The formal presentations concluded at 4:30 PM. Michael asked about additional topics, but none was proposed. He adjourned the meeting.

The next Open Forum teleconference will be held June 22, 2007 from 8:00 AM to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org
In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda-stds.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda-stds.org)
IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt

http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	April 20, 2007	May 11, 2007	June 1, 2007	June 5, 2007
Advanced Micro Devices	Producer	Active	√	√	√	
Agilent Technologies	User	Inactive				√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
Cadence Design Systems	User	Inactive				√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active	√	√	√	√
Green Streak Programs	General Interest	Inactive			√	
Hitachi ULSI Systems	Producer	Inactive				√
Intel Corp.	Producer	Active	√	√	√	√
LSI Logic	Producer	Inactive				
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Active	√	√	√	
Samtec	Producer	Inactive				
Signal Integrity Software	User	Inactive				√
Sigrity	User	Inactive				√
STMicroelectronics	Producer	Active	√	√	√	
Synopsys	User	Inactive				
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Active			√	√
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive				√
ZTE	User	Inactive				
Zuken GmbH	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
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- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.