

---

# More on Initial Delay Issues

---

2007 DAC IBIS Summit

Lance Wang

IO Methodology Inc.

[lwang@iometh.com](mailto:lwang@iometh.com)



# Agenda



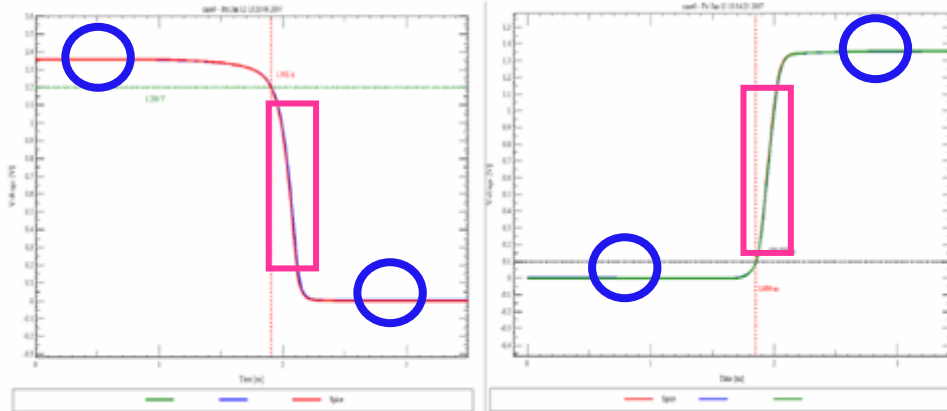
- Last presentation revisit
- Dive into IBIS simulation implementation
- Situations and solutions
- Conclusions

# Last presentation revisit



## Driver Model: Transistor-level Spice model vs. IBIS model

- Perfect matching results on Rising and Falling between all three simulators



Good for only Rising or Falling stage

VT curves reached stable zone

Ramp rate:  
 $0.8\text{v}/115\text{ps}$

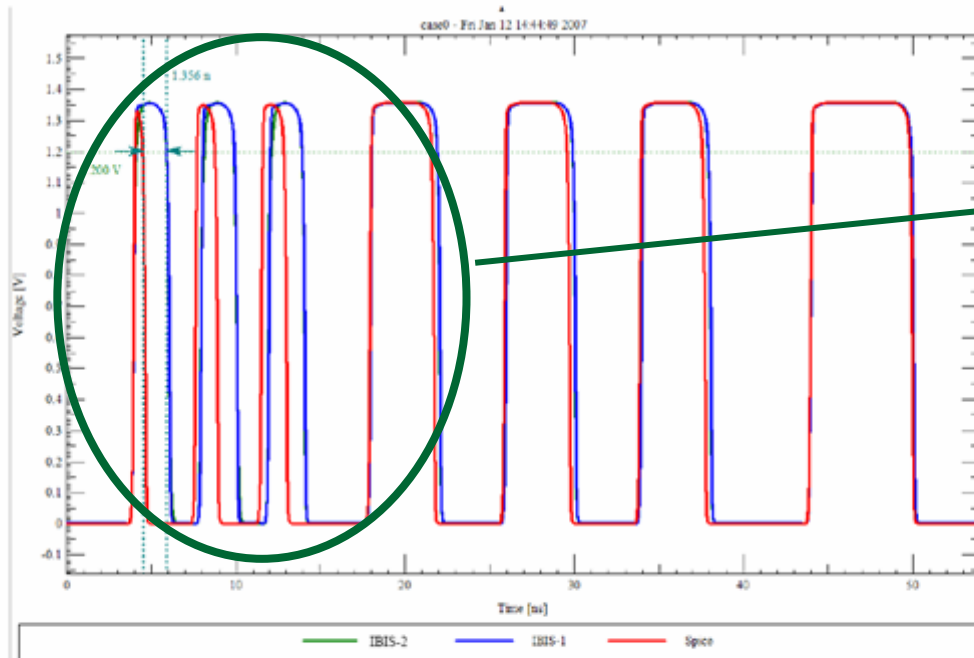
**This is a good IBIS model**

# Last presentation revisit



With full VT waveforms

- Stimulus patterns “010101001100110011000111000”



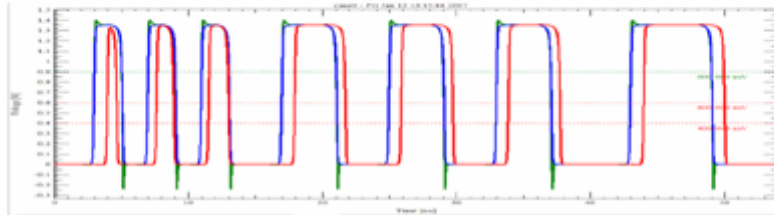
This is an ISI issue, not only timing

# Last presentation revisit



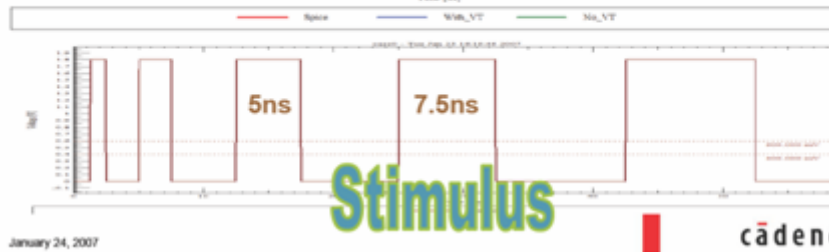
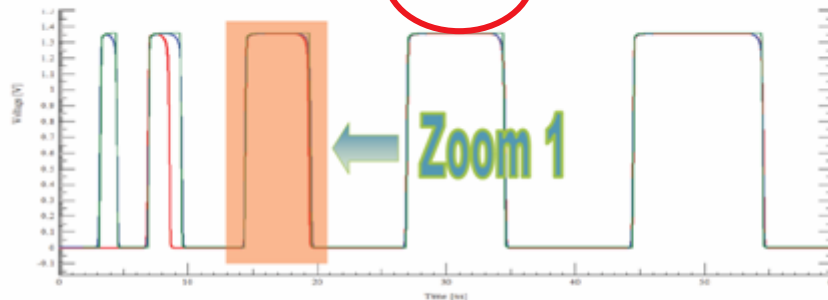
With cut off 1ns delay VT waveforms

- Stimulus patterns "010101001100110011000111000"



IBIS Simulator-1

- Spice vs. with\_VT vs. no\_VT



Cut out extra delay or not  
use VT curves does not  
solve the issue

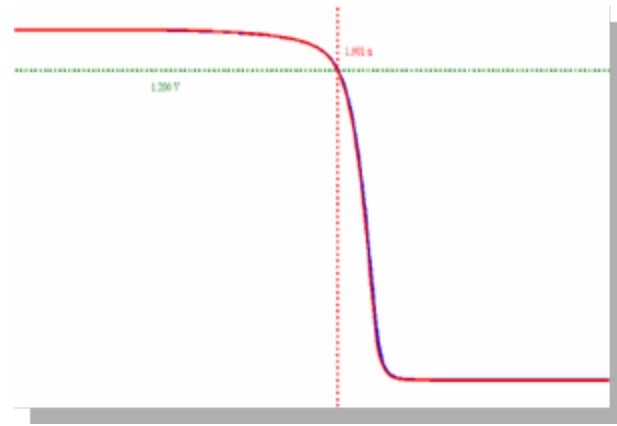
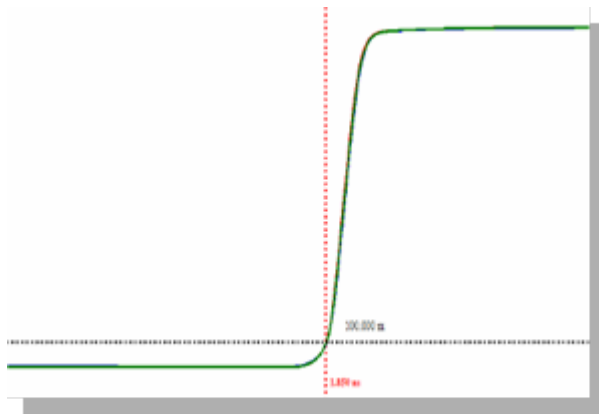
# Dive into IBIS simulation implementation



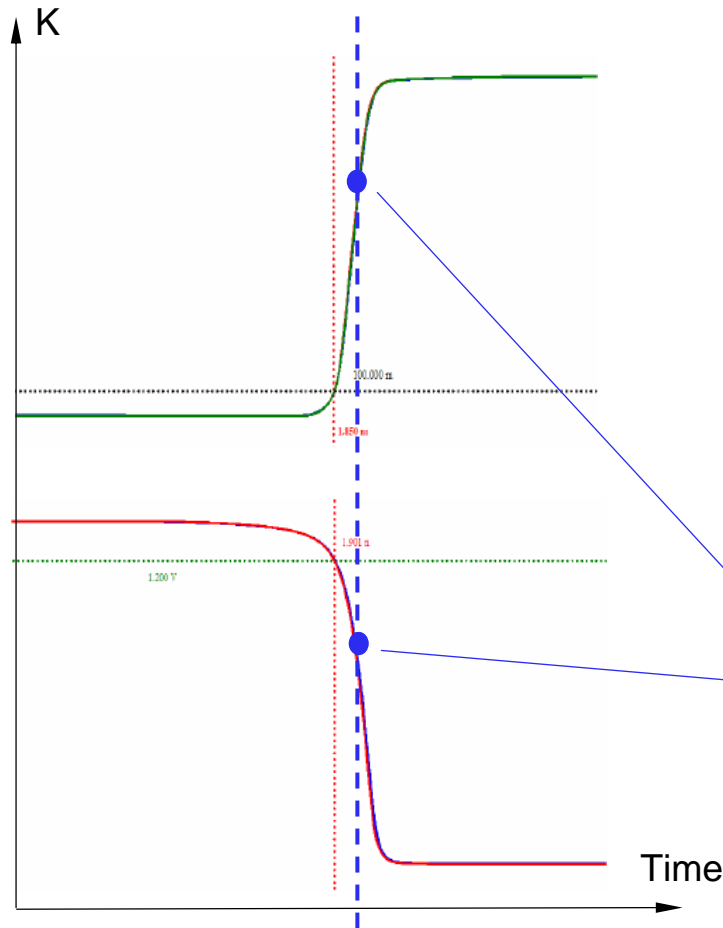
## General IBIS Output Equation

$$-I_{\text{out}}(t) = K_u(t)I_{\text{pu}}(V) + K_d(t)I_{\text{pd}}(V) + I_{\text{pc}}(V) + I_{\text{gc}}(V)$$

Important  $K_u(t)$  and  $K_d(t)$



# Dive into IBIS simulation implementation



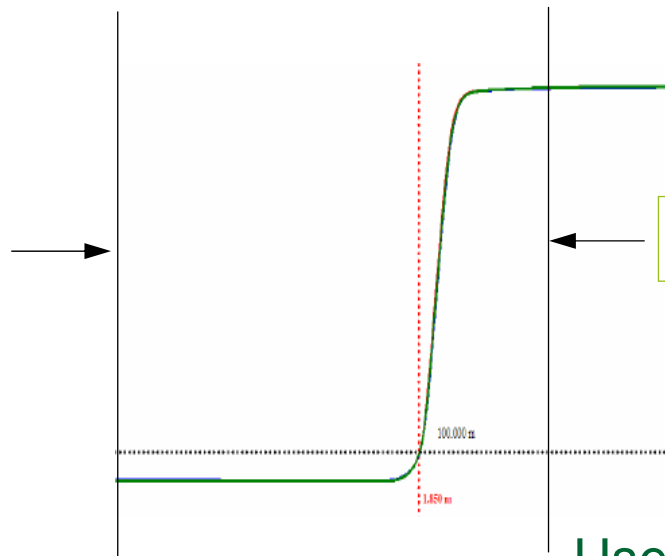
- Simulators care starting time not ending time
- Always assume both Ku and Kd will reach stable state (full state transition period)

Current IBIS implementation is not good for incomplete transition cases

# Situations and solutions



- How to avoid this problem
  - Let assumptions to be true



$T(r/f)s$  – (Rise/Fall) Safe transition period

Rising and falling  $T_s$  may be different

Use it only when stimulus state transition time (minimum bit width) is greater than  $2 \times T_s$

# Situations and solutions



- Can simulation equation be enhanced?

One possibility:

$$-I_{\text{out}}(t) = K_{\text{us}}(t)I_{\text{pu}}(V) + K_{\text{ds}}(t)I_{\text{pd}}(V) + I_{\text{pc}}(V) + I_{\text{gc}}(V)$$

where  $K_{\text{us}}(t) = K_{\text{u}}(t) * f(\text{state\_transit})$

$$K_{\text{ds}}(t) = K_{\text{d}}(t) * f(\text{state\_transit})$$

$f(\text{state\_transit})$ : transition factor

# Conclusions



- Current IBIS implementation is not good enough for ISI analysis
  - Cut off initial delay or not use VT curves does not solve the problems
- Your IBIS model may be not good enough for high speed digital signals
  - You will have more reasonable Error Rate analysis results if your minimum bit width is great than  $2 \cdot T_s$  (safe transition period)
- Can IBIS output equation be enhanced?
  - One possibility is to add signal transition factor



# The Hope starts here!

**Fully Customized Internal Tool  
Development and Maintenance Services**

**[www.IOMeth.com](http://www.IOMeth.com)**