Power Integrity Analysis for High Speed ASICs

Meng Liqiang Liu Xiaoxuan

Meng.Liqiang@zte.com.cn Liu.Xiaoxuan1@zte.com.cn

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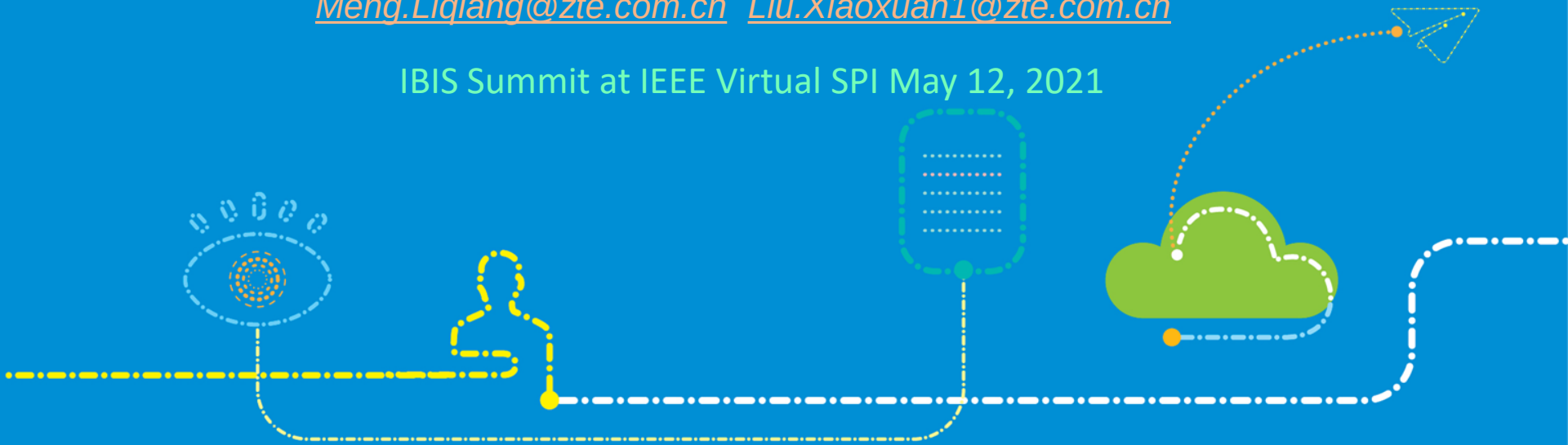
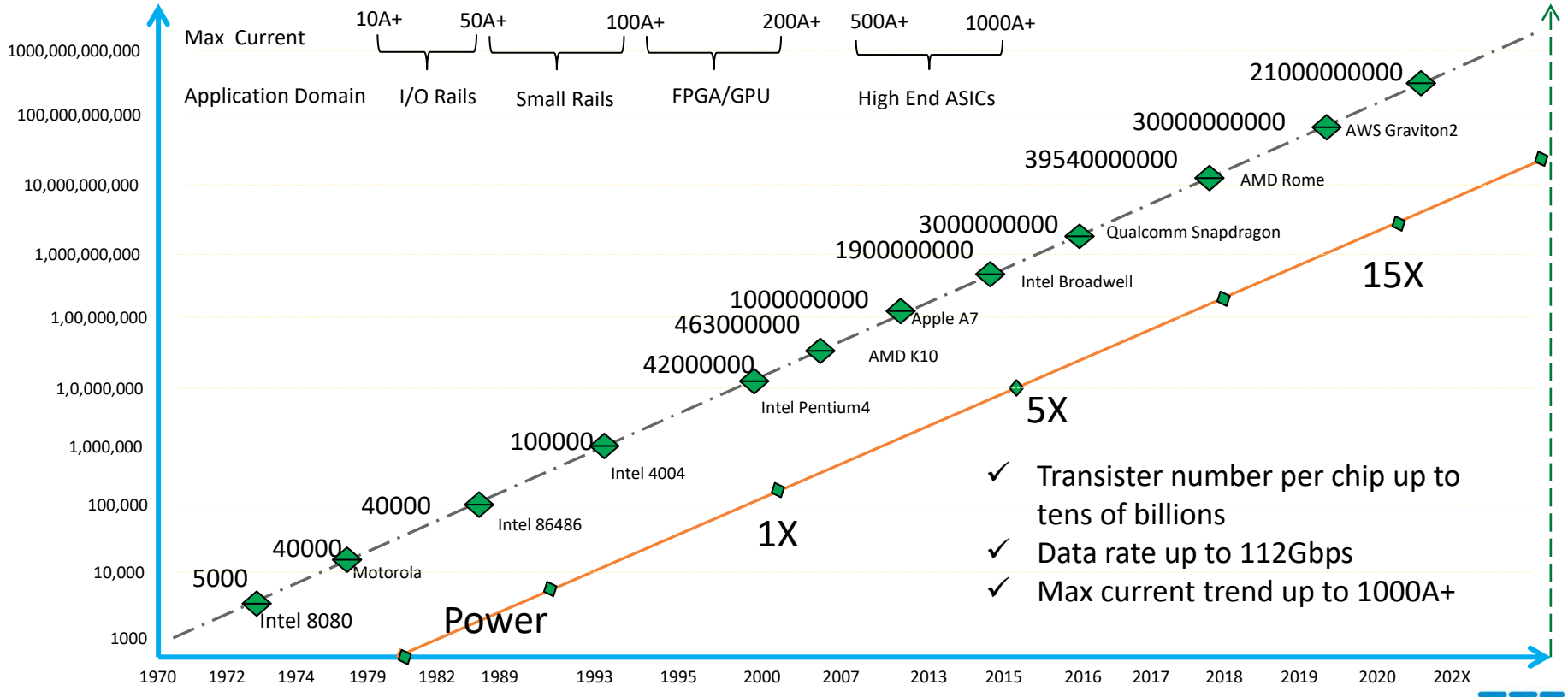


Agenda

- Maximum Current in Different Application Domains
- PDN Characteristic Impedance Design
- PDN Design Flow with CPM Model
- Summary

Maximum Current in Different Application Domains



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Target Impedance Definition

- The transient current is the maximum current change at any possible operation
- If transient current reaches up to hundreds of Amps, the target impedance will become smaller

$$Z_{PDN} < \frac{V_{tolerance}}{I_{transient}} = \frac{Vdd \times tolerance}{I_{transient}} = Z_{target}$$

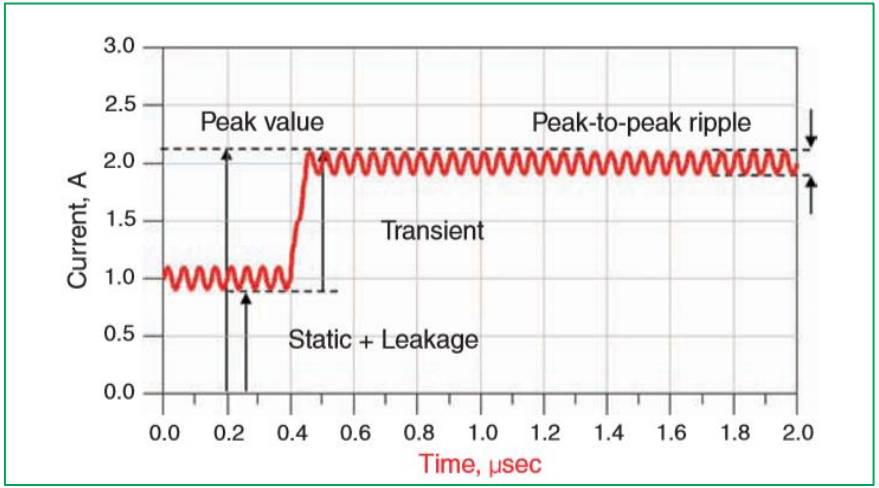

Figure 1. transient current

Pre-Simulation for High-Speed ASICs

➢ Basic information

- ✓ Supply voltage is 1 Volt
- ✓ Max current is 380 Ampere
- ✓ Transient current is 50% of Imax
- ✓ V_ripple is 5%

➢ Characteristic Impedance results

- ✓ Z_target is about 0.00026 ohm
- ✓ The calculated Z_target is extremely low as illustrated in Figure 2
- ✓ Even with 415 decaps at pre-simulation stage, the characteristic impedance Zeff is still far away from Z_target

Item	CAP Value (μF)	QTY
1	0.047	100
2	0.1	250
3	22	10
4	47	30
5	330	5
6	470	20
Total Capacitor Count		415

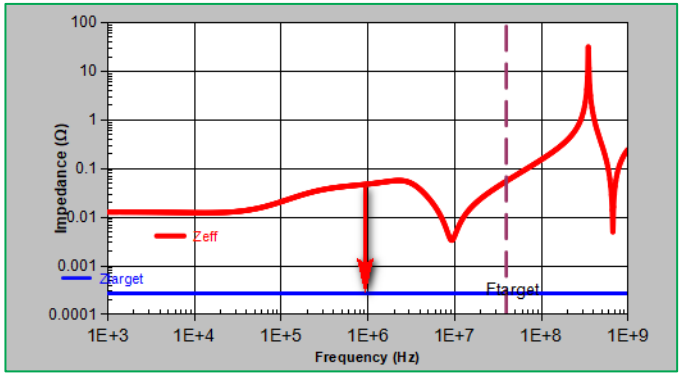

Figure 2. A Real Project PDN Impedance Design

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Transient Analysis

- The traditional target impedance design cannot meet the requirement in case of heavy current
- It is very necessary to use the CPM model for transient analysis

- VRM and CPM are provided by vender
- PCB model is extracted with precise DC point
- Set up for AC and transient analysis

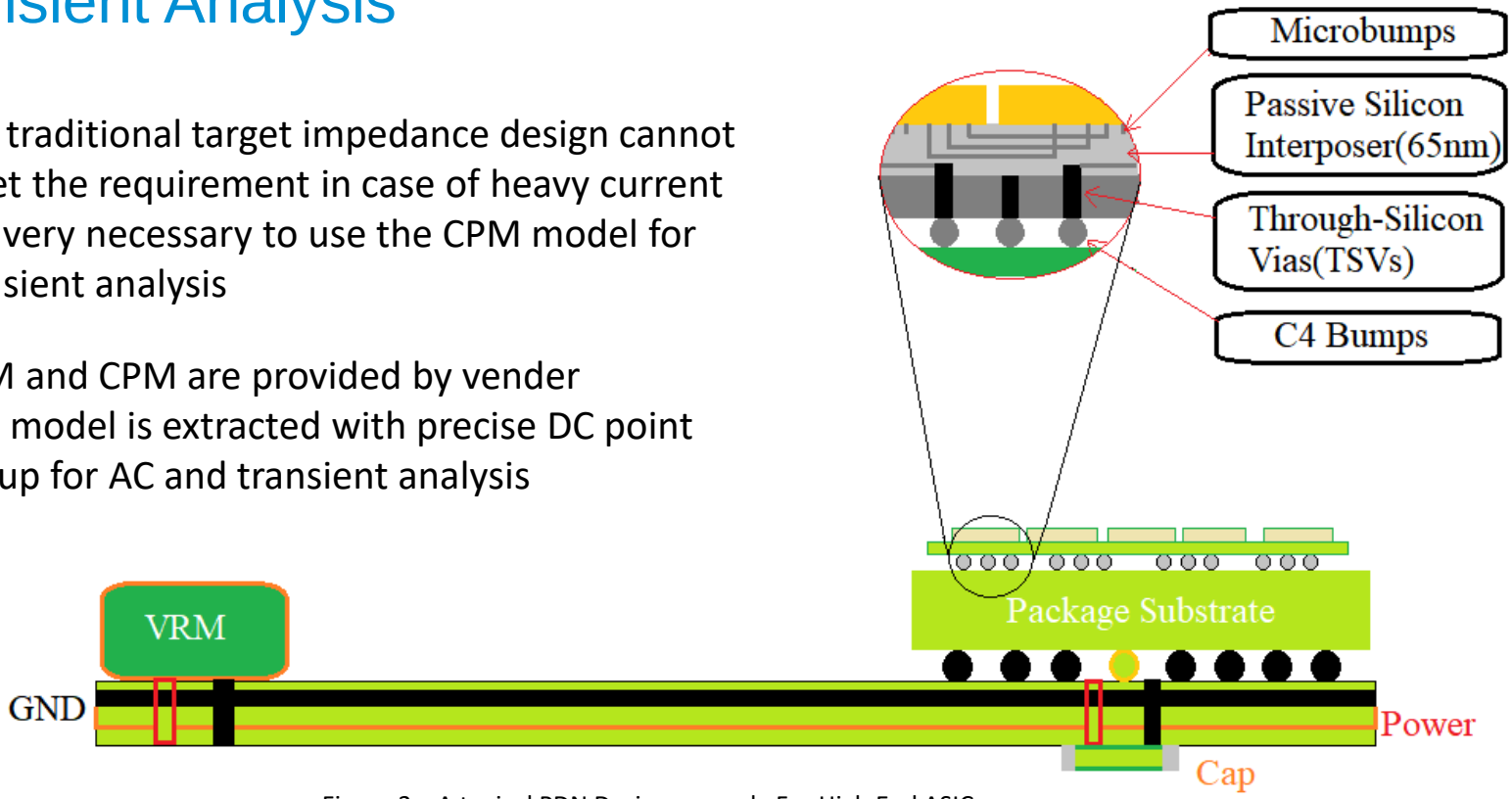

Figure 3. A typical PDN Design example For High End ASICs

Chip Power Modeling

CPM model consists of

- Package and Die Decaps info
- Controlled transient current

Transient analysis can provide

- Noise on die
- Noise at bumps
- Resonance
- Optimization of decaps on PCB
- Tradeoffs for die and package decaps
- As a reference target impedance

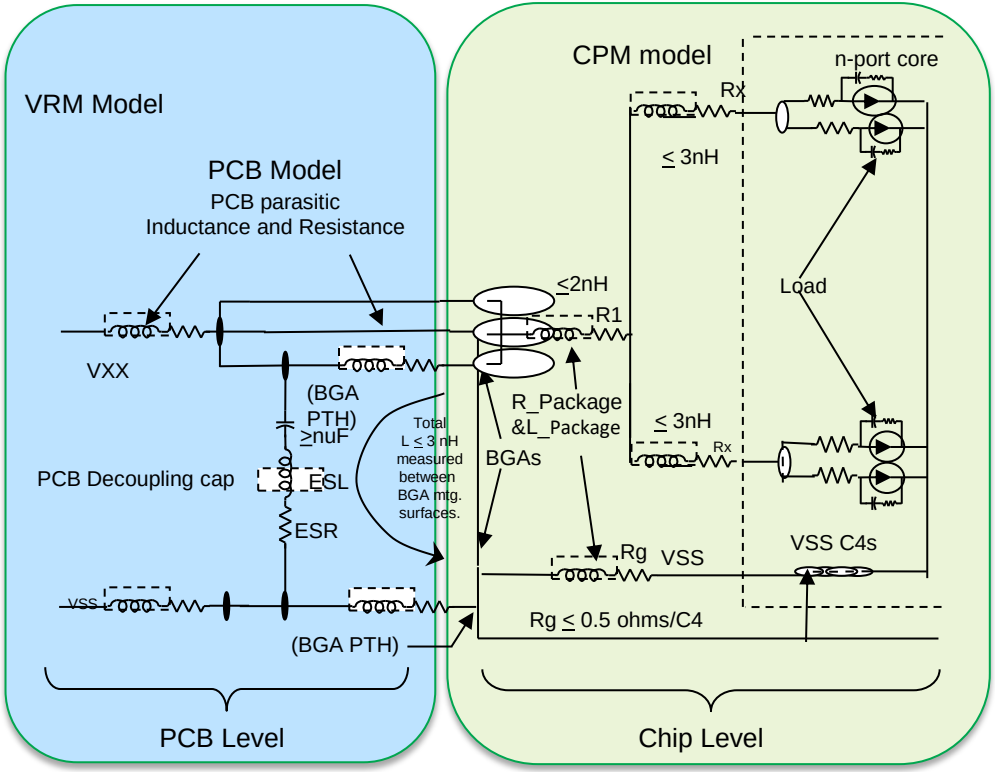

Figure 4. PDN Model Diagram

Simulation Setup

- VRM RLC or SPICE model
- PCB Broadband SPICE or S-parameter
- PKG S-parameter or RLC model
- Controlled current model under different operating modes on die

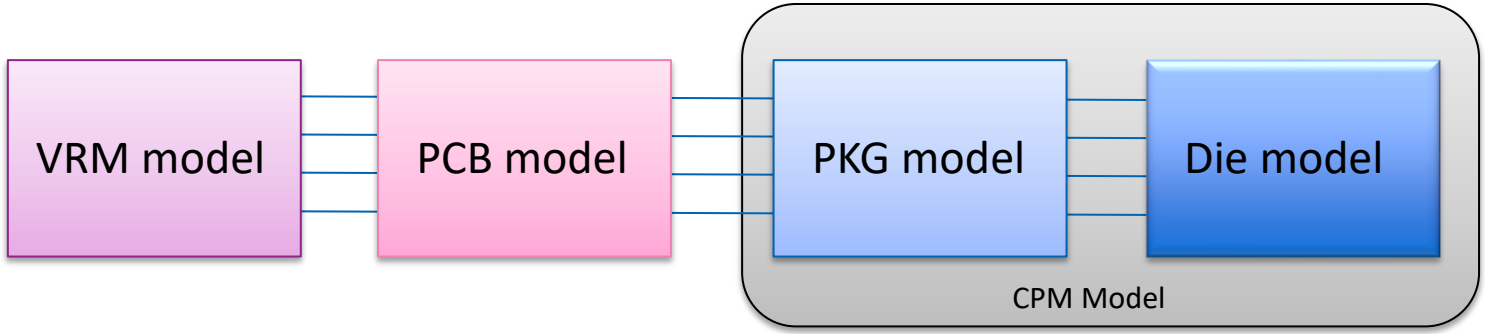

Figure 5. System Simulation Setup for Core VDD

Simulation Result

- Input and Requirement
  - 380A+ max current
  - Delay the power up/down current waveform as follows
    Lane 1: 0ns and Lane 2: 200ns ~Lane 8: 2500ns
  - AC+DC total 6% Tolerance
- Transient Analysis Results
  - AC noise is 1.9%
  - DC IR Drop is 4%
- Characteristic Impedance Results
  - Target Impedance as low as 0.00026 ohm below 10MHz (Blue)
  - Characteristic Impedance is about 0.004 ohm at post-simulation Stage (Red)
- Conclusions
  - Even though the characteristic impedance is worse than target impedance, transient analysis shows that AC noise meets the requirement
  - This characteristic impedance can be considered as target impedance for similar designs with the same chip

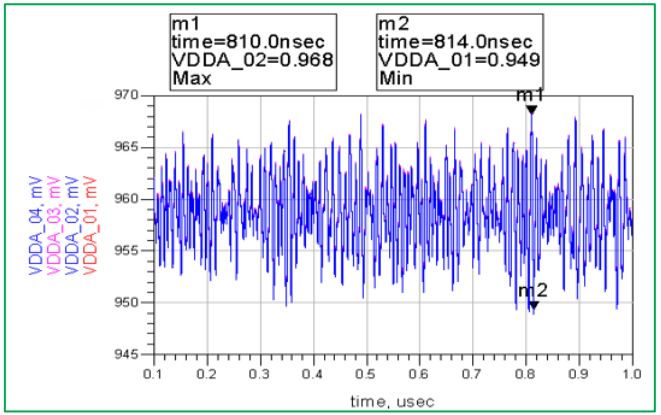

Figure6. Transient Analysis Result

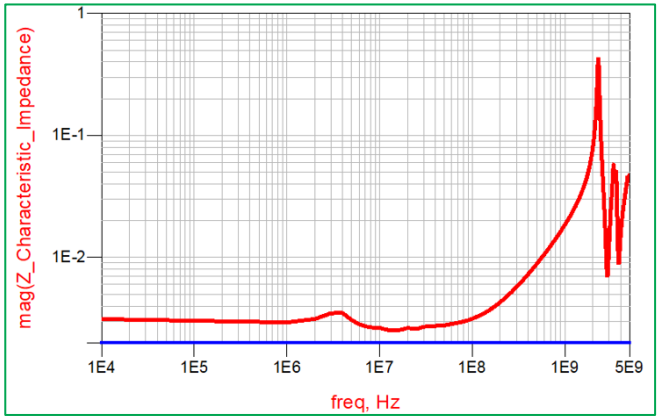

Figure7. Characteristic Impedance Result

Validation

- Transient Analysis Result
  - 16mV@BGA (red: m3-m5)
- Measurement Result
  - 18.8mV@BGA，test BW is 20MHz
- Conclusion
  - There are 14% difference between simulation and measurement ,which both meeting the requirement of AC tolerance

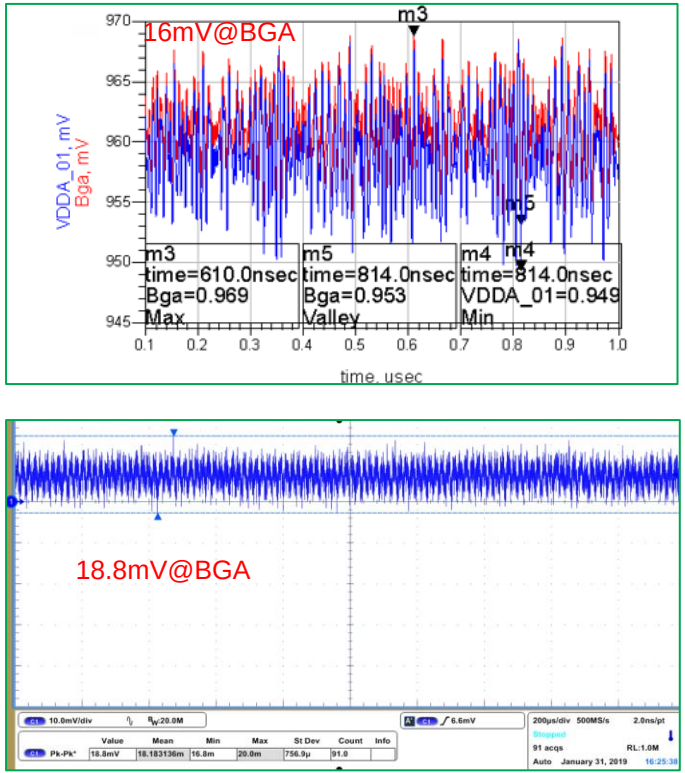

Figure8 . Transient Analysis Simulation vs Test

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Summary

- It is very difficult to meet the requirement of target impedance when there is a heavy current at the PCB level
- Characteristic impedance obtained from transient analysis with CPM model can serve as a reference target impedance for similar designs
- Relatively accurate CPM model is required
- Power up/down current sequence can be optimized for different blocks

Thank you

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