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Fast Simulation of Analog Circuit Blocks under Nonstationary Operating Conditions via Reduced Order Equivalent Circuits

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Intro

SOC/SIP







Simulating components behaviors

Raw subdivision of the components



Passive - Linear



Active devices - Nonlinear



Simulating components behaviors

Different first-principle models

e.g. Maxwell
$\nabla \cdot D = \rho$ $\nabla \cdot B = 0$ $\nabla \times E = -\frac{\partial B}{\partial t}$ $\nabla \times H = J + \frac{\partial D}{\partial t}$
Passive - Linear



Active devices - Nonlinear



Simulating components behaviors

Reduced Order Equivalent circuits





Semiconductors-NL



Analog Circuit Blocks

Amplifiers, LDOs, Filters, Oscillators...

Schematic. Preliminary design



Transistor models only

Including layout (possibly packaging)



Transistor models + RLC elements



LDO test-case



A Transient simulation requires minutes on our hardware (72-core 2.3GHz CPUs, 128Gb RAM)

30 MB netlist !

T. Y. Man, P. K. T. Mok and M. Chan, "A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 9, pp. 755-759, Sept. 2007.



The CB Interacts with the external system



 $u \equiv \text{Port Voltage}$ $y \equiv \text{Port Current}$

$$\begin{bmatrix} U_0: \text{Bias voltage} \\ Y_0: \text{Bias current} \end{bmatrix} = \begin{bmatrix} \widetilde{u}: \text{ voltage small signal} \\ \widetilde{y}: \text{ current small signal} \end{bmatrix} = \begin{bmatrix} \widetilde{u}: V_0 \\ \widetilde{y}: C_0 \\ \widetilde{$$

Linearized Models for Small Signal Analyses



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Small signal componenents approximation



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Restoring the appropriate bias level



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Post layout circuit equations are encrypted in the netlist. We collect AC data and perform rational approximation.



Once the small signal model is available, compute the required Y_C from a DC analysis. Equivalent netlist synthesis is possible



Bias point: $V_{DD} = 1V$, $I_L = 5mA$ Small-signal: Sequential square pulses of amplitude $\pm 25mV$ over V_{DD} Computed time span: $100\mu s$



Regulated Voltage

Model time requirements: 93 ms

Transistor level post Layout: 63 s





Affine linearized models are valid only for a single operating point



DC components combinations at each of the P ports define different bias conditions

The bias point parameterizes the small signal transfer function (and the output correction level)

Equivalent Circuit via Parameterized Rational Fitting





For our LDO test case







Model structure and generation



Small-Signal Model ($V_{DD} = 1V$)

Dynamic order: 9

Parameter Dependent Basis: Chebyshev Polynomials of order 4 and 3 for numerator and denominator respectively

208 AC responses were exploited for fitting



Dashed Red Lines : Model Blue Lines: AC sweep data

Parameterized Small-Signal Model ($I_L = 10mA$)

Stability is preserved for all bias conditions using standard parameterized macromodeling techniques (more on this later)

Group



Dashed Red Lines : Model Blue Lines: AC sweep data



A more involved simulation scenario



A Linear Time Invariant (LTI) equivalent circuit is instantiated depending on the SPICE DC point analysis. U_0 is uncertain but constant

What if the operating point changes during the simulation?

Nonstationary bias conditions



A Linear Parameter Varying Model

We would like our model to track the operating point variation

Standard small sig. analysis

 $u(t) = \frac{U_0}{U_0} + \tilde{u}(t), \qquad \tilde{u}(0) = 0$

- The bias is U_0 is constant and determined via OP analysis ($U_0 = u(0)$)
- The linearized model is instantiated accordingly
- The equivalent circuit is linear time invariant

 $\dot{x} = A(U_0)x + B(U_0)u$ $y = C(U_0)x + D(U_0)u + Y_c(U_0)$

Dynamic small sig. analysis

 $u(t) = U_0(t) + \tilde{u}(t), \qquad \tilde{u}(0) = 0$

- The bias is determined by a large time varying signal $U_0(t)$
- The linearized model should depend on the instantaneous value of $U_0(t)$
- The equivalent circuit should be time varying

 $\dot{x} = A(U_0(t))x + B(U_0(t))u$ $y = C(U_0(t))x + D(U_0(t))u + Y_c(U_0(t))$



The same modeling framework can be adapted to the LPV case

ASSUMPTIONS

$$u(t) = U_0(t) + \tilde{u}(t), \qquad \tilde{u}(0) = 0$$

If it holds that

- $\tilde{u}(t)$ is still a small signal component
- $U_0(t)$ is slow wrt the circuit response

The circuit instantaneously works around the OP induced by $U_0(t)$ as if it was constant



Under the previous assumptions, the modeling workflow is as follows

- 1. Define the range of admissible values for $U_0(t) \in \mathcal{U}_0$ (a hypercube)
- 2. Repeatedly sample the circuit SS transfer function over \mathcal{U}_0 , via AC analyses with different STATIC bias configurations
- 3. Build the multivariate rational approximation $H(s, U_o) = \frac{N(s, U_o)}{D(s, U_o)}$, and the parameterized affine term $Y_C(U_0)$
- 4. Cast the rational transfer function into a parameterized time-varying equivalent circuit with components depending on $U_0(t)$ or in SS

 $\dot{x} = A(U_0(t))x + B(U_0(t))u$ $y = C(U_0(t))x + D(U_0(t))u + Y_c(U_0(t))$



Two main problems must be solved to generate reliable models

- 1. During online operation the bias component $U_0(t)$ is merged with the small signal.
- 2. If the circuit block is known to be stable under the action of u(t) so must be the model.

To tackle the above we propose to

- 1. Embed in the model a low pass filter that extracts $U_0(t)$ from u(t)
- Constraint the model generation to guarantee stability in a time varying setting



Bias Component Extraction

The total input signal $u(t) = U_0(t) + \tilde{u}(t)$ is filtered to extract $U_0(t)$





Robust LTI stability for standard parameterized macromodels



If $D(s, U_0)$ is a passive immittance function, then its zeros have strictly negative real part.

Stability enforcement

The same criterion is not applicable for the proposed LPV model



With appropriate model structure, the unknowns $r_{n,\ell}$ can be found via convex programming to ensure asymptotic stability

Bradde, Tommaso, et al. "Fast Simulation of Analog Circuit Blocks Under Nonstationary Operating Conditions." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 11.9 (2021): 1355-1368.

Nonstationary bias conditions



$$V_{DD} \in [2.85, 3] V$$

$$\dot{x} = A(U_0(t))x + B(U_0(t))u$$

$$y = C(U_0(t))x + D(U_0(t))u + Y_c(U_0(t))$$

Excellent AC accuracy



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Transient simulation







The LPV model performs much better then standard Linearized time invariant equivalent



A realistic test case



- We simulate a load state transition from 0.5 to 2 mA, $\Delta t = 6$ ms
- 0.2 mA small signal, noise with flat power spectrum over [1,10] kHz



Full time window

Zoom on transition

REFERENCE: 13 min, MODEL: 16 s 50 × Speed-up!

- We simulate a load state transition from 5 to 8 mA, $\Delta t = 6$ ms
- 0.5 mA small signal, noise with flat power spectrum over [1,10] kHz



Full time window

Zoom on transition



- We discussed how linearized reduced order equivalent circuits can replace native mildly nonlinear CB descriptions for fast simulations
- Three fitting-based modeling approaches are possible depending on the required flexibility-vs-time requirements



• In all cases, models are accurate, stable, and generated via automated algorithms





Thanks for your attention!

Time for Q&A



Stability enforcement

The same criterion is not applicable for the proposed LPV model

The dynamic equations $\dot{x} = A(U_0(t))x$ may be unstable even if $A(U_0)$ is Hurwitz for constant U_0

Stability can be ensured for any $U_0(t)$ trajectory through Lyapunov theory

 $\dot{x} = A(U_0(t))x$ is asymptotically stable if $\exists P > 0: A^T(U_0)P + P A(U_0) < 0$ $\forall U_0 \in U_0$

Stability enforcement



 $\dot{x} = A(U_0(t))x$ is asymptotically stable if $\exists P > 0: A^T(U_0)P + P A(U_0) < 0$ $\forall U_0 \in \mathcal{U}_0$

The state matrix $A(U_0)$ depends on the parameterized denominator coefficients $r_{n,\ell} \zeta_{\ell}(U_0)$. Find coefficients s.t. the Lyapunov condition is satisfied





Simpler sufficient conditions can be derived with suitable polynomial basis

 $\zeta_{\ell}(U_0) \equiv b_{\ell,\overline{\ell}}(U_0)$ The ℓ – th basis of Bernstein polynomials of degree $\overline{\ell}$

Positivity	Partition of unity
$0 \leq b_{\ell,\overline{\ell}} \left(\mathbf{U_0} \right) \leq 1 \ \forall \ \ell$	$\sum_{\ell}^{\overline{\ell}} b_{\ell,\overline{\ell}} \left(\underline{U_0} \right) = 1$



Stability Enforcement

Under this particular parameterization we can tackle the problem



- 1. Bases $b_{\ell,\overline{\ell}}(U_0)$ are always non-negative
- 2. The matrix coefficients $X_{\ell}(P, r_{n,\ell})$ depend linearly on the decision variables, meaning that:

