IBIS Quality Checklist Level 4 Additions

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IBIS Quality Level 4

Level 4 is declared but not defined in the current version (2.0) of the quality specification

- IQ0 - No IQ checking at all
- IQ1 - Passes IBISCHK without Errors or unexplained Warnings
- IQ2 - IQ1 + data for basic simulation checked
- IQ3 - IQ2 + data for timing analysis checked
- IQ4 - IQ3 + data for power analysis checked

1.1.5. IQ4 – Suitable for Power Analysis
An IQ4 file is suitable for power analysis. The power and ground currents associated with groups of buffers are accurately modeled. This is distinct from the signal analysis capabilities addressed by IQ2 and IQ3. This is a placeholder, since no IQ level 4 checks are currently defined. These checks will be defined in a future version of the IBIS Quality Specification. Currently no IBIS file can have an IQ4 level.

Agenda

- Section 3.1. Component Package Requirements
- Section 3.4. (new) Component Pin Mapping Requirements
- Section 5.7. (new) Model ISSO Table Requirements
- Section 5.8. (new) Model I-T Table Requirements
- Smoothness
- Comments and Discussion

3.1. Component Package Requirements

3.1.3. Package model includes power pins

Package model includes power pins with coupling between signals, power, and ground

- [Define Package Model]
- [External Circuit] not preferred
- [Interconnect Model Group] (including IBIS-ISS and Touchstone files)
- EMD

These sections should not be mixed in the same component since this situation causes confusion for the model user and possibly for the EDA tool.

The model comments should explain package modeling method.

Package modeling trade-offs

Model Type	Pro	Con
[Define Package Model]	Details for long pin interconnect	Coupled, single-stage, lumped OR T-lines with forks - not both
[External Circuit]	Existing	Possible misinterpretation Replaced by newer syntax
[Interconnect Model Group]	Very flexible	Complicated Difficult to check
EMD	Multi-die modules with coupling	Complicated Not referenced from IBS file (reversed reference) Not yet fully supported by all EDA tools

Package model guidance

Package model includes power pins with coupling between signals, power, and ground.

How much is a requirement and how much of this is guidance?

While it's valid to use a package model that does not include the coupling between signals, power, and ground pins, a good quality model includes these coupling effects. Likewise, the loop inductance through the power and return paths could be modeled by a single inductance value in the power path, but such a model does not fully represent the voltage fluctuations used in the ISSO Pulldown effect.

(guidance) How to use Touchstone (TS) file(s) for package model, since loop inductance in only one side of the loop.

Note: passivity and causality checks are slightly different between EDA tools. The model creator might comment on which tool was used to check passivity and causality.

3.1.4. On-die and on-package decoupling included

The inclusion of on-die and on-package decoupling can have a significant effect on the SSO calculation in the buffer model.

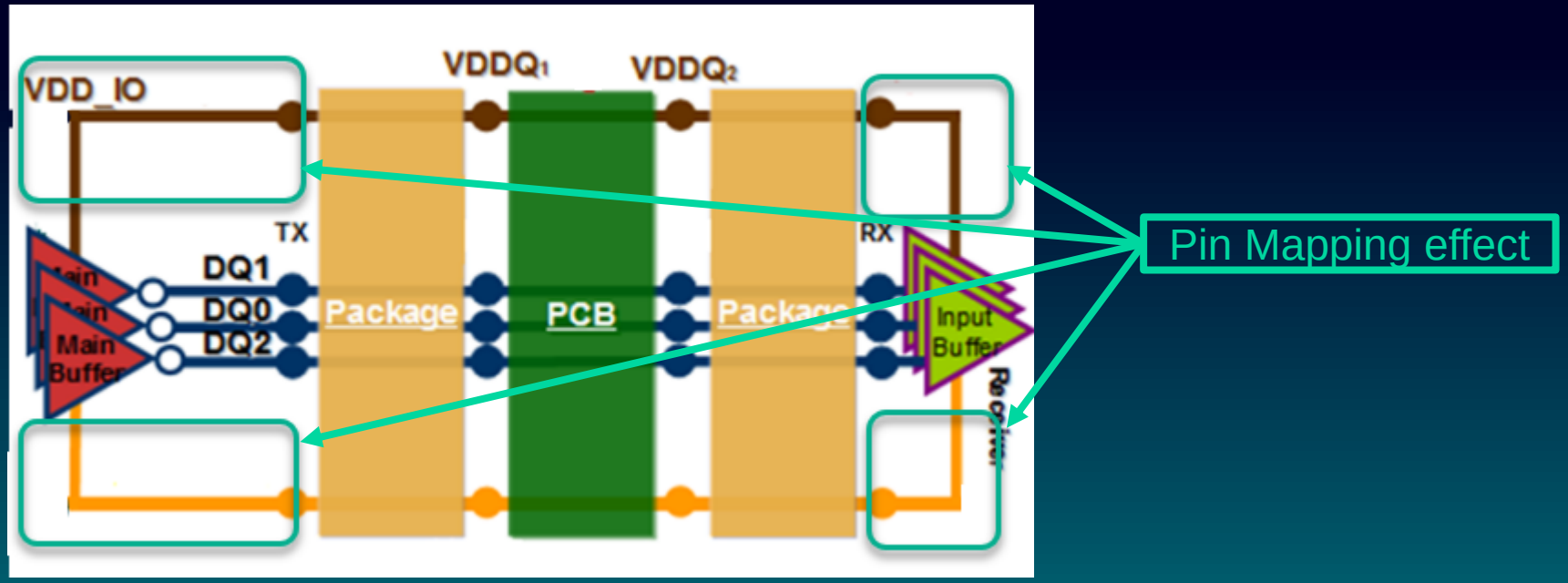
On-die decoupling (non-ideal capacitance) is an important part of the component PDN. The on-die decoupling is probably included in an:

- [Interconnect Model] section (IBIS-ISS or Touchstone models)
- [External Circuit] and [Circuit Call] sections
- [PDN Domain] section
    - new keywords and parameters in 7.1 (BIRD198.3)
    - [PDN Domain], Signal_name, Bus_label, [PDN Model], C_pdn, R_pdn, and R_leak.

The on-package decoupling is included in the package model.

3.4. Component Pin Mapping Requirements

3.4.1. [Pin Mapping] section is included



https://ibis.org/summits/nov13c/lay.pdf (6 JAN 2023)

3.4.2. [Pin Mapping] includes all I/O pins from the [Pin] section

This requirement is checked by ibischk7. The IBIS specification 7.0 states, “If the [Pin Mapping] keyword is present, then the bus connections for every pin listed under the [Pin] keyword whose model_name is not POWER, GND or NC shall be given.”

Since this is checked by ibischk, the check is classified level 1

3.4.3. [Pin Mapping] includes power and ground pins

If [IBIS Ver] < 7.0 then all power pins must be included in [Pin Mapping] section.

In version 7.0 the requirement is relaxed (BIRD182) to link [Pin Mapping] bus labels to [Pin] signal names.

5.7. Model ISSO Table Requirements

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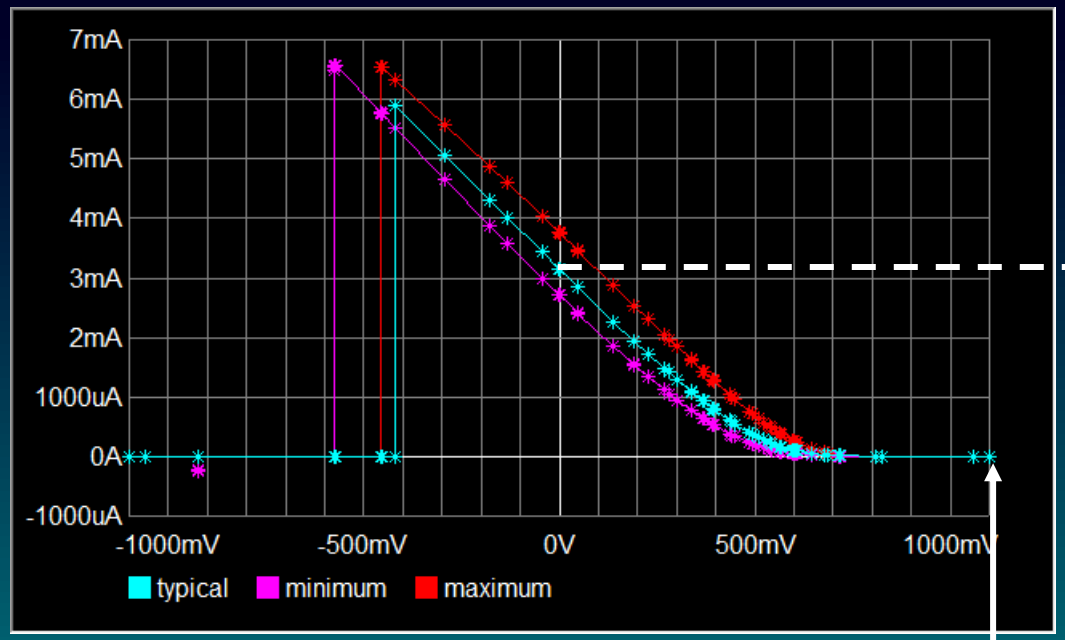
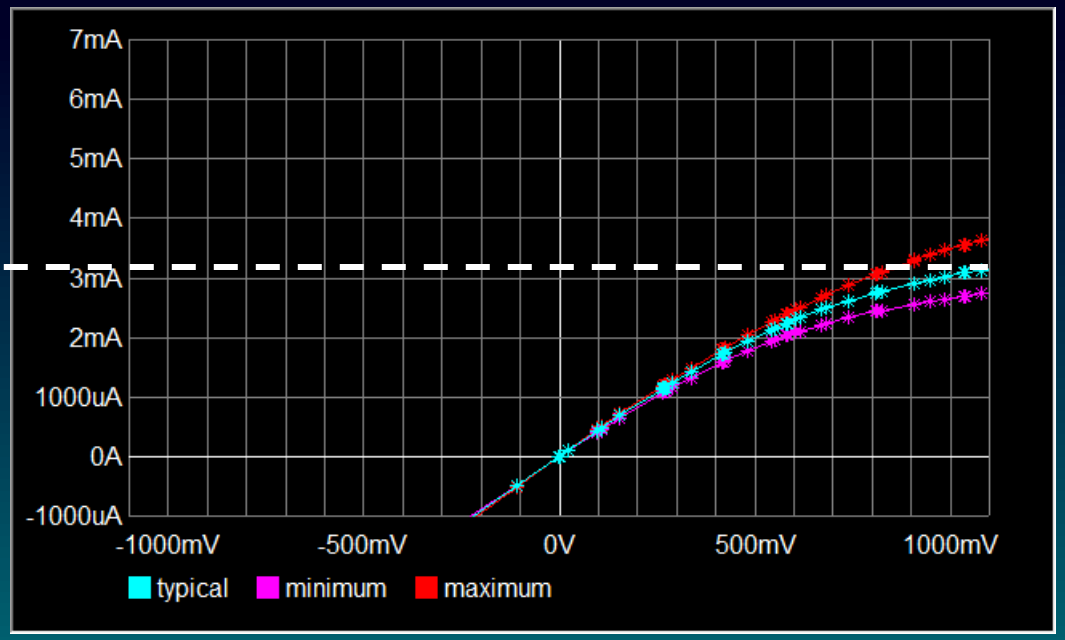
5.7.1. ISSO table data correlate with pullup and pulldown curves

IBISCHK7 checks that Isso_pd(0) = Ipd(Vcc) and Isso_pu(0) = Ipu(Vcc).
IBISCHK7 checks that Isso_pd(Vcc) = 0 and Isso_pu(Vcc) = 0.

Since this is checked by ibischk, the check is classified level 1



[ISSO PD]



[Pulldown]

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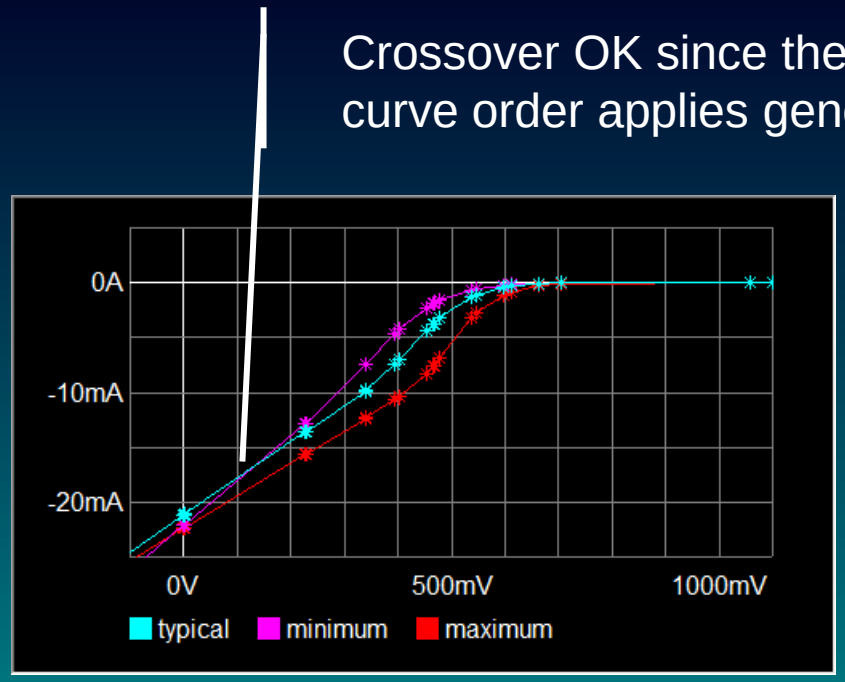
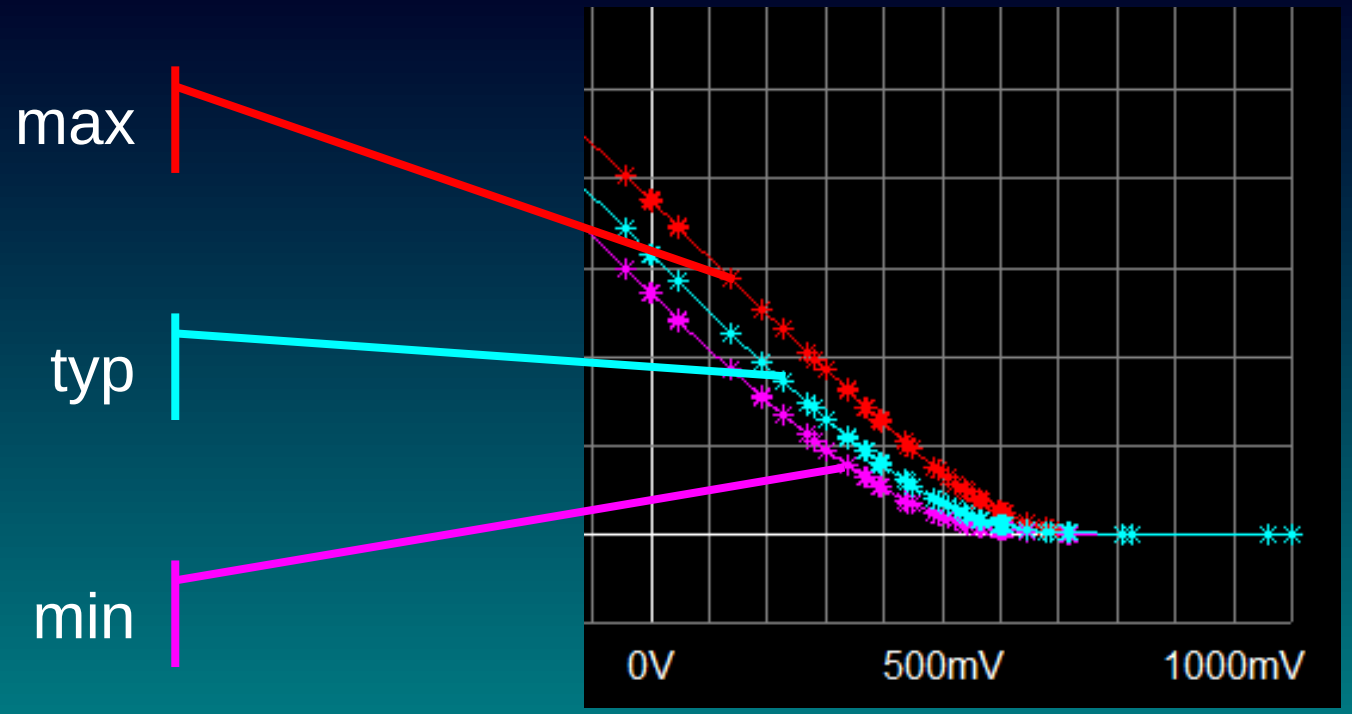
5.7.2. ISSO tables have correct typ/min/max order

Generally, the current values for each voltage point in the ISSO Pullup and ISSO Pulldown tables should have the value in the minimum column less than the value in the typical column, which is less than the value in the maximum column. Viewed as a curve, these curves might cross each other for short ranges, but the order should apply generally; |Imin| < |Ityp| < |Imax|.



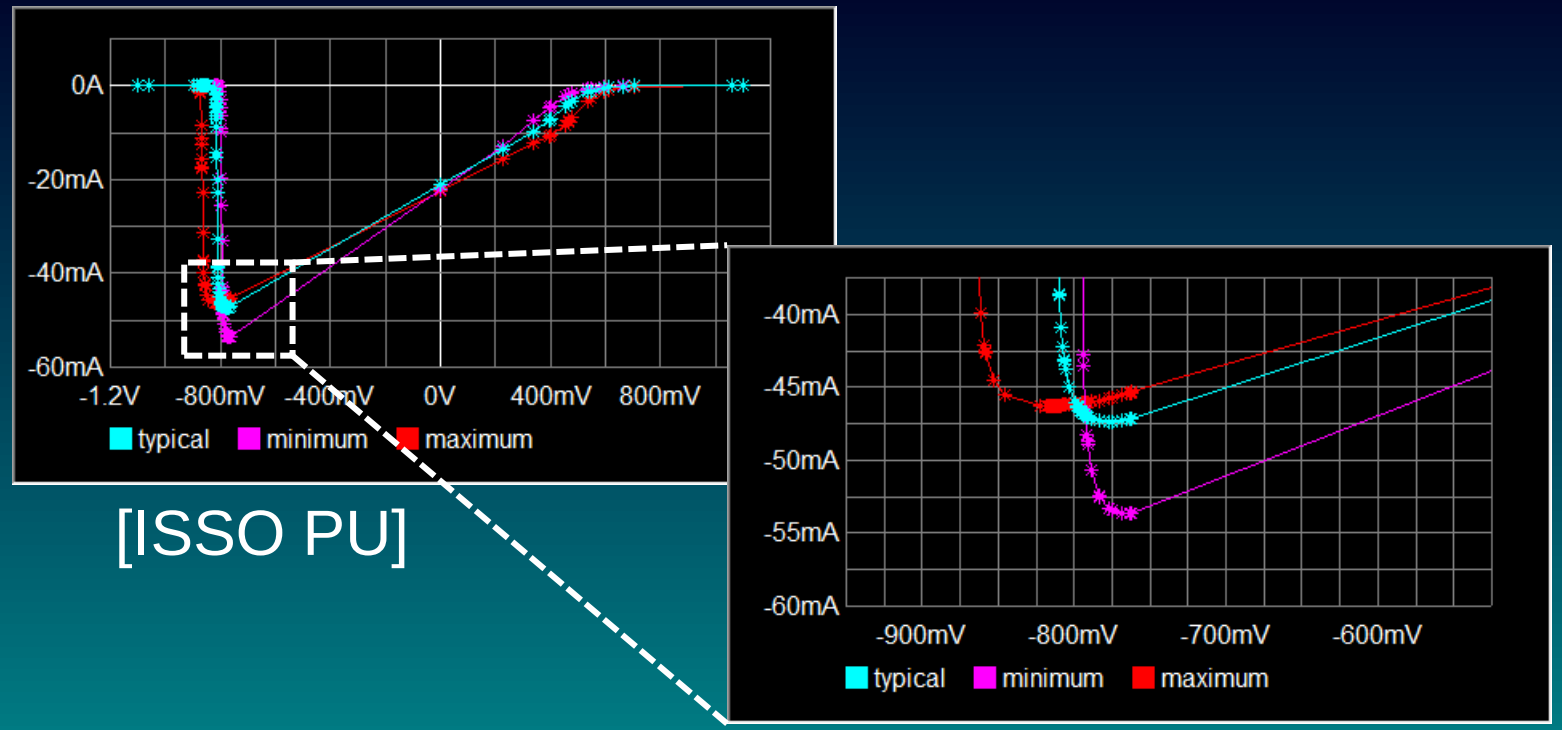
[ISSO PU]



[ISSO PD]

5.7.3. ISSO tables have sufficient point distribution

We recommend a minimum of 10 data points at points of inflection in I-V tables to prevent interpolation issues in simulations. The table data viewed as a curve should not have sharp changes of the slope of the curve. See Smoothness section.



[ISSO PU]

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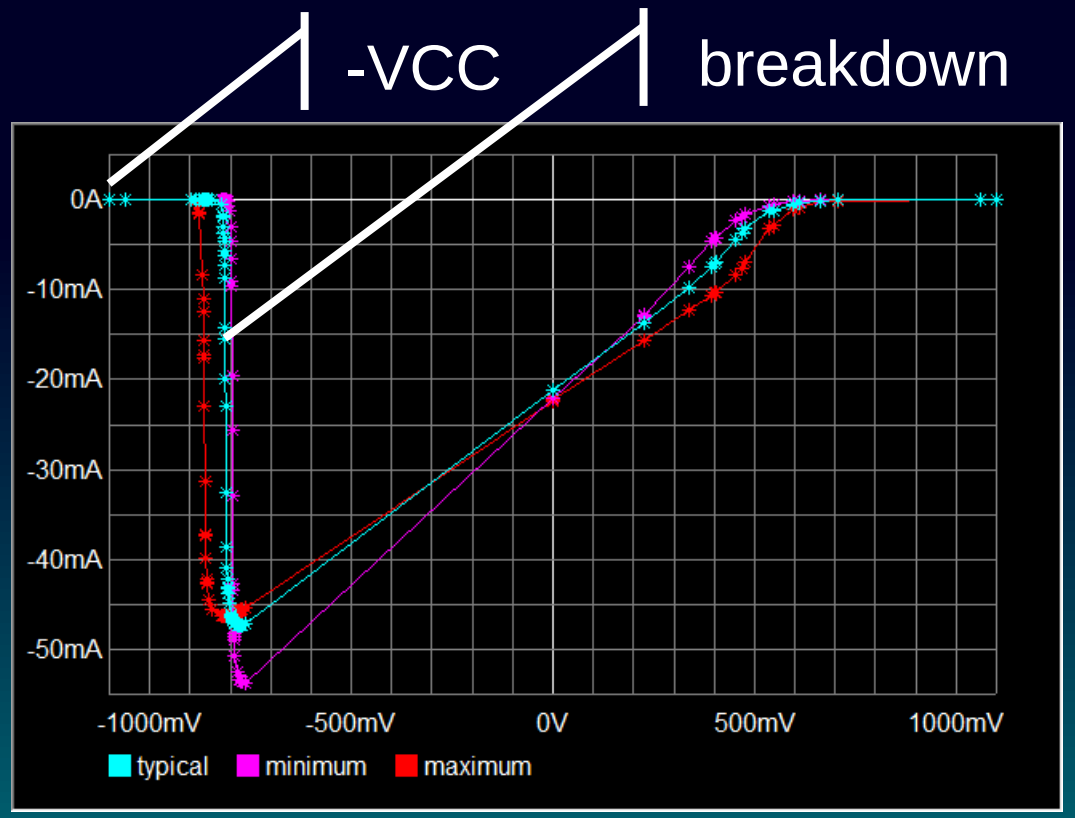
5.7.4. ISSO tables voltage sweep range is correct

The ISSO Pullup and ISSO Pulldown tables should span voltage range +/- VCC. Ibischk7 checks the correlation of the current at Vtable = +VCC, so that point is required. On the negative voltage side, the modulation behavior might break down and show 0 amps before the table voltage reaches -VCC. In this situation, it seems sufficient for the table to include the voltages down to the point where the current reaches 0 amps. But IBIS Specification version 7.1, page 91 states, “Each of the tables are aligned with and span the typical -Vcc to Vcc voltages.”



[ISSO PU]

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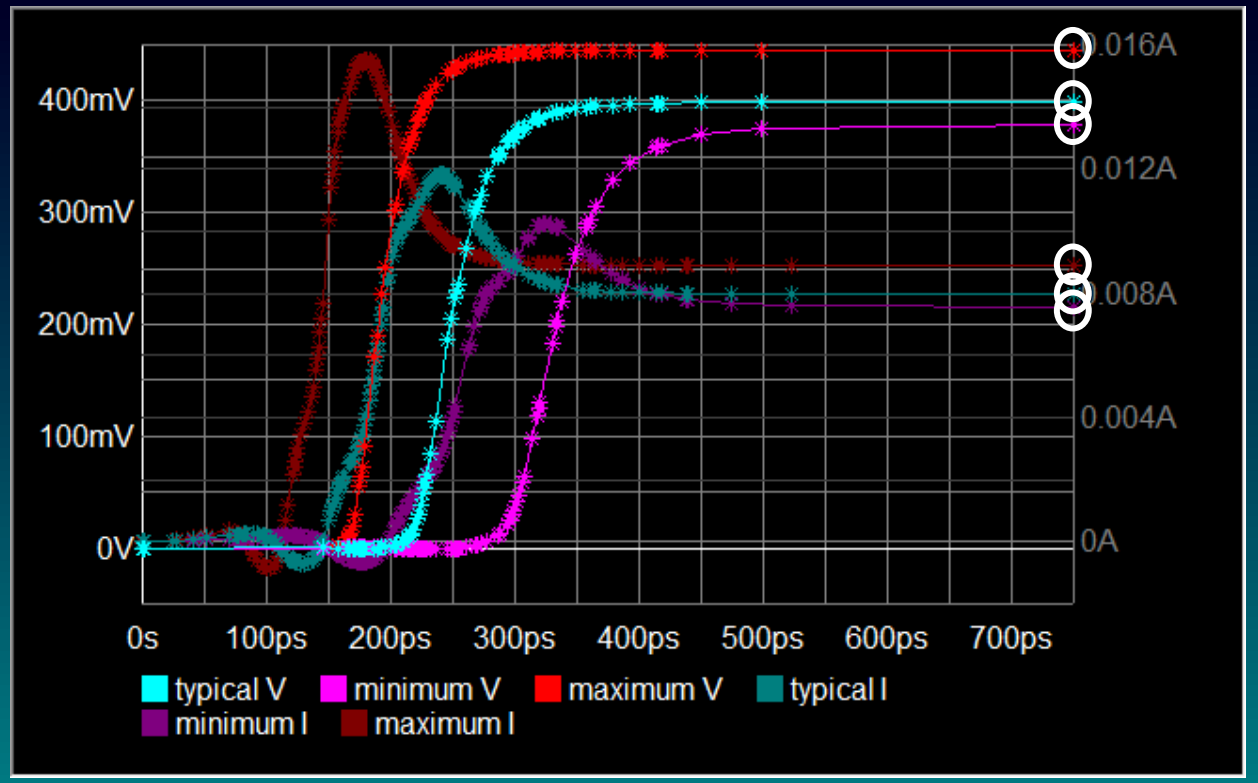
5.8. Model I-T Table Requirements

5.8.1. Composite current waveform data points cover the same time range as the corresponding V-T waveforms

The start and end times in each [Composite Current] table should be equal to the start and end times in the associated rising or falling waveform table.



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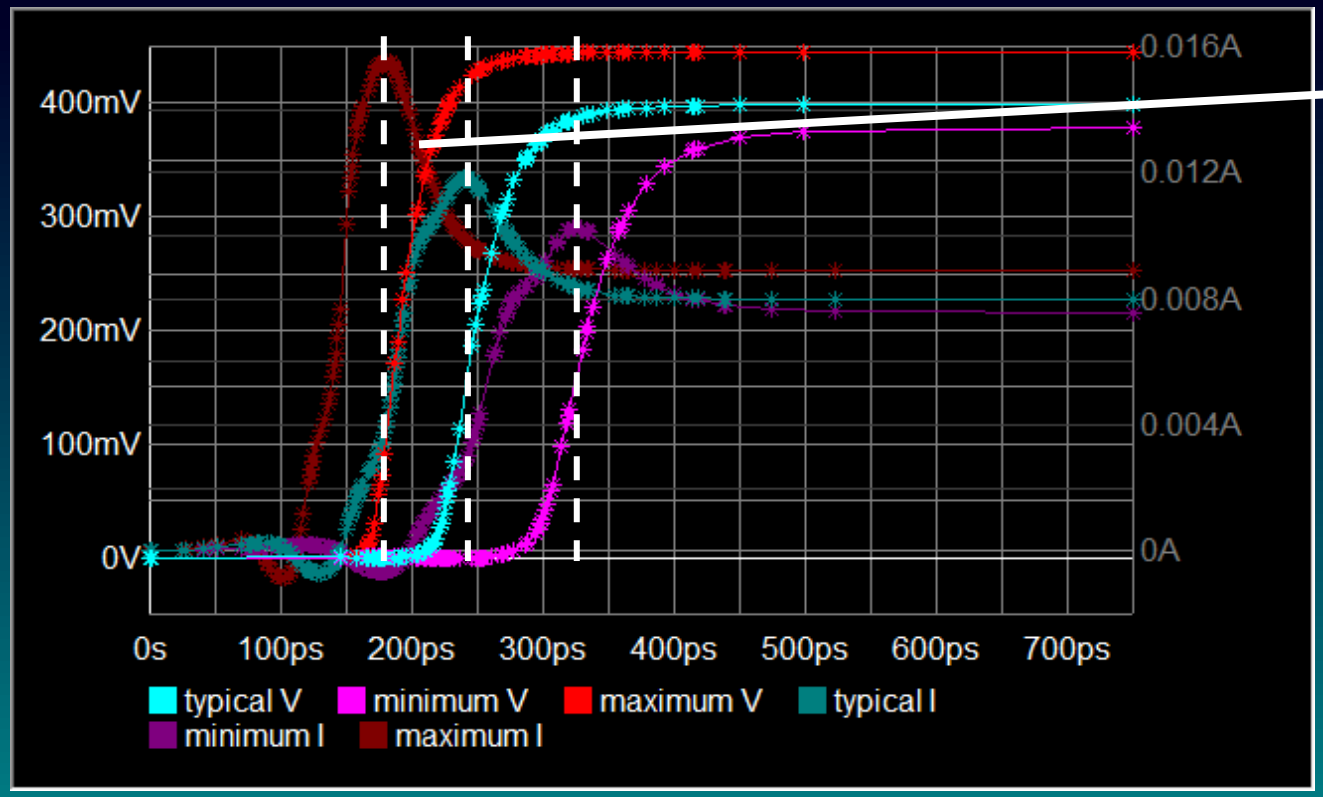
5.8.2. Composite current waveforms must be time-aligned with corresponding V-T waveforms

Each time point in the [Composite Current] table shows the current associated with the same time point (actual or interpolated) in the associated rising or falling waveform.



Peaks in current waveforms generally align with maximum slope in corresponding voltage waveforms

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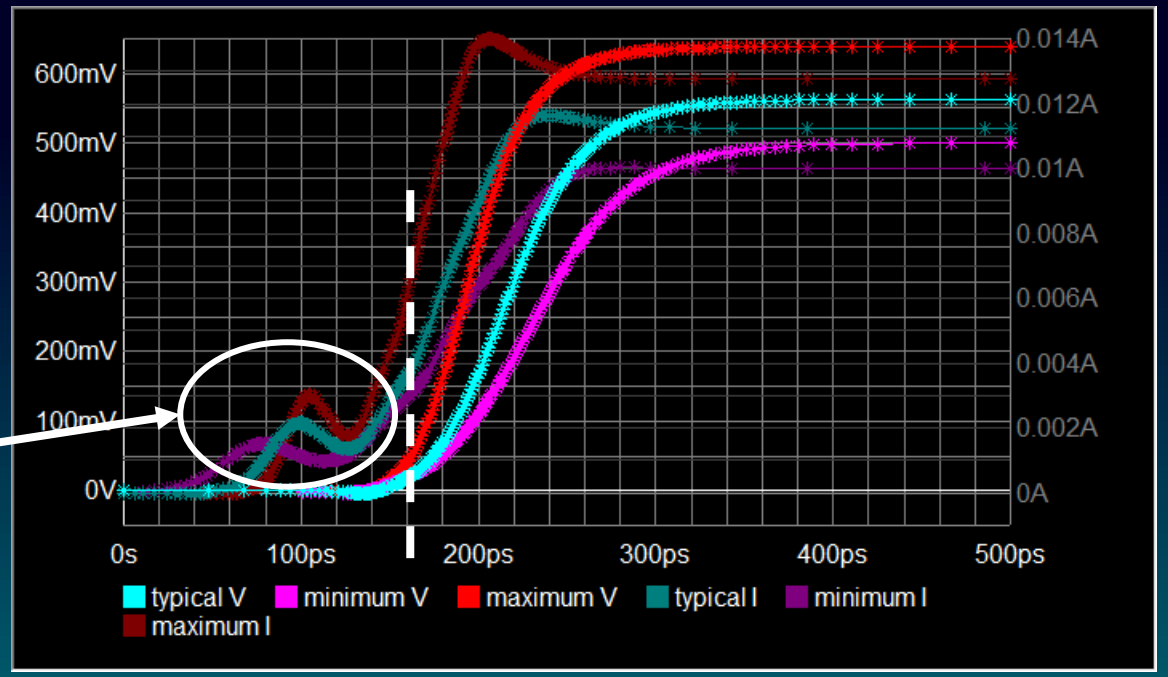
5.8.3. Composite current includes pre-driver behavior

This assumes that the pre-driver is on the same power supply as the main driver.

In keeping with the check for time-correlated current and voltage, the rising and falling waveform tables might need to be delayed with some inactive section at the beginning to allow time in the [Composite Current] table to represent the activity of the pre-driver circuit.

This requirement can be checked by looking for significant changes in the composite current curve before the associated voltage waveform shows its transition.



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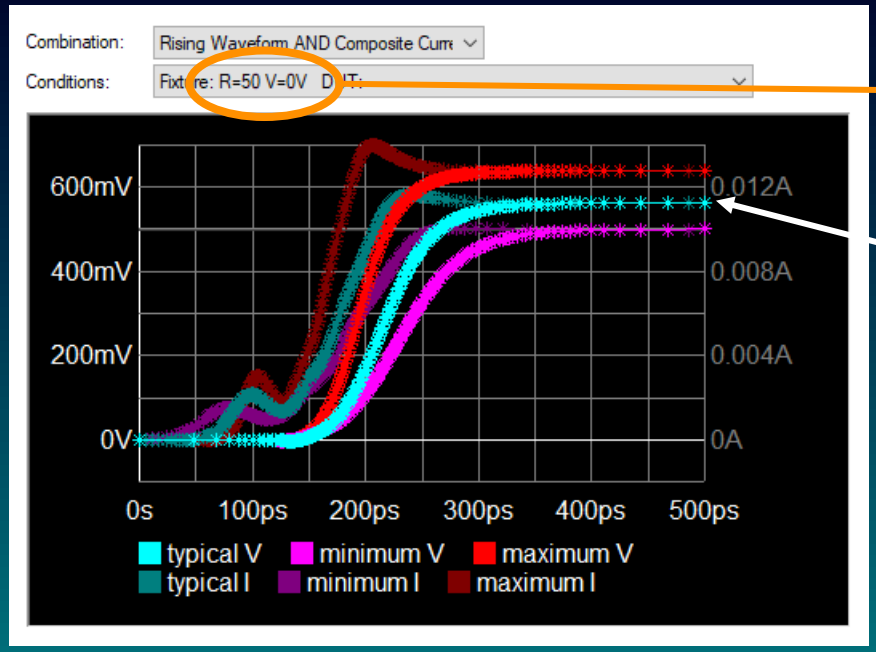
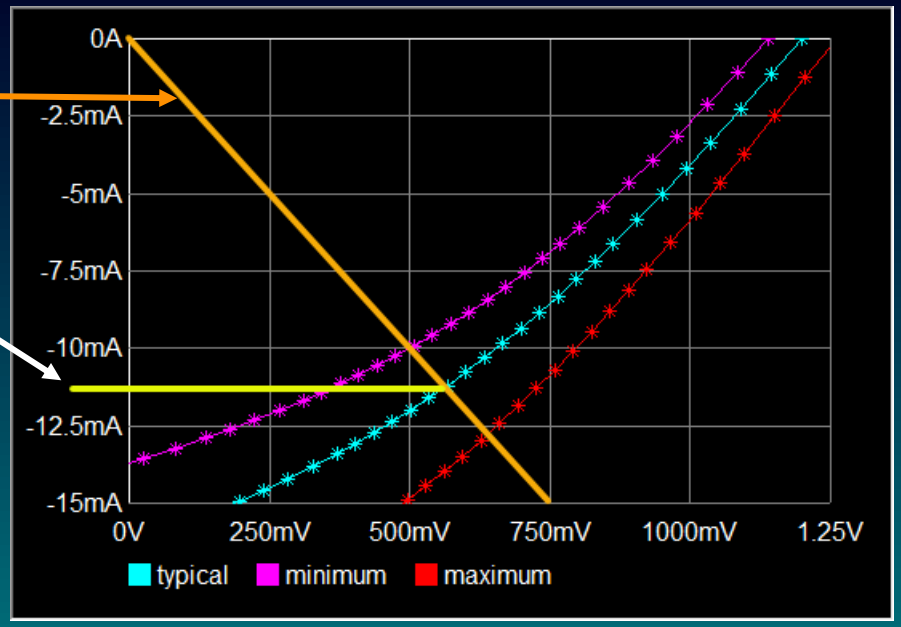
5.8.4. Start and end points composite current values correlate with pullup and pulldown

Like the start and end voltage values that ibischk7 calculates for rising and falling waveforms, the calculated current values from the load-line evaluation should match the start and end values of the [Composite Current] tables.



11.2 mA



Pullup + both clamps

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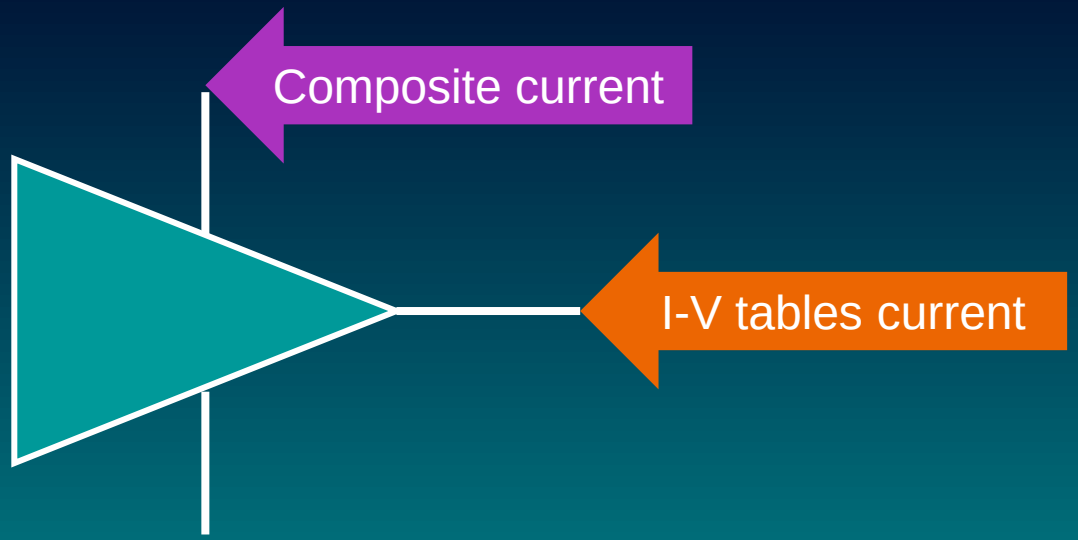
Start and end points composite current values might not match

Is this always the case?

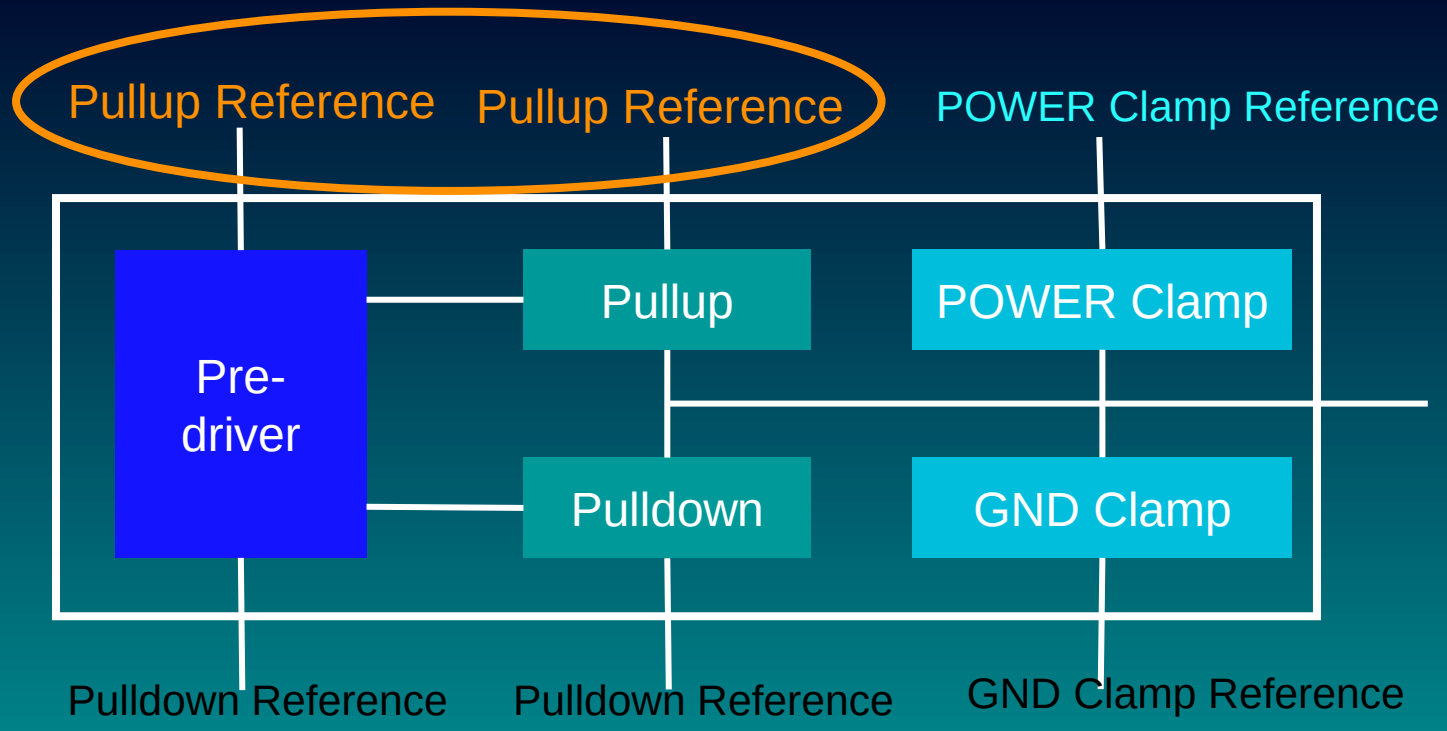
- A poorly designed pre-driver might have some constant current that would not be included in this comparison
- Sub-model currents are not included in load-line checks
- Composite current and traditional I-V tables are measured at different nodes



- The best we can hope for is correlation in the pullup state
- Does it make sense to check this correlation?

5.8.5. Composite current data includes current from correct voltage rails

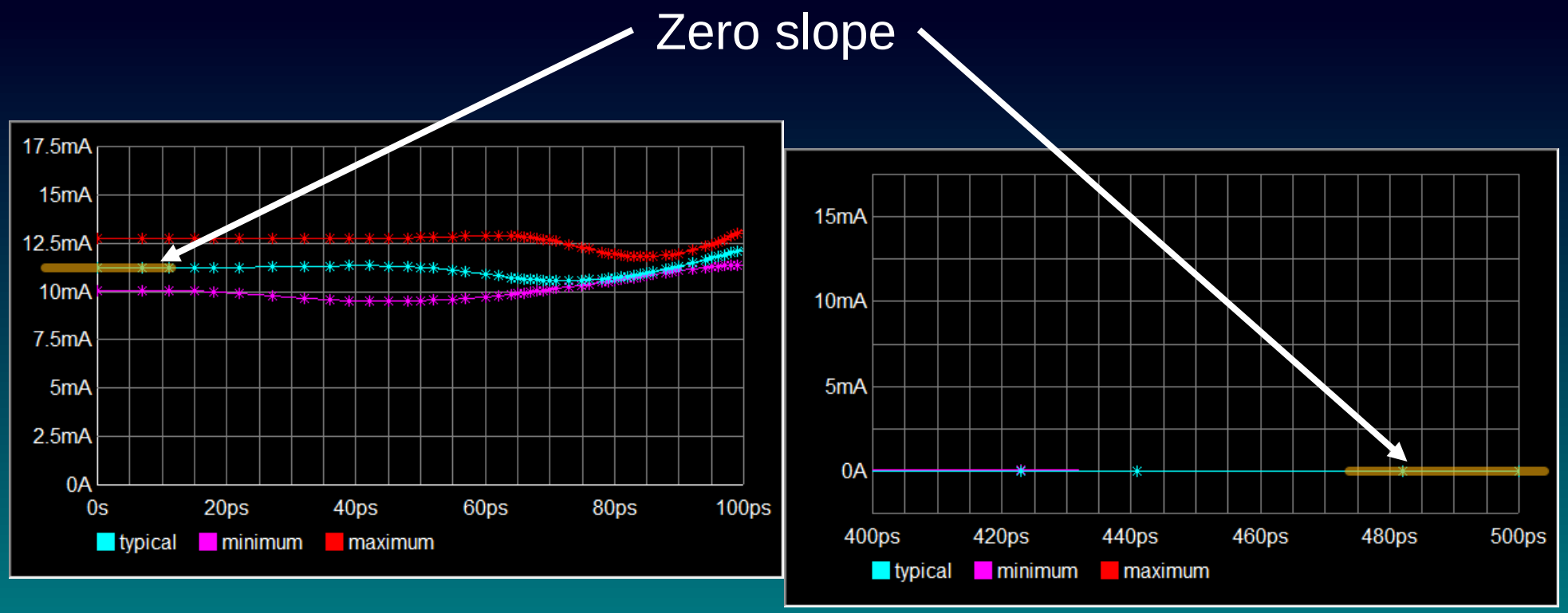
When a buffer circuit has more than one voltage supply node defined as [Pullup Reference] or [Voltage Range], the multiple currents into the circuit must be added to produce the values in the [Composite Current] table. The [Composite Current] table values do not include current from the [POWER Clamp Reference] node when the [Pin Mapping] data specifies a different bus_label for the power-clamp reference bus.



This requirement cannot be checked from the data in the IBIS file. The connections or assumptions of the data extraction should be documented in the file.

5.8.6. Composite current curve is flat at start and end

The start and end values of a [Composite Current] table might be non-zero, but the derivative of the curve should be 0. A non-zero derivative at the start or end of the curve indicates that some activity was not captured in the time range of the waveform.



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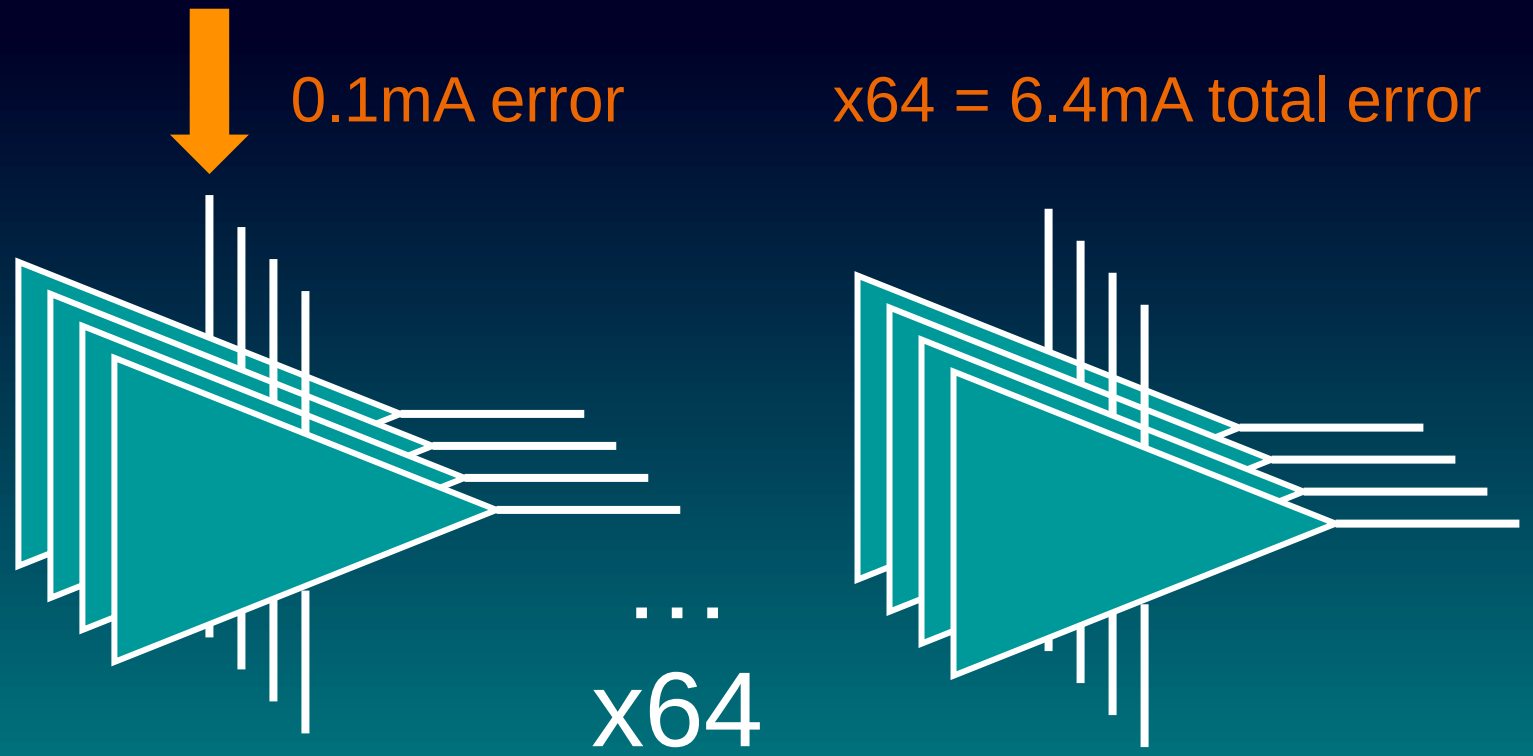
5.8.7. composite current table values should start or end at 0A

When V_fixture = 0, start of rising waveform and end of falling waveform currents must be 0 amps.
Even small current values can add up to an erroneous current flow in a multi-buffer simulation.



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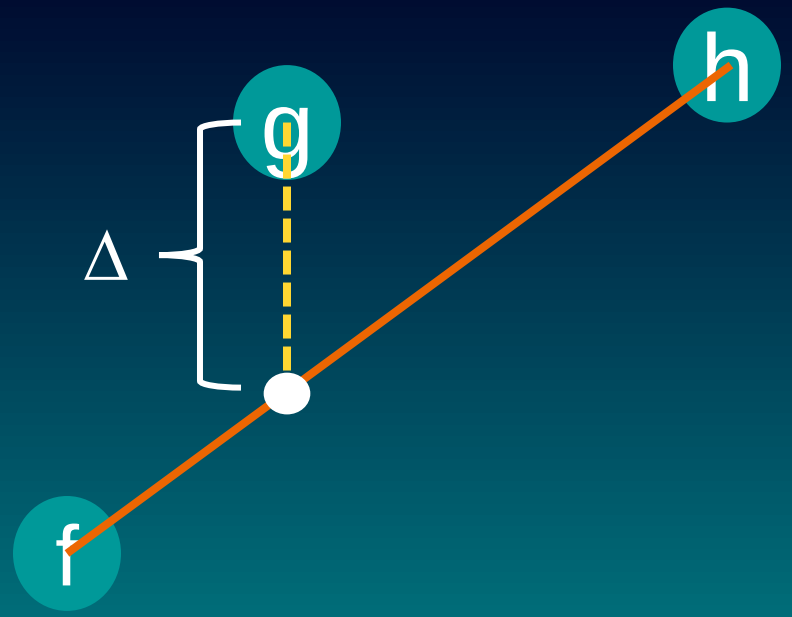
Smoothness

Smoothness checking

The smoothness of table data representing a curve can be tested algorithmically. The threshold on the smoothness metric might be adjusted with experience or to represent good, caution, or error conditions. An example of a smoothness measure follows.

1. Examine every 3 consecutive data points, f, g, and h, in the table.
2. Calculate a line segment between end points f and h.
3. Calculate the delta between the Y value of point g and the interpolated Y value at the same X value from the line segment in step 2. Smaller delta values are evidence of a smoother curve.
4. Use the delta values to calculate an average error, or RSS error, or similar metric. The X delta value is also useful to weight the Y delta values.
5. Compare the error metric to an empirically determined threshold to report a warning or error.



Comments and Discussion

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